Oversampling Converters and PLLs

Tuesday 23rd of March, 2010, 9:15 – 11:10

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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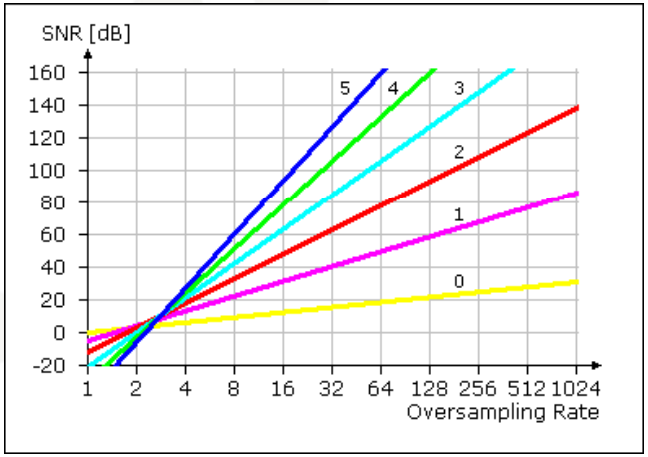
Last time – and today, Tuesday 16th of March:

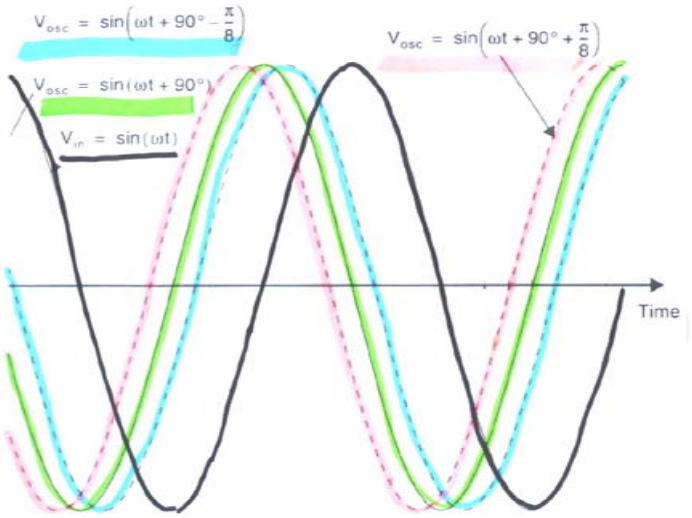
Last time:

13.6 Interpolating A/D Converters
13.7 Folding A/D Converters
14.1 Oversampled converters



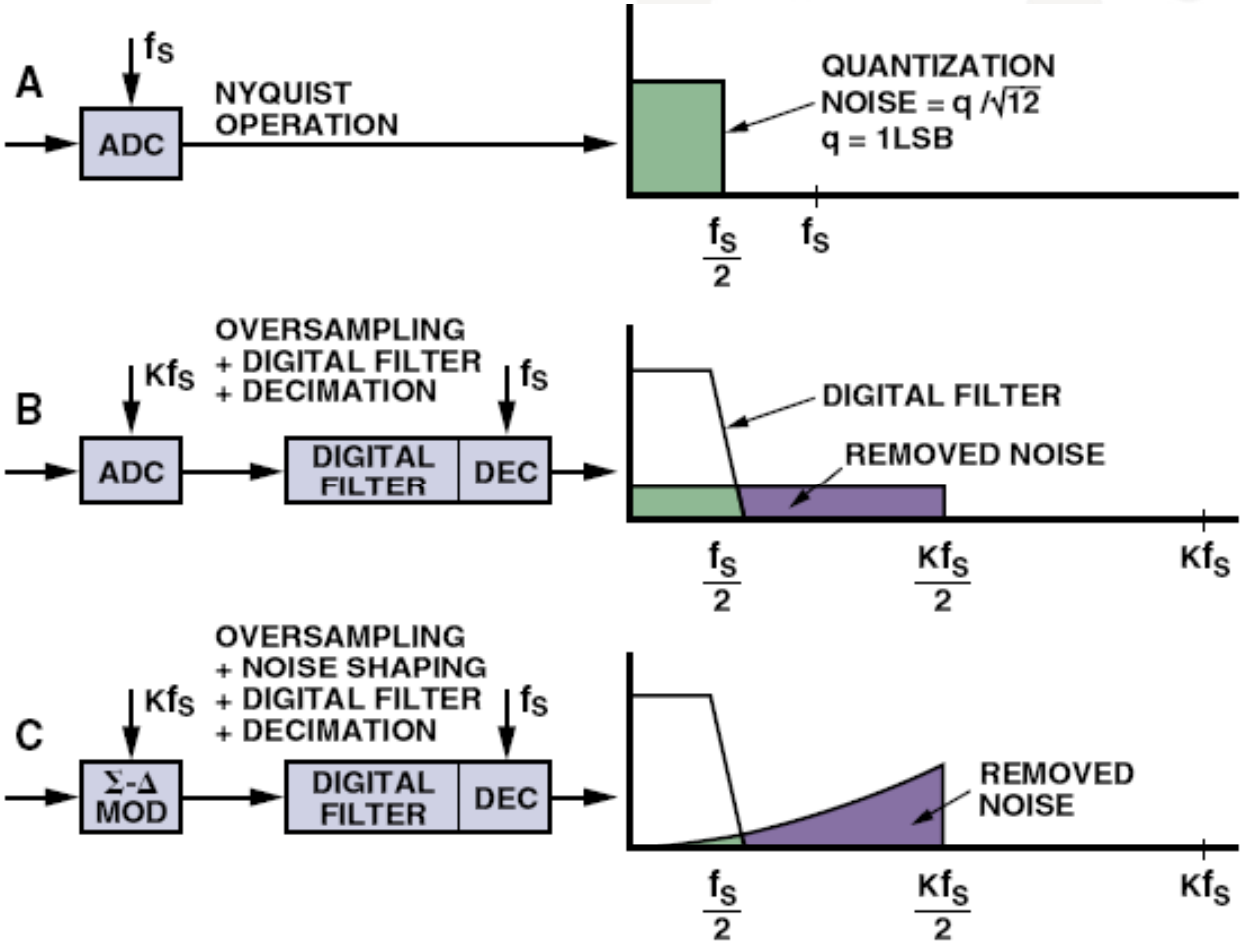
Today:

14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
2nd order sigma delta design example
16.1 Basic Phase Locked Loop Architecture



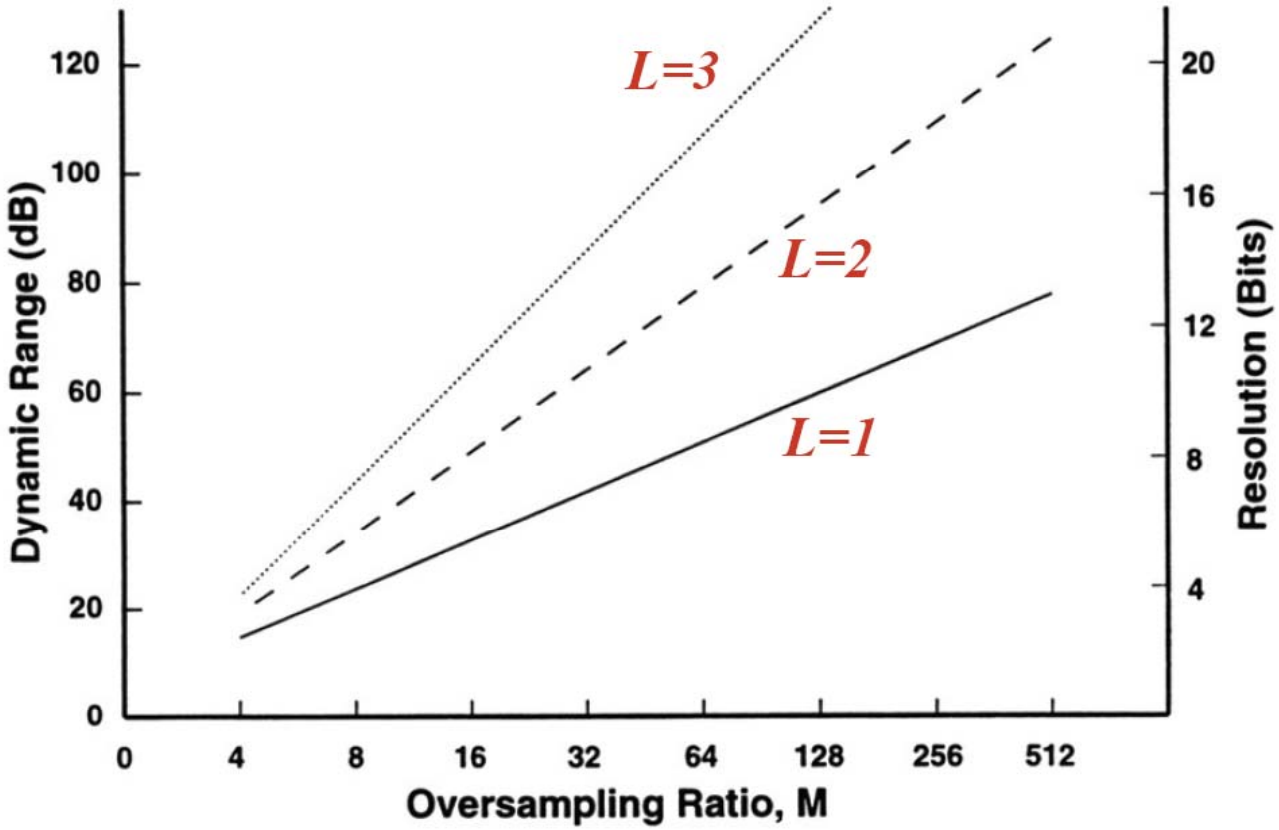
he relative phase angles of the input signal and the output of the oscillator.
Fig. 16.3

Nyquist Sampling, Oversampling, Noise Shaping



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- $fs > 2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

OSR, modulator order and Dynamic Range



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- Oversampling and noise shaping

14.2 Oversampling with noise shaping

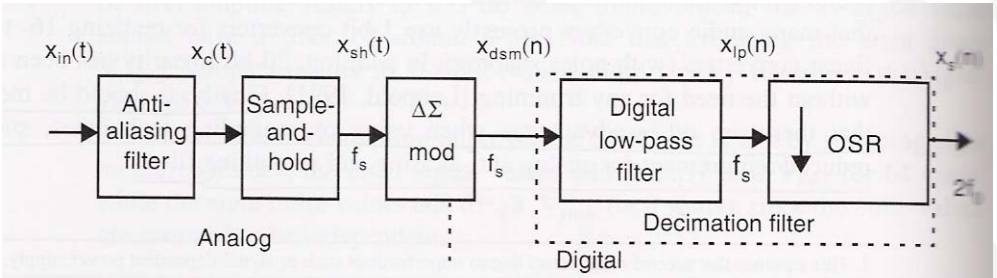
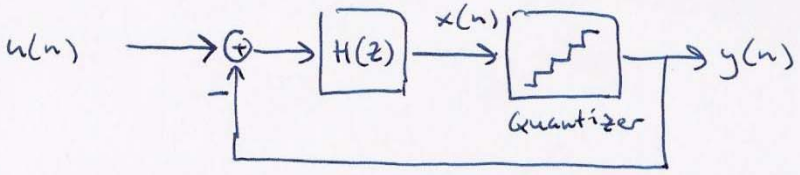


Fig. 14.5 Block diagram of an oversampling A/D converter.

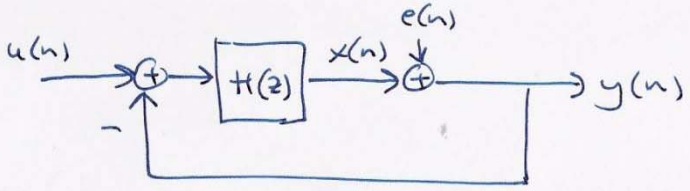
- The anti aliasing filter bandlimits the input signals less than $f_s/2$.
- The continous time signal $x_c(t)$ is sampled by a S/H (not necessary with separate S/H in Switched Capacitor impl.)
- The Delta Sigma modulator converts the analog signal to a noise shaped low resolution digital signal
- The decimator converts the oversampled low resolution digital signal into a high resolution digital signal at a lower sampling rate usually equal to twice the desired bandwidth of the desired input signal (conceptually a low-pass filter followed by a downsampler).

Noise shaped Delta Sigma Modulator

General $\Delta\Sigma$ modulator

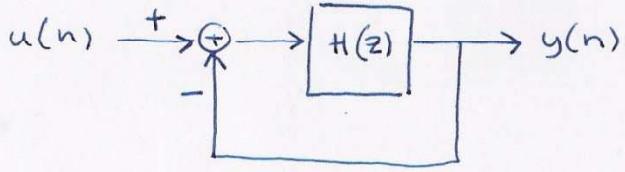


Linear model

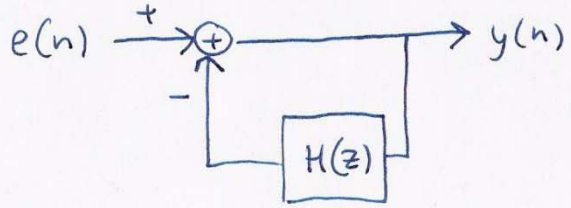


The linear model can be treated as having two independent inputs (which is an approximation).

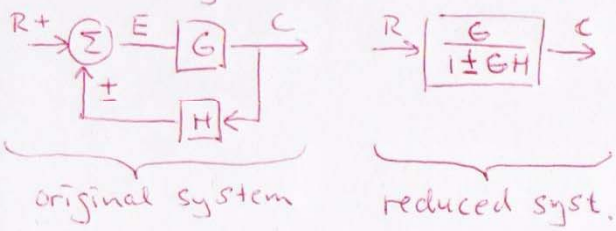
Signal :



Noise :



BLOCK DIAGRAM ALGEBRA, Cathey & Nasar p. 292; eliminating a feedback loop:



Signal transfer function, $S_{TF}(z)$:

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}$$

Noise transfer function, $N_{TF}(z)$:

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

The output is the combination of the input and noise : $Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z)$

Generator armature. So long as the generator is operated open-circuit, $E_G = v_T$, and the transfer function between ϕ_G and v_T is simply a constant:

$$\frac{V_T(s)}{\Phi_G(s)} = K_G \tag{6}$$

Voltage divider. If the series combination of the exciter field resistance and the reference-command potentiometer resistance is much larger than R_2, then voltage division is valid and the transfer function relating v_T to v_{fb} is

$$\frac{V_{fb}(s)}{V_T(s)} = \frac{R_2}{R_1 + R_2} \tag{7}$$

The above transfer functions and summer signal have been used to form the (mathematical) block diagram of Fig. 16-2.

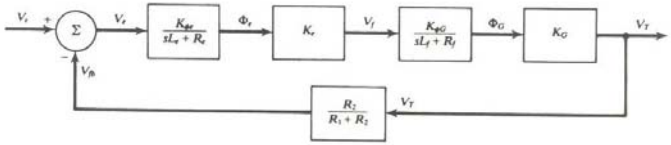


Fig. 16-2

16.2 BLOCK DIAGRAM ALGEBRA

For a control system of any complexity, the block diagram will contain many transfer functions in series and parallel arrangements. It is expedient to reduce the block diagram to more tractable form by applying the rules of *block diagram algebra*, as summarized in Table 16-1.

Table 16-1

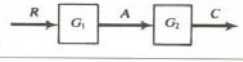
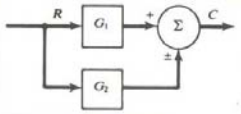
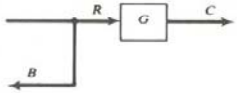
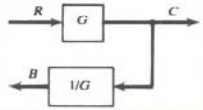
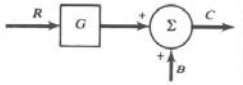
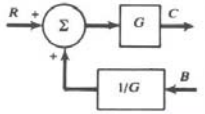
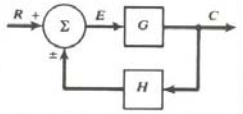
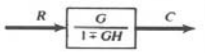
Rule	Original System	Reduced System
1. Cascaded blocks		
2. Parallel paths		
3. Moving a pickoff point		

Table 16-1 (*cont.*)

Rule	Original System	Reduced System
4. Moving a summer		
5. Eliminating a feedback loop		

The original system of Rule 5 exhibits the *canonical form* into which any control system with feedback can be transformed.

Example 16.2 Reduce the block diagram of Fig. 16-3(*a*) to a single block.

Move the pickup point for feedback signal $W(s)$ from the left to the right of block $C(s)$, using Rule 3. The result is shown in Fig. 16-3(*b*).

Combine cascaded (series-connected) blocks in the forward and feedback paths by Rule 1, giving the reduced block diagram of Fig. 16-3(*c*).

Finally, the simple negative feedback loop is eliminated by Rule 5, to yield the diagram of Fig. 16-3(*d*).

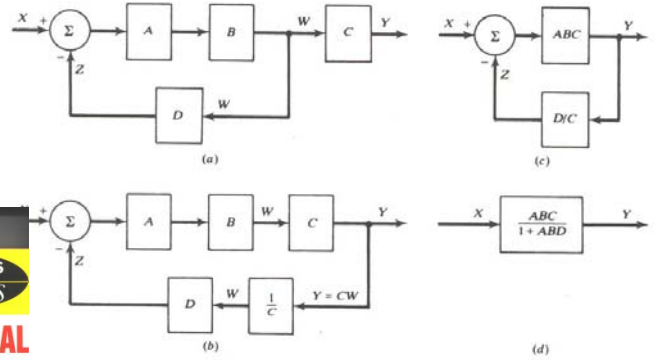
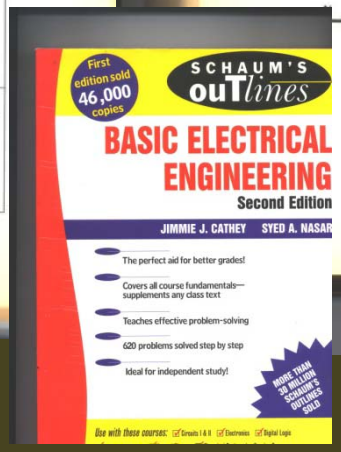


Fig. 16-3



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First-Order Noise Shaping (Figures from Schreier & Temes '05)

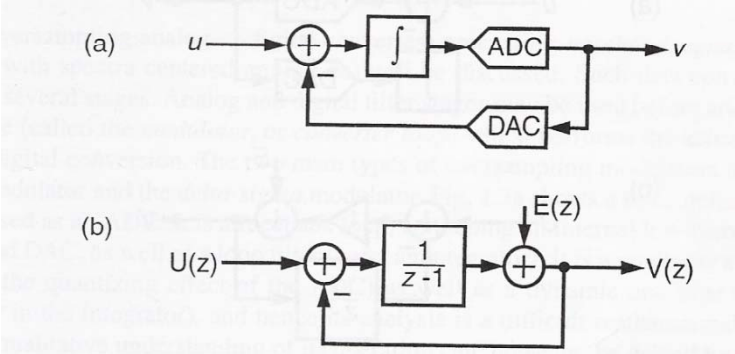

Figure 1.4: (a) A delta-sigma modulator used as an ADC and (b) its linear z-domain model.

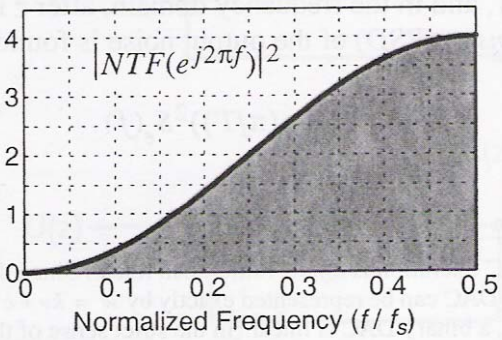

Figure 1.5: Noise-shaping function for the $\Delta\Sigma$ modulator shown in Fig. 1.4.

- $S_{TF}(z)$ = [H(z)/1+H(z)] (eq. 14.15) $N_{TF}(z)$ = [1/1+H(z)]
- Y(z) = $S_{TF}(z)$ U(z) + $N_{TF}(z)$ E(z)
- H(z) = 1/z-1 (discrete time integrator) gives 1st order noise shaping
- $S_{TF}(z)$ = [H(z)/1+H(z)] = 1/(z-1)/[1+1/(z-1)] = z^{-1}
- $N_{TF}(z)$ = [1/1+H(z)] = 1/[1+1/(z-1)] = (1 – z^{-1})
- The signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator (i.e. a high-pass filter)

14.2 Oversampling with noise shaping

$$N_{TF}(f) = 1 - e^{-j2\pi f/f_s} = \left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right) \cdot e^{-j\pi f/f_s} = \frac{\left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right) \cdot 2j \cdot e^{-j\pi f/f_s}}{2j}$$

$$= \sin\left(\frac{\pi f}{f_s}\right) \cdot 2j \cdot e^{-j\pi f/f_s}$$

$$|N_{TF}(f)| = 2 \sin\left(\frac{\pi f}{f_s}\right) \quad (\text{"high-pass"})$$

$$\cos z = \frac{e^{jz} + e^{-jz}}{2}$$

$$\sin z = \frac{e^{jz} - e^{-jz}}{2j}$$

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Quantization noise power over the frequency band 0 to f_0 is now given by

$$P_e = \int_{-f_0}^{f_0} S^2_e(f) \cdot |N_{TF}|^2 df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right) \frac{1}{f_s} \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad (14.23)$$

Making the approximation that $f_0 << f_s$ $(OSR >> 1)$ so that $\sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s}$:

$$P_e \approx \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2 \pi^2}{36}\left(\frac{1}{OSR}\right)^3 \quad , \quad OSR = \frac{f_s}{2f_0}$$

It is assumed that the maximum signal power is the same as obtained before, in equation 14.11 $(P_s = \Delta^2 2^{2N}/8)$, making maximum SNR:

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} \cdot 2^{2N}\right) + 10 \log\left[\frac{3}{\pi^2}(OSR)^3\right], \text{ or:}$$

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30 \log(OSR)$$

Doubling the OSR gives an SNR improvement for a 1st order modulator of 9 dB/octave or, equiv. 1.5 bits/octave.

Quantization noise power for linearized model of a general ΔΣ modulator

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\,|N_{TF}(f)|^2\,df = \int_{-f_0}^{f_0} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \quad (14.23)$$

Using the approximation that $f_0 << f_s$ (i.e. $OSR >> 1$) so that we may approximate $\sin\frac{\pi f}{f_s}$ to be $\frac{\pi f}{f_s}$:

$$P_e = \int_{-f_0}^{f_0} \frac{\Delta^2}{12}\frac{1}{f_s}\left[2\frac{\pi f}{f_s}\right]^2 df = \int_{-f_0}^{f_0} \frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2}\cdot f^2\,df$$

Letting $K = \frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2}$

$$P_e = K\int_{-f_0}^{f_0} f^2\,df = \frac{K}{3}\left(f_0^3 - (-f_0)^3\right) = \frac{K}{3}\cdot 2f_0^3$$

$$= \frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2\cdot 3}\cdot f_0^3 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\cdot\frac{2\cdot 2\cdot 2}{f_s^3}\cdot f_0^3 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{2f_0}{f_s}\right)^3$$

Using $OSR = \frac{f_s}{2f_0} \Leftrightarrow \frac{2f_0}{f_s} = \frac{1}{OSR}$: $P_e = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \quad (14.24)$

Second-order noise shaping

Fig. 14.10 — 2nd order modulator

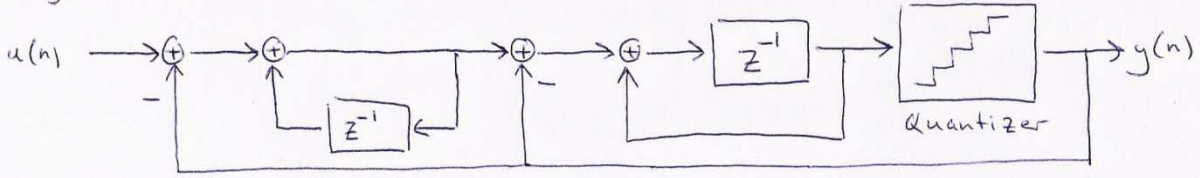
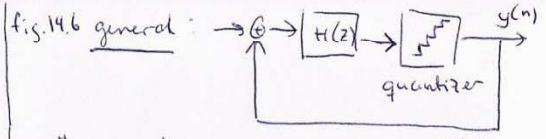
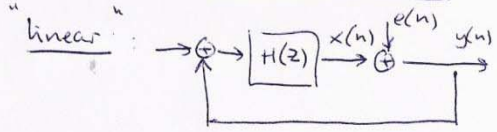


fig. 14.6 general:



"linear":



The above modulator realizes 2nd order noise shaping.

The signal transfer function is given by

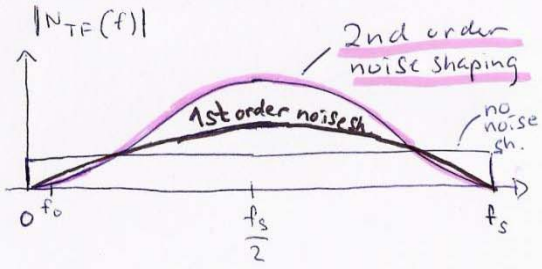
$$S_{TF}(f) = z^{-1}$$

The noise transfer function is given by

$$N_{TF}(f) = (1 - z^{-1})^2$$

Magnitude: $|N_{TF}(f)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2$

fig. 14.11:



The quantization noise power over the frequency band of interest:

$$P_e \cong \frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5$$

Max SNR:

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} 2^{2N}\right) + 10 \log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

or:

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \quad (14.32)$$

Doubling the OSR improves the SNR for a 2nd order mod. by 15 dB.

Ex. 14.5 p. 545:
1-bit A/D, 6-bit SNR. f_0 = 25 kHz
96 dB SNR is the goal.
Sample rated needed?
- oversampling: 54 THz
- 1st order n.s.: 75 MHz
- 2nd order n.s.: 5.8 MHz

14.3 System Architectures (A/D)

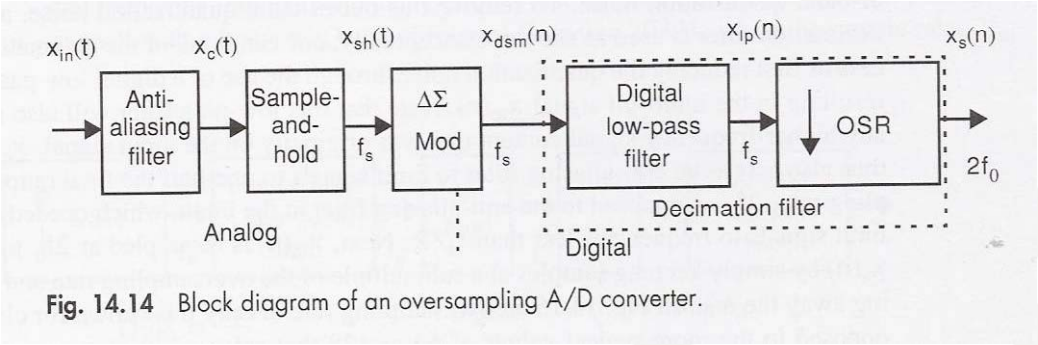
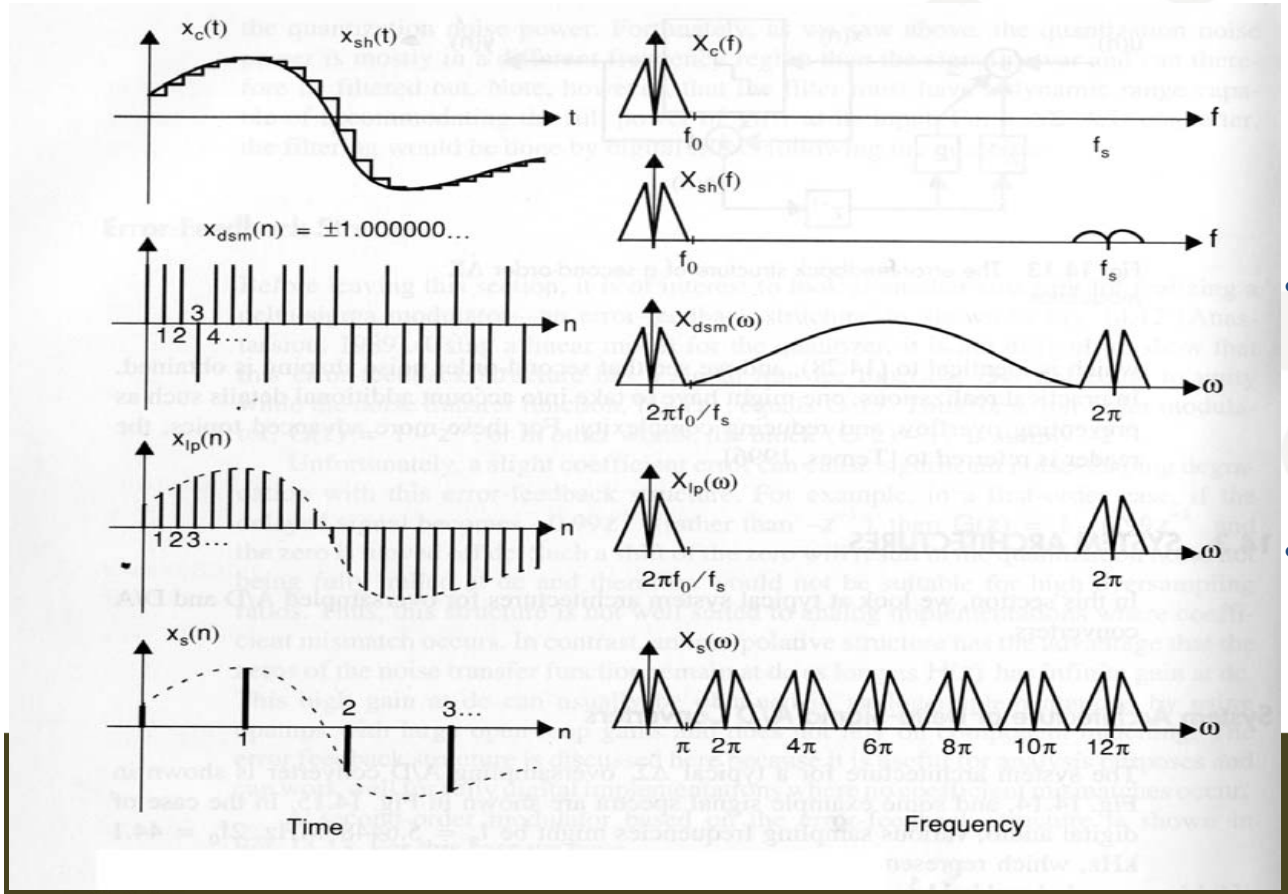
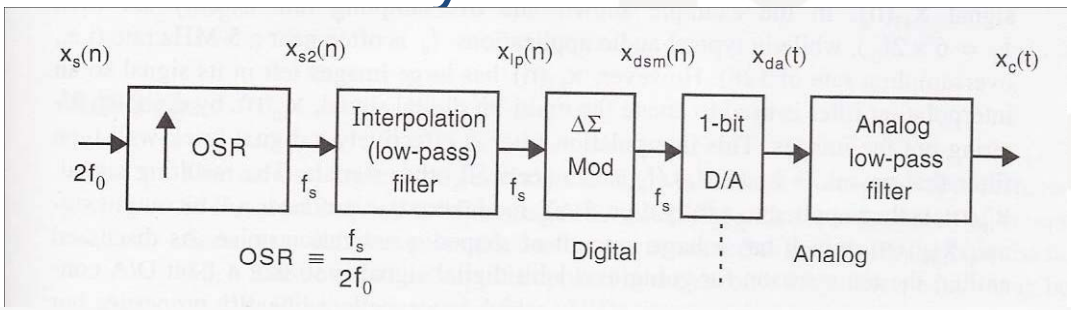


Fig. 14.14 Block diagram of an oversampling A/D converter.



- $X_c(t)$ is sampled and held, resulting in $x_{sh}(t)$.
- $x_{sh}(t)$ is applied to an A/D Sigma Delta modulator which has a 1-bit output, $x_{dsm}(n)$. The 1-bit signal is assumed to be linearly related to the input $X_c(t)$ (accurate to many orders of resolution), although it includes a large amount of out-of-band quantization noise (seen to the right).
- A digital LP filter removes any high frequency content, including out of band quantization noise, resulting in $X_{lp}(n)$
- Next, $X_{lp}(n)$ is resampled at $2f_0$ to obtain $X_s(n)$ by keeping samples at a submultiple of the OSR

System Architectures (D/A)



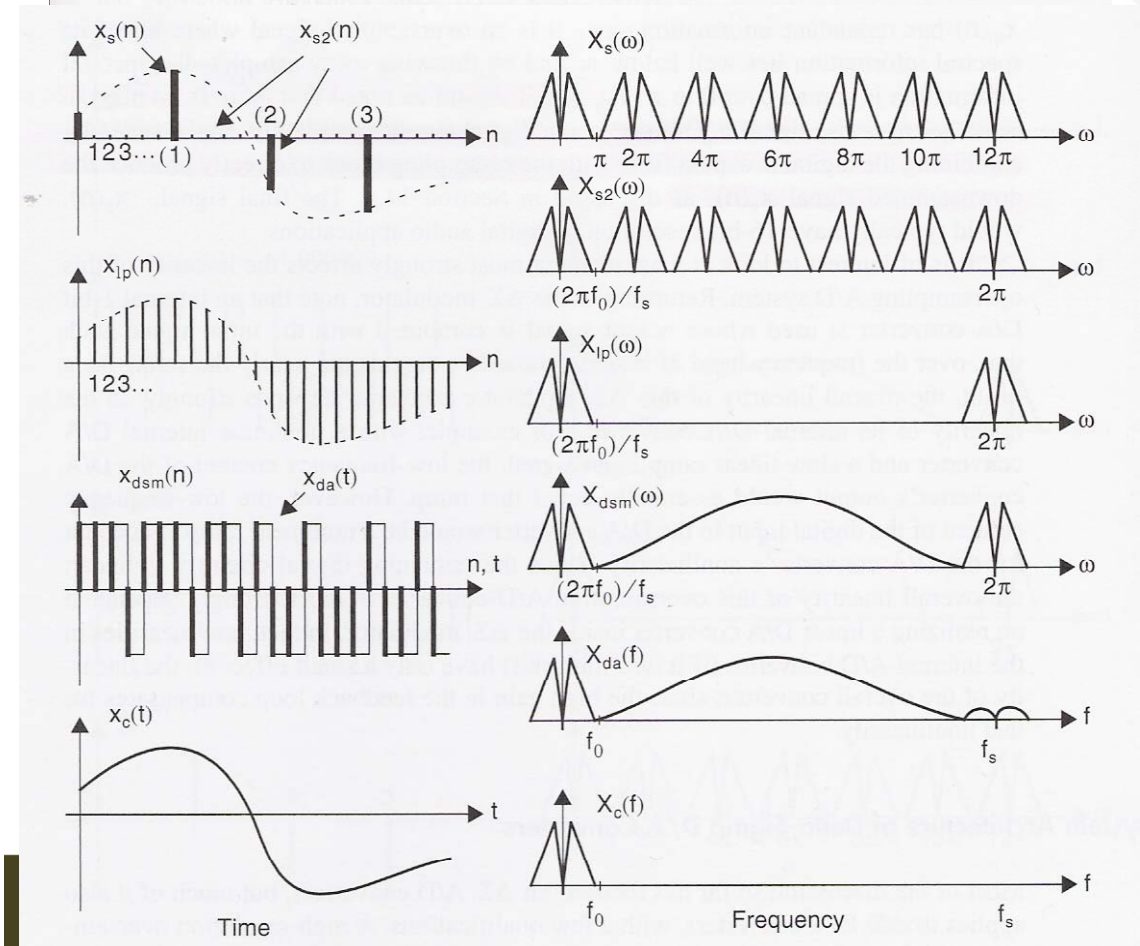


Fig. 14.17 Signals and spectra in an oversampling D/A converter.

- The digital input, $X_s(n)$ is a multi-bit signal and has an equivalent sample rate of $2f_0$, where f_0 ,is slightly higher than the highest input signal frequency.
- Since $X_s(n)$ is just a series of numbers the frequency spectrum has normalized the sample rate to 2π.
- The signal is upsampled to an equivalent higher sampling rate, f_s, resulting in the signal $x_{s2}(n)$
- $x_{s2}(n)$ has images left that are filtered out by the interpolation filter (brick-wall type) to create the multi-bit signal $X_{lp}(n)$, by digitally filtering out the images.
- $X_{lp}(n)$ is applied to a fully digital sigma delta modulator producing the 1-bit signal, $X_{dsm}(n)$, containing shaped quantization noise.
- $X_{dsm}(n)$ is fed to a 1-bit D/A producing $X_{da}(t)$, which has excellent linearity properties but still quantization noise.
- The desired signal, $X_c(t)$ can be obtained by using an analog filter to filter out the out-of-band quantization noise. (filter should be at least one order higher than the modulator.)

14.4 Digital decimation filters

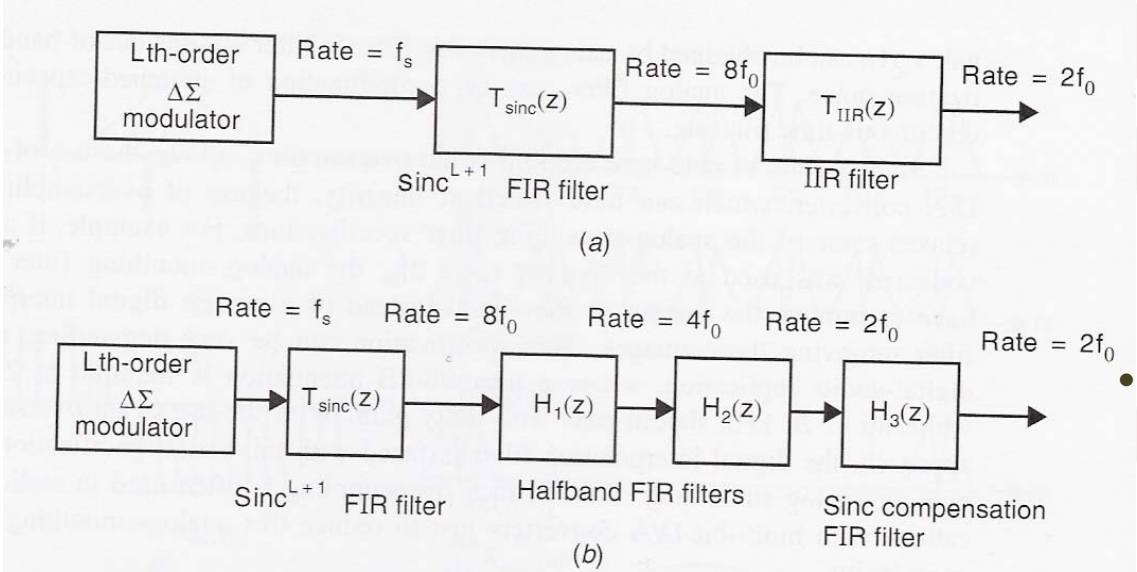


Fig. 14.18 Multi-stage decimation filters: (*a*) sinc followed by an IIR filter; (*b*) sinc followed by halfband filters.

- Many techniques
- a) FIR filter removes much of the quantization noise, so that the output can be downsampled by a 2nd stage filter which may be either IIR type (as in a), uppermost) or a cascade of FIR filters (as in b), below)
- In b) a few halfband FIR filters in combination with a sinc compensation FIR-filter are used.

  In some applications, these halfband and sinc compensation filters can be realized using no general multi-bit multipliers [Saramaki, 1990]

14.5 Higher-Order Modulators – Interpolative structure

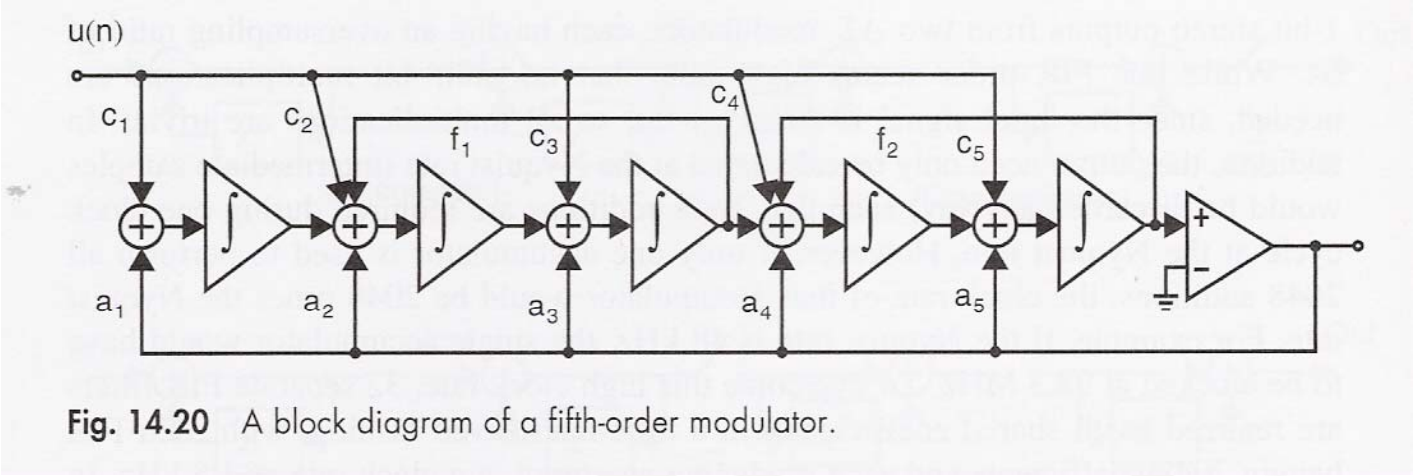


Fig. 14.20 A block diagram of a fifth-order modulator.

- Lth order noise shaping modulators improve SNR by 6L+3dB/octave.
- Typically a single high-order structure with feedback from the quantized signal.
- In figure 14.20 a single-bit D/A is used for feedback, providing excellent linearity.
- Unfortunately, modulators of order two or more can go unstable, especially when large input signals are present (and may not return to stability) Guaranteed stability for an interpolative modulator is nontrivial.

Multi-Stage Noise Shaping architecture ("MASH")

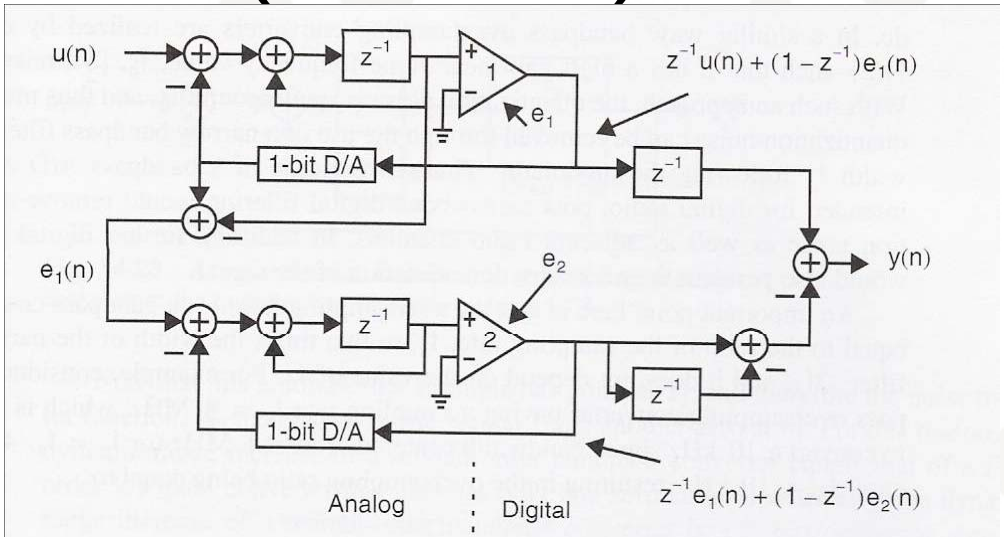


Fig. 14.21 A second-order MASH modulator using two first-order modulators. Note that the output, y(n), is a four-level signal.

- Overall higher order modulators are constructed using lower-order, more stable, ones → more stable overall system.
- Fig. 14.21: 2nd order using two first-order modulators.
- Higher order noise filtering can be achieved using lower-order modulators.
- Unfortunately sensitive to finite opamp gain and mismatch

14.7 Practical considerations

- Stability
- Linearity of two-level converters
- Idle tones
- Dithering
- Opamp gain

tor. For this case, the output sequence becomes

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, \ldots\} \quad (14.47)$$

The period of this output pattern is now 16 cycles long and has some power at $f_s/16$. With an oversampling ratio of eight (i.e., $f_0 = f_s/16$), the post low-pass filter will not attenuate the signal power at $f_s/16$ since that frequency is just within the frequency band of interest. In other words, a dc level of 3/8 into this modulator will produce the correct dc output signal but

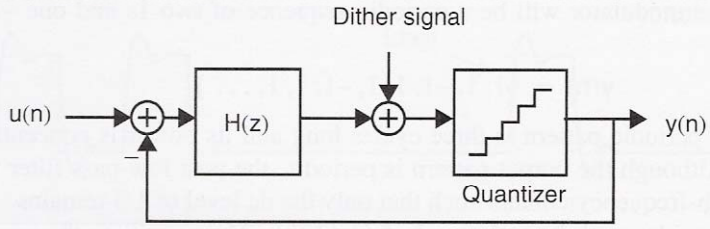


Fig. 14.26 Adding dithering to a delta-sigma modulator. Note that the dithered signal is also noise shaped.

Design example, 14b 2nd order Sigma-Delta mod

Second-Order Sigma Delta Modulator

Snorre Aunet
Email: sa@nvlsi.no
Nordic VLSI
Norway

May 4, 1994

BOSER AND WOOLEY: SIGMA-DELTA MODULATION ANALOG-TO-DIGITAL CONVERTERS

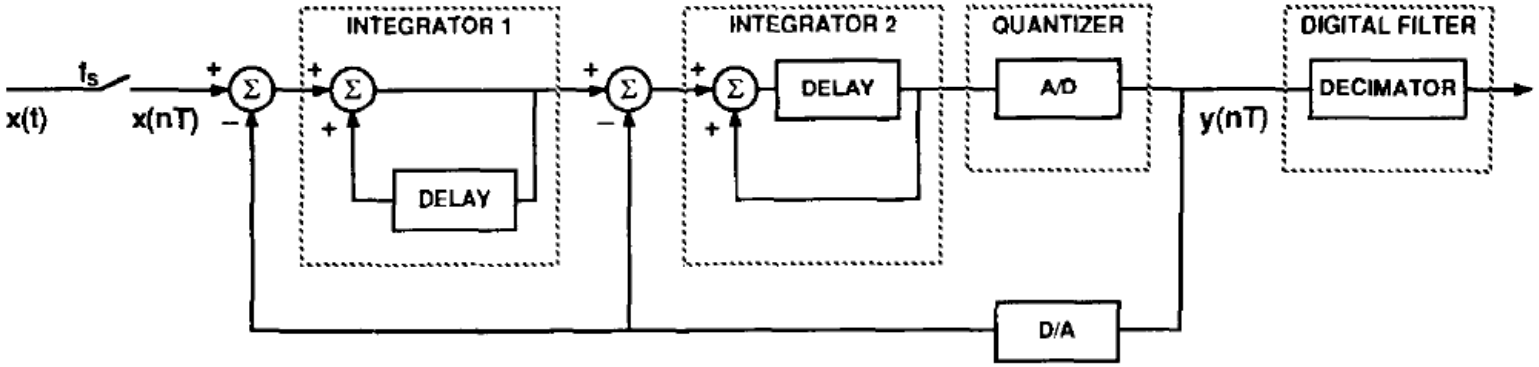


Fig. 1. Block diagram of second-order ΣΔ modulator with decimator.

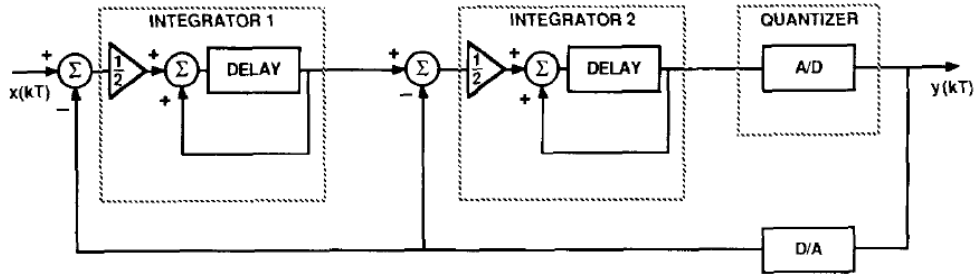


Fig. 2. Modified architecture of second-order ΣΔ modulator.

- 16 bit, 24 kHz , OSR as powers of two, and allowing for increased baseband noise due to nonidealities: OSR 512 was chosen

Design example, 14b 2nd order Sigma-Delta mod

- Among most relevant nonidealities:
- Finite DC gain
- Bandwidth,
- Slew rate
- Swing limitation
- Offset voltage
- Gain nonlinearity
- Flicker noise
- Sampling jitter
- Voltage dependent capacitors
- Switch on-resistance
- Offset voltage and settling time for comparators

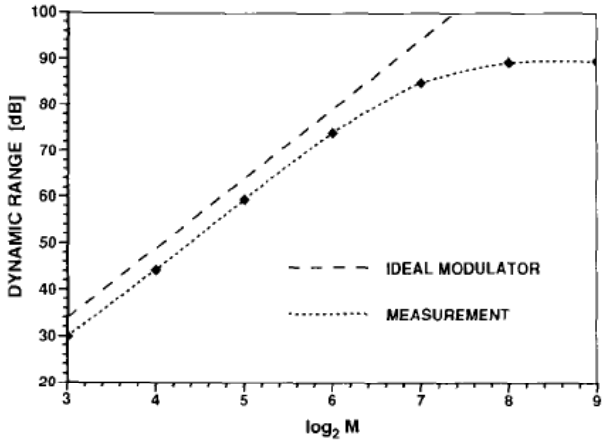
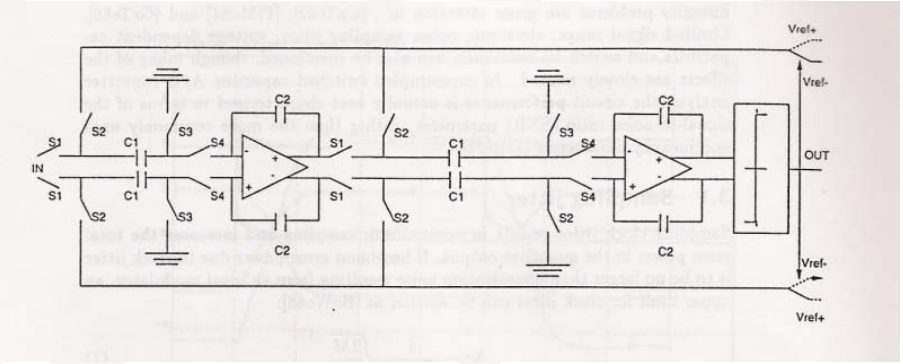


Fig. 15. Dynamic range as a function of the oversampling ratio for a sampling frequency of 4 MHz.



Design example, 14b 2nd order Sigma-Delta mod

Second-Order Sigma Delta Modulator

Snorre Aunet
Email: sa@nvlsi.no
Nordic VLSI
Norway

May 4, 1994

4.1 Specification of modulator functions

- SYSTEM
  - Technology: CMOS 0.8 micron
  - Power supply: VSS = -2.5 V, GND = 0 V, VDD = 2.5 V
  - Temperature: 0 to 70 degrees C
- OPERATIONAL AMPLIFIER
  - Gain: 1000 (60 dB)
  - Unity-Gain Bandwidth: 100 MHz
  - Phase Margin: 60°
  - Maximum capacitive load: several pF
  - Input voltage sving: 4 V
  - Diff. output voltage sving: $\geq 6V$
  - Slew rate: at least $300\frac{V}{\mu s}$
- SWITCH
  - $R_{on} < 440\Omega$
- CAPACITORS
  - Type:
  - C_1: 1 pF
  - C_2: 2 pF
- LATCH
  - D-type, able to settle within 20 ns.
- COMPARATOR
  - Hysteresis: < 0.5 V
  - Settling time: < 20 ns

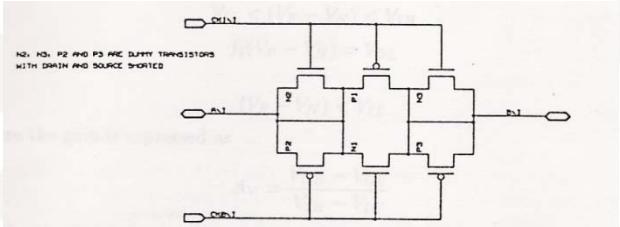


Figure 11: Dummy switch charge injection compensation [S-

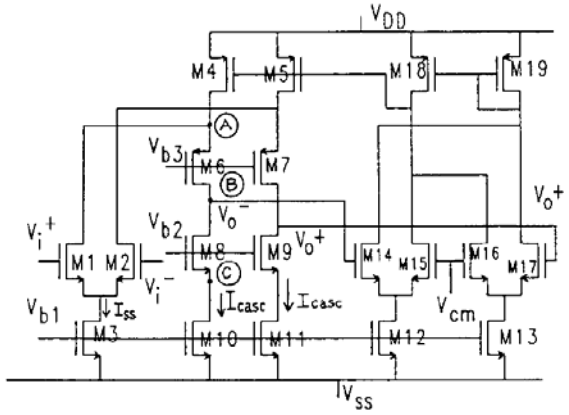


Fig. 1. Fully differential folded-cascode amplifier (after [4]).

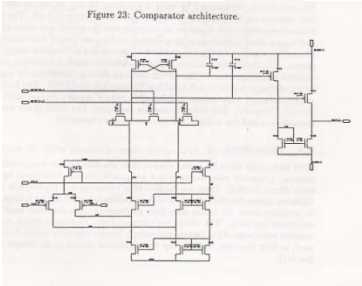


Figure 23: Comparator architecture.

- Noninverting parasitic insensitive integrator (fig 10.9) was used (fully differential implementation)

2nd order modulator; top level schematics

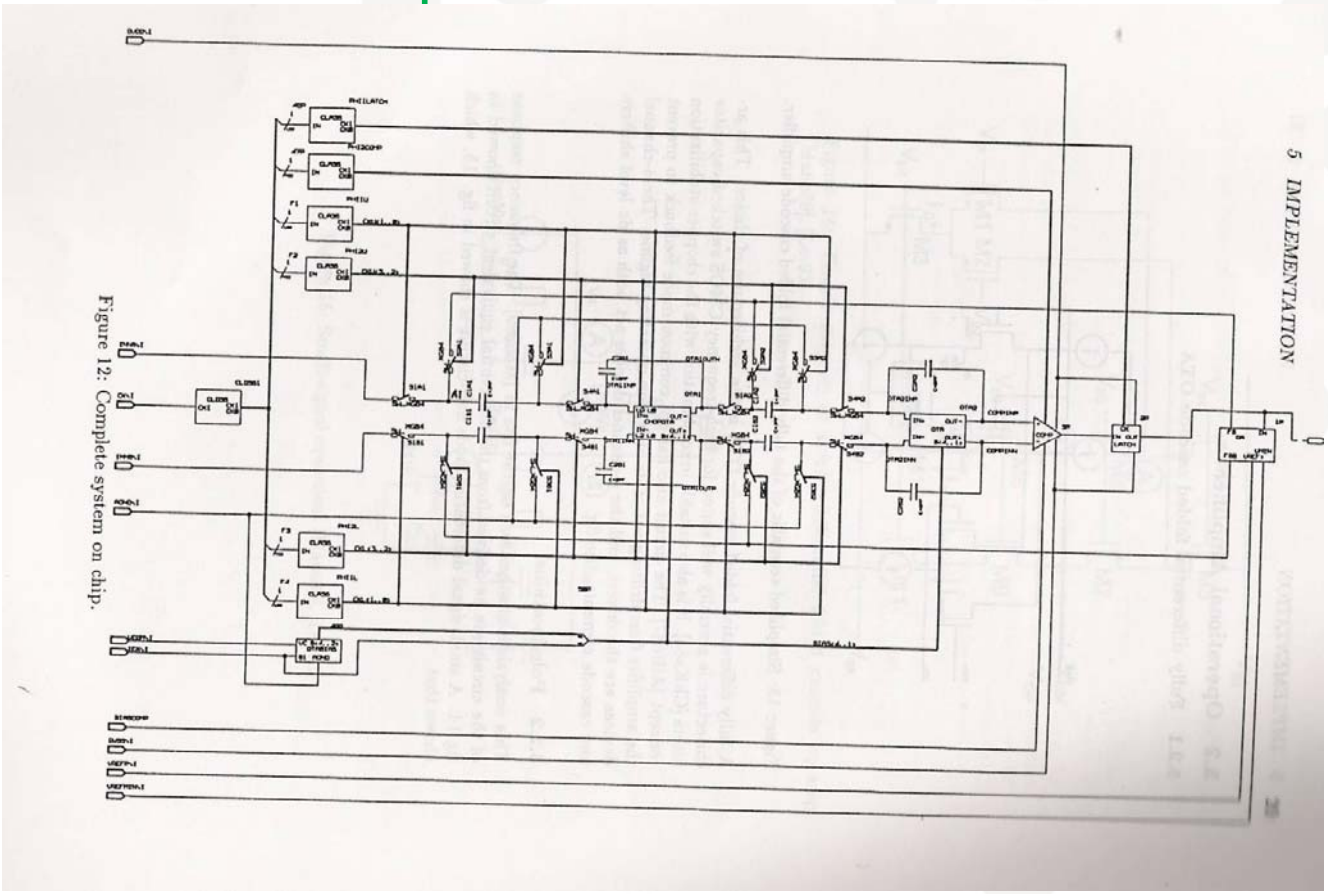


Figure 12: Complete system on chip.

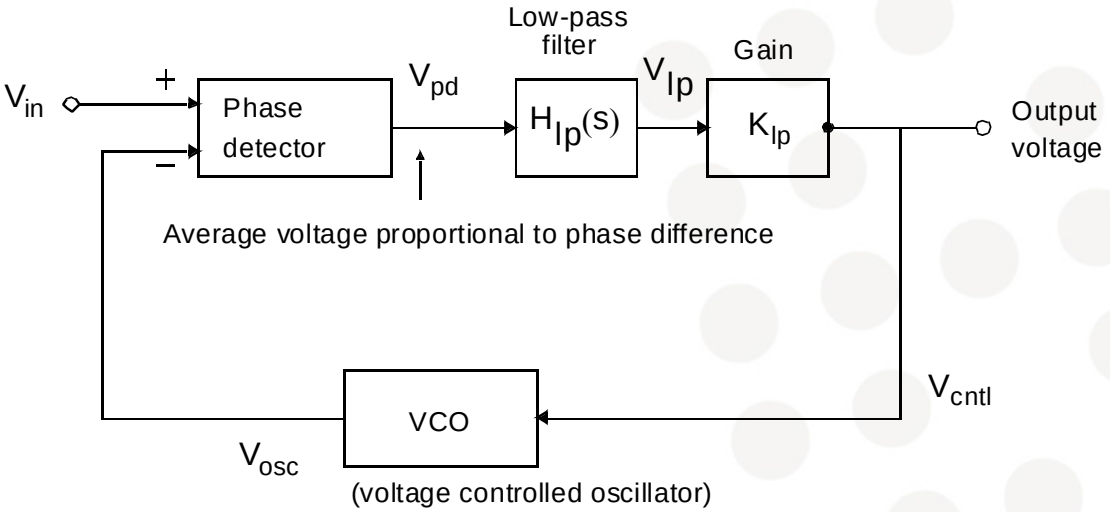
5 IMPLEMENTATION

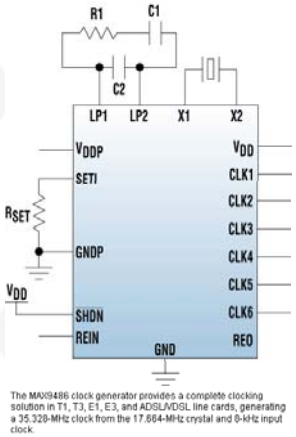
- Two-phase clock generator, switches, chopper stabilized OTA (1st int.), OTA (2nd int.- fully differential folded cascode), comparator, latch, two-level DAC. Biasing circuit. Functional after test.

Phase-locked loops (chapter 16)

- **Phase-locked loop**
- From Wikipedia, the free encyclopedia
- A **phase-locked loop** or **phase lock loop** (PLL) is a control system that generates a signal that has a fixed relation to the phase of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A phase-locked loop is an example of a control system using negative feedback.
- Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a cycle per second up to many gigahertz.

Phase-locked loops (chapter 16)





The MAX9486 clock generator provides a complete clocking solution in T1, T3, E1, E3, and ADSL/VDSL line cards, generating a 35.328-MHz clock from the 17.664-MHz crystal and 8-kHz input clock.

- Clock multiplication:
  - The input signal is reference oscillator with fixed frequency
  - The PLL output is a signal with frequency N times the input frequency where N is an integer
- Data recovery and clock resynchronization:
  - The input signal is a digital signal containing data
  - The output is digital data at a certain clock rate
  - The system clock is recovered from the digital input signal
- Frequency synthesis (ex: to select channels in television or wireless communication systems):
  - The input signal is reference oscillator with fixed frequency
  - The PLL output is a signal with frequency N times the input frequency where N may be a fractional number
- FM demodulation:
  - The input is a FM signal (IF)
  - The output is the demodulated baseband signal

Phase-Locked Loop, typical architecture

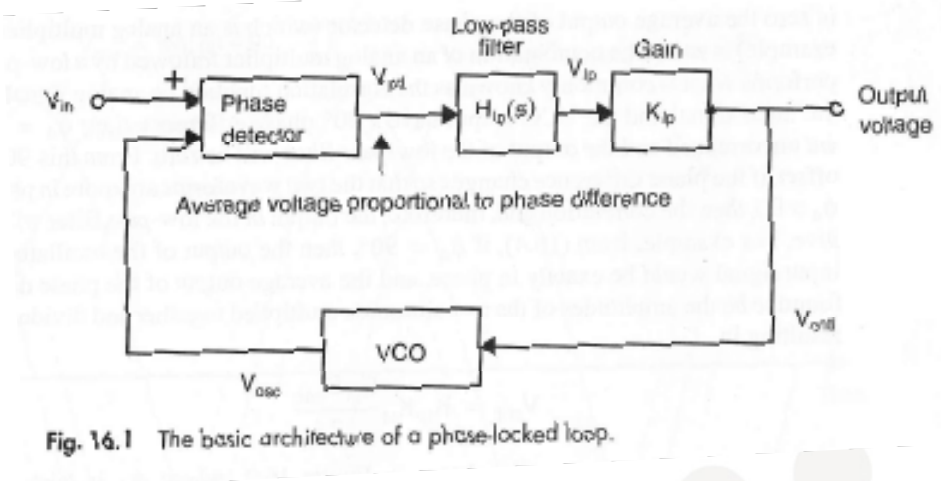
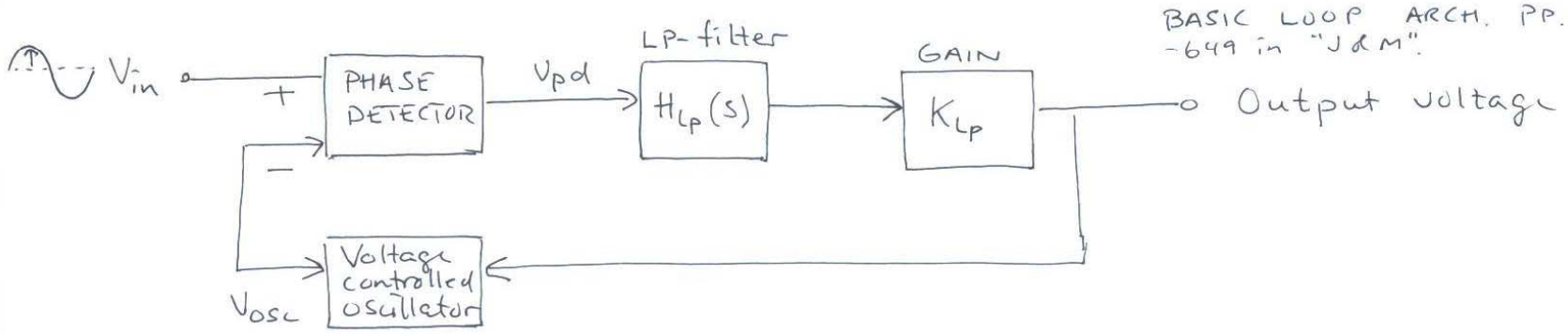


Fig. 16.1 The basic architecture of a phase-locked loop.

- The *phase detector* (”PD”) normally has an output voltage with an average value proportional to the phase difference between the input signal and the output of the VCO (”Voltage Controlled Oscillator”).
- The *low-pass filter* is used to extract the average value from the output of the PD.
- The average value is amplified by the *Gain* block and used to drive the VCO.
- The negative feedback of the loop results in the output of the VCO being synchronized with the input signal.

Phase-locked loop example (p. 649)



- The input signal, V_{in}, is assumed to be a sinusoid with known amplitude.
- The phase detector is realized as an analog multiplier with
  $V_{pd} = K_M \cdot V_{in} \cdot V_{osc}$ ∧ K_M: multiplication constant.
- $H_{LP}(s) = \dfrac{1 + s\tau_z}{1 + s\tau_p}$, $\tau_z << \tau_p$; first-order LEAD-LAG filter.
- $V_{in} = E_{in} \cdot \sin(\omega t)$
- $V_{osc} = E_{osc} \sin(\omega t - \Phi_d + 90^\circ) = E_{osc} \cos(\omega t - \Phi_d)$

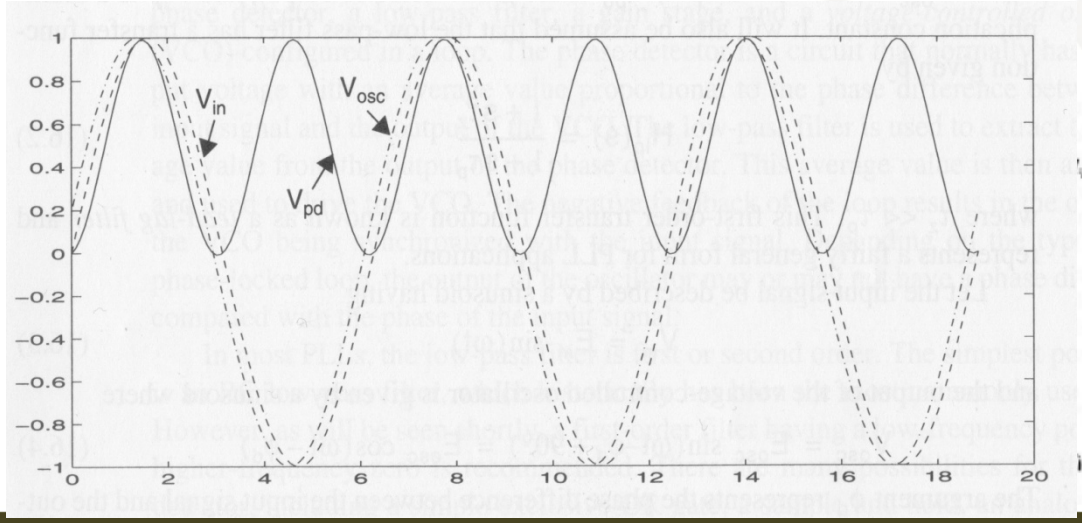
  Φ_d represents the phase difference between the input signal and the output of the oscillator. The reason for the 90° offset is that the PD (analog mult.) has a zero average output for a phase difference of zero.

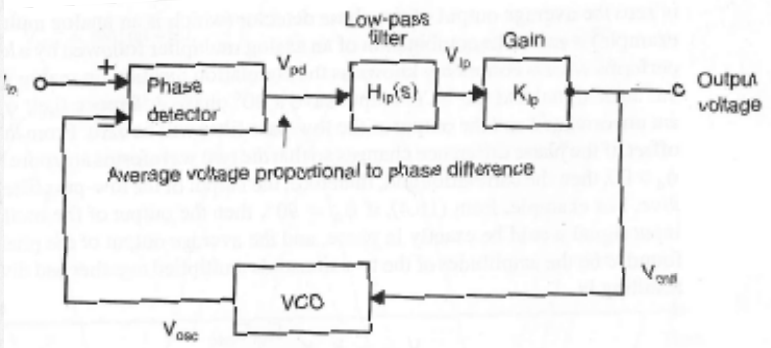
V_{in} and V_{osc} exactly in phase when Φ_d=90º

- $V_{in} = E_{in} \sin(\omega t)$,
- $Vosc = E_{osc} \sin(\omega t - \Phi_d + 90º) = E_{osc} \sin(\omega t - 90º + 90º) = E_{osc} \sin(\omega t)$
- The input signal and the output of the oscillator will be exactly in phase, and the output from the phase detector (" PD") is found to be the amplitudes of the two sinusoids multiplied together and divided by 2, resulting in

$V_{cntl} = K_{lp}K_M E_{in}E_{osc}/2$ (Eq. 16.5, p 650 in J&M)

Fig. 16.2, below, shows the output from the PD when V_{in} and V_{osc} are nearly in phase.



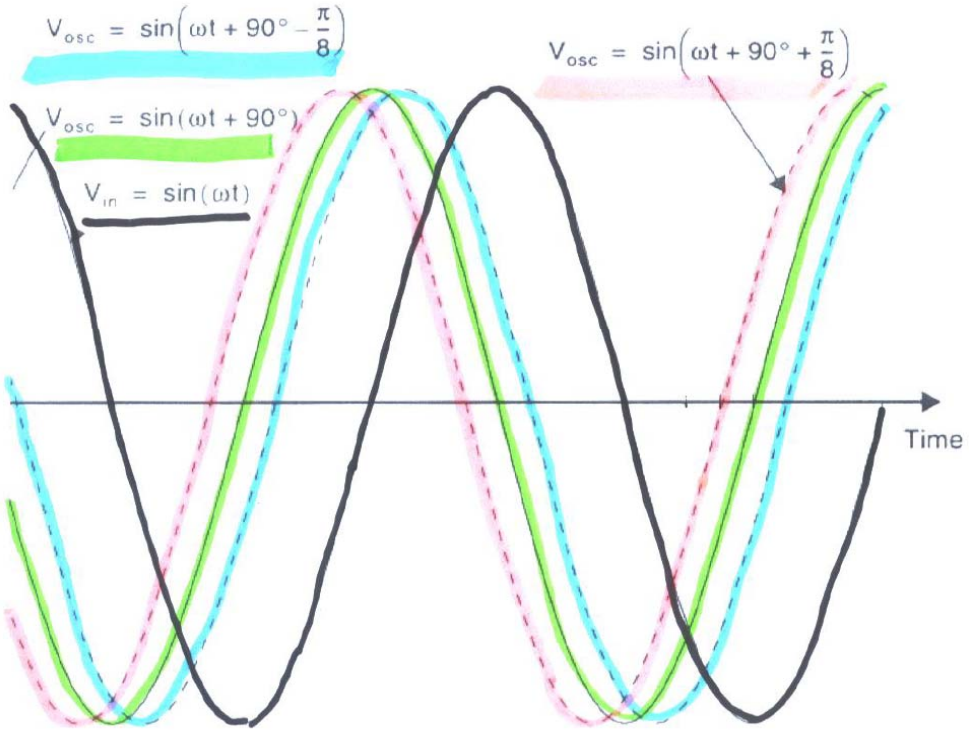


ig. 16.1 The basic architecture of a phase-locked loop.

Examples of different waveforms, as a function of different Φ_d,

(J&M p 650-651 ,fig. 16.3)

- $V_{osc} = E_{osc}\sin(\omega t - \Phi_d + 90°) = E_{osc}\cos(\omega t - \Phi_d)$ (16.4)
- $\Phi_d > 0$ corresponds to waveforms that are more in phase.
- When the input signal and VCO output have a 90º phase diff. ($\Phi_d = 0$), they are uncorrelated and the output of the LP-filter will be zero.)



he relative phase angles of the input signal and the output of the oscillator.

Fig. 16.3

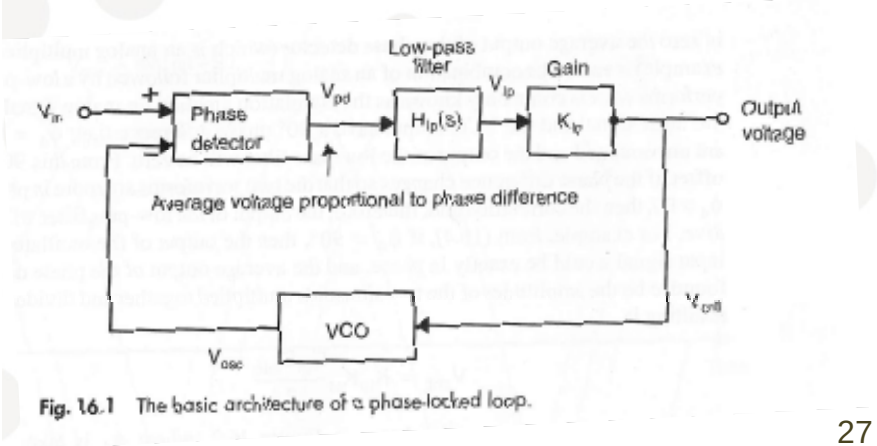


Fig. 16.1 The basic architecture of a phase-locked loop.

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Some relevant mathematical relationships from 16.1, pages 650-652 in "J&M"

- The output of the phase detector:
- $V_{pd} = K_M V_{in} V_{osc} = K_M E_{in} E_{osc} \sin(\omega t)\cos(\omega t - \Phi_d)$ (16.6)
- Using $\sin(A)\cos(B) = (1/2)[\sin(A+B)+\sin(A-B)]$ we have
  $V_{pd} = K_M V_{in} V_{osc}/2\ [\sin(\Phi_d)+2\sin(2\omega t - \Phi_d)]$ (16.8)
- The LP-filter removes the second term at twice the frequency of the input signal, so V_{cntl} is therefore given by
  $V_{cntl} = K_{lp} K_M (E_{in} E_{osc}/2) \sin(\Phi_d)$ (16.9)
- Since V_{cntl} is either a dc value or slowly varying, for small Φ_d the following approximation for (16.9) may be used:

  $V_{cntl} \approx K_{lp} K_M (E_{in} E_{osc}/2)\ \Phi_d = K_{lp} K_{pd}\ \Phi_d$ (16.10)

  Thus, the output of the LP-filter is approximately proportional to the phase difference between the output of the oscillator and the input signal, assuming the 90 ofset bias is ignored. The approximation is used in analyzing the PLL to obtain a linear model. The constant of proportionality is called K_{pd} and is given by

  $K_{pd} = K_M (E_{in} E_{osc}/2)$ (16.11)

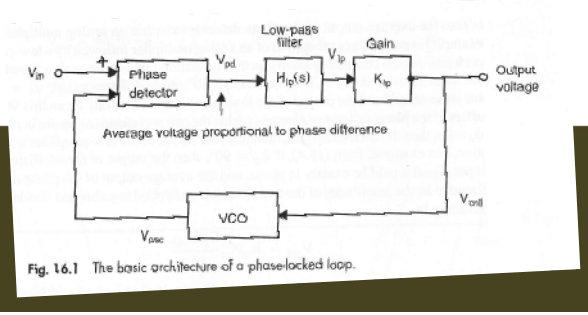
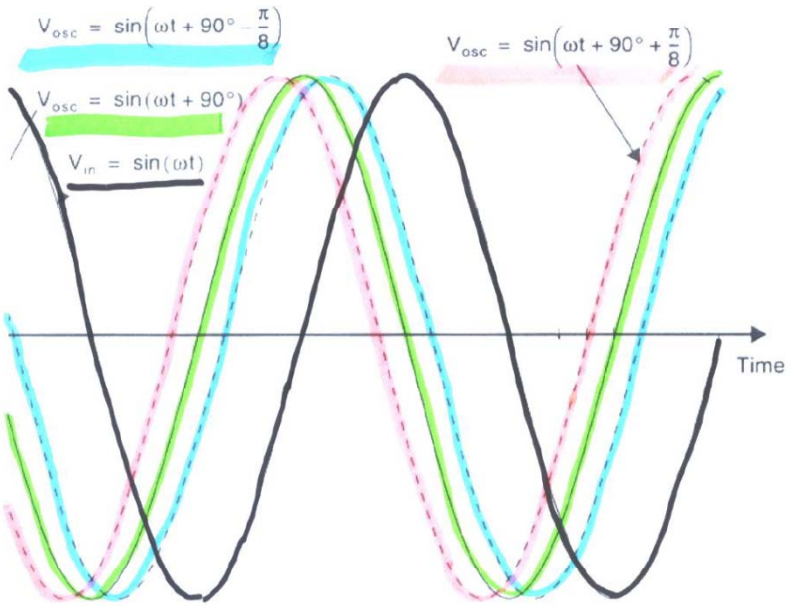


Fig. 16.1 The basic architecture of a phase-locked loop.

More on PLL operation (p. 652-653)

- Assume that the VCO has a free-running frequency ω_{fr} when it's input is zero, and that the input signal is initially equal to ω_{fr}, and the system has $\Phi_d = 0$ (in lock).
- NEXT, assume the input frequency slowly increases. Now, with $\Phi_d > 0$, the two waveforms will become more in phase (See fig. 16.3). After a short time the output of the LP-filter will go positive. Since the two waveforms are at slightly different frequencies, the output of the LP-filter will slowly increase. Since the VCO frequency is proportional to V_{cntl}, this increase will cause the VCO frequency to increase until it is the same of that of the input signal again, which will keep the two signals in synchronism (i.e. locked). (The opposite would occur for a decrease in the input signal frequency.)



he relative phase angles of the input signal and the output of the oscillator.

Fig. 16.3

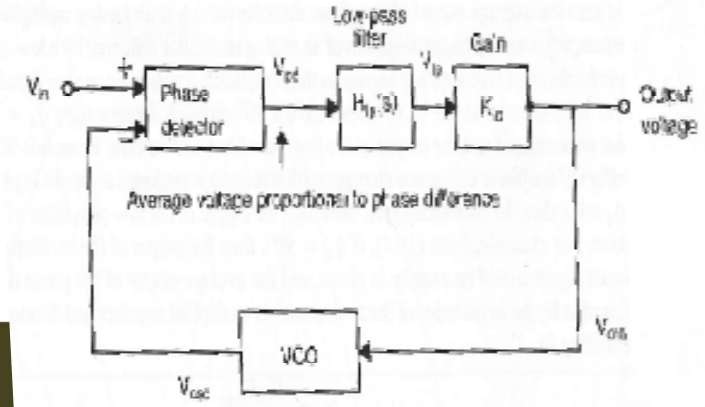


Fig. 16.1 The basic architecture of a phase-locked loop.

More on PLL operation (p. 652-653)

- At a new input frequency, ($\neq \omega_{fr}$) which does not equal the free-running frequency, we can find the new phase difference for the two locked signals by noting that the frequency of the oscillator's output signal is given by

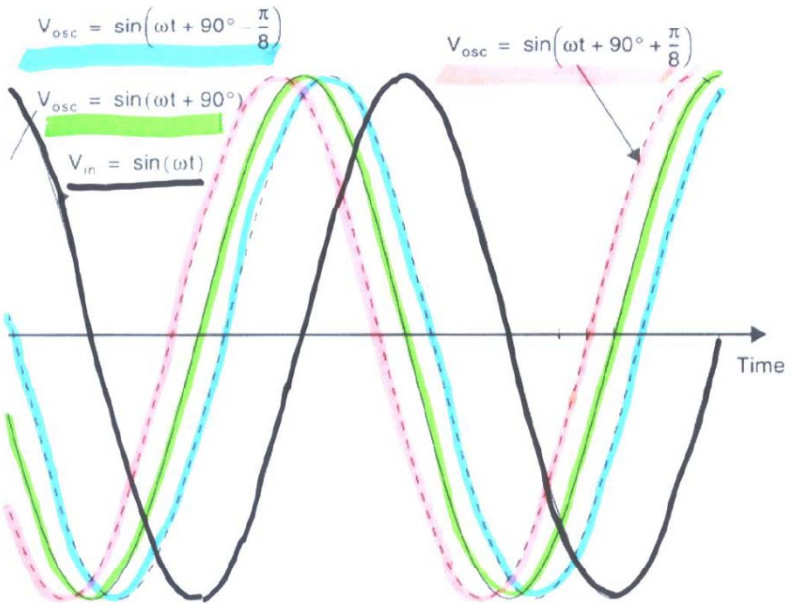
  $\omega_{osc} = K_{osc} V_{cntl} + \omega_{fr}$ (16.12).

  K_{osc} is a constant relating the change in frequency to control voltage ratio. The output voltage of the amplified LP-filter is now given by

  $V_{cntl} = (\omega_{in}\omega_{fr})/K_{osc}$ (16.13)

  where ω_{in} is the frequency of the input signal, which is equal to the frequency of the oscillator's output. From (16.10):

  $\Phi_d = V_{cntl}(K_{lp}K_{pd}) = (\omega_{in}-\omega_{fr})/K_{lp}K_{pd}K_{osc}$ (16.14)



he relative phase angles of the input signal and the output of the oscillator.

Fig. 16.3

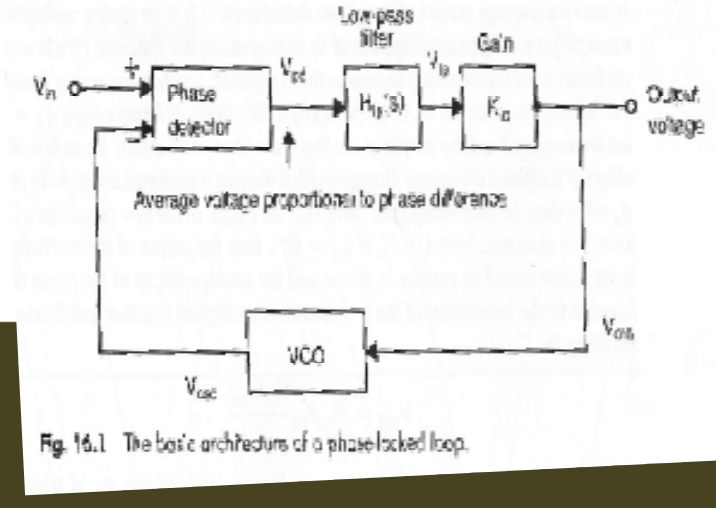
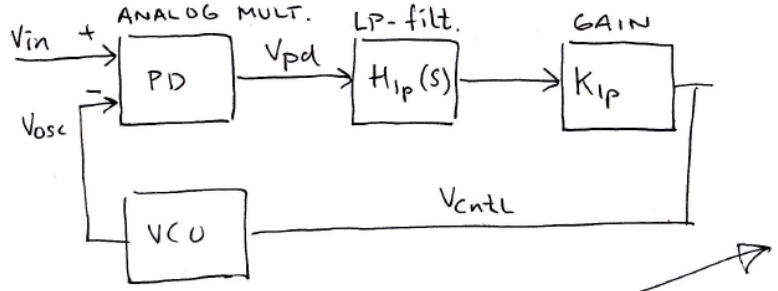


Fig. 16.1 The basic architecture of a phase-locked loop.

Ex. 16.2



Ex. 16.1 problem to the right

$$\Phi_d = \frac{V_{cntl}}{K_{lp} \cdot K_{pd}} = \frac{\omega_{in} - \omega_{fr}}{K_{lp} \cdot K_{pd} \cdot K_{osc}} \qquad (16.14)$$

K_{pd} and K_{osc} are needed in 16.14:

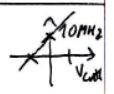
The phase detector realized as an analog multiplier has the following relationship:

$$V_{pd} = K_M \cdot V_{in} \cdot V_{osc} \qquad (16.1)$$

$$K_M = \frac{2.0\,V}{2.0\,V \cdot 2.0\,V} \left(= \frac{V_{pd}}{V_{in} \cdot V_{osc}} \right) \Leftrightarrow K_M = 0.5\,\frac{1}{V}$$

$$K_{pd} = K_M \cdot \frac{E_{in} \cdot E_{osc}}{2} = 0.5\,\frac{1}{V} \cdot \frac{0.75\,V \cdot 0.75\,V}{2} = 0.140625\,V$$

K_{osc} is a constant relating the change in frq. to control voltage ratio: $\frac{\Delta \omega_{osc}}{\Delta V_{cntl}} = \frac{2\pi \cdot 10^7\,rad/s}{1V}$



Using 16.14: $\Phi_d = \frac{2\pi\,(11\,MHz - 10\,MHz)}{K_{lp} \cdot K_{pd} \cdot K_{osc}} = 0.7112\,rad = 40.8°$

Counting in 90° offset: $90° - 40.8° = 49.2°$

EX. 16.1

Consider a PLL where the amplitudes of the inp. signal and the oscillator output are both at a 0.75 V peak. The analog mult. ~~which~~ would have 2V output when both inputs are DC values of 2V. The VCO free-running frequency is 10 MHz, and would decrease to zero for $V_{cntl} = -1V$. The gain block is unity, i.e. $K_{lp} = 1$. When in lock, what is the phase difference between the input and osc. output when $f_{in} = 11$ MHz? What is the phase difference when the input is 9 MHz? How does the phase difference change if $K_{lp} = ?$

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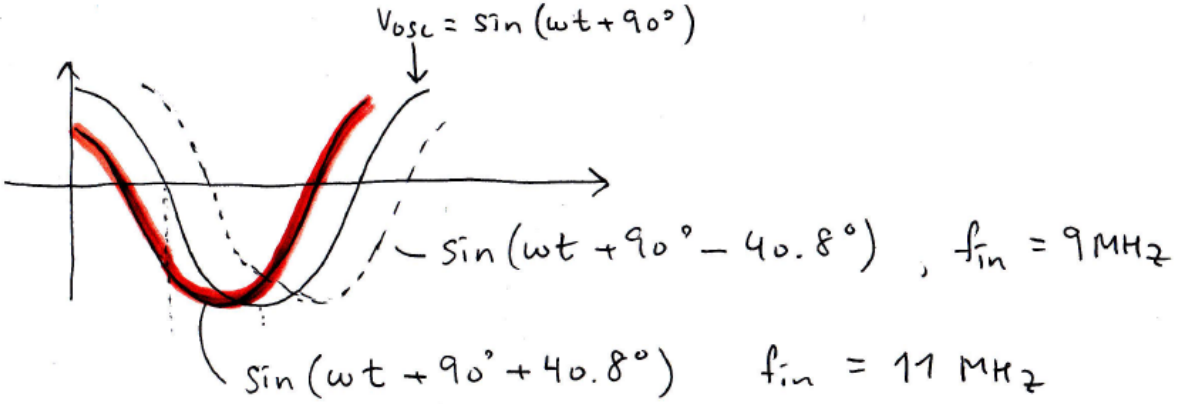
Ex. 16.1

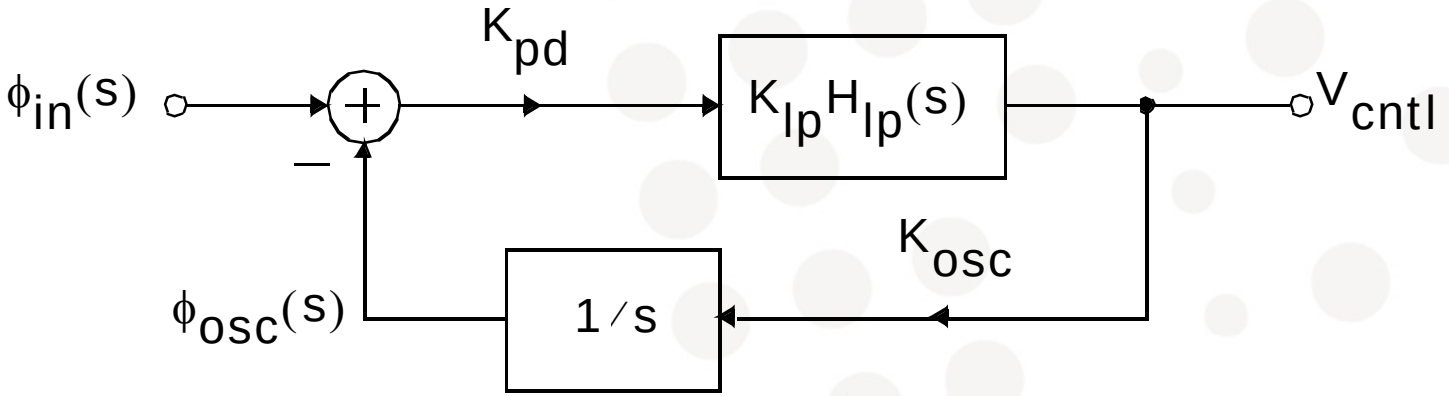


$f_{in} = 11$ MHz : The phase difference between the input and oscillator output becomes $90° - 40.8° = 49.2°$.

$f_{in} = 9$ MHz : $\phi_d = -40.8°$ $\Rightarrow$ phase difference of $90° - (-40.8°)$
$= 130.8°$

For $K_{LP} = 2$, half the phase difference results in the same VCO control voltage, V_{cntl}. So, for $\omega_{in} = 11$ MHz, $\phi_d = \frac{40.8°}{2}$ $= 20.4°$, and for 9 MHz, $\phi_d = -20.4°$. (Since $\phi_d = \frac{\omega_{in} - \omega_{fr}}{K_{LP} \cdot K_{pd} \cdot K_{OSC}}$)

Linear model of the PLL – when in lock



$$V_{cntl}(s) = K_{pd} K_{lp} H_{lp}(s) [\phi_{in}(s) - \phi_{osc}(s)]$$

$$\phi_{osc}(s) = \frac{K_{osc} V_{cntl}(s)}{s}$$

PLL transfer functions

- Combining equations from previous slide:

$$\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{sK_{pd}K_{lp}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a highpass response from input phase to the control voltage.
- Rewriting gives:

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{K_{pd}K_{lp}K_{osc}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a lowpass response from the input phase

Additional litterature

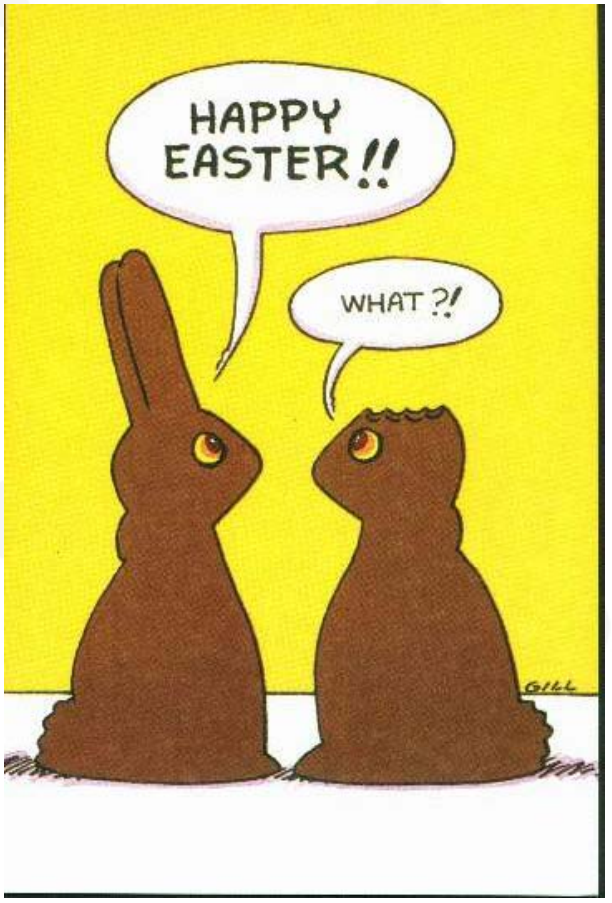
- Walt Kester: Which ADC Architecture is right for your application?, Analog Dialogue, Analog Devices, 2005.
- Behzad Razavi: ”Design of Analog CMOS Integrated Circuits”, McGraw-Hill, reprint 2009.
- Jimmy J. Cathey, Syed A. Nasar: Basic Electrical Engineering , Schaum’s Outlines, McGraw Hill 1997.
- Richard Schreier, Gabor C. Temes: Understanding Delta-Sigma Data Converters, IEEE Press / Wiley Interscience, 2005
- Tapio Saramaki et. Al: Multiplier-Free Decimator Algorithms for Super-Resolution Oversampled Converters, IEEE International Symposium on Circuits and Systems, 1990.
- Bernhard A. Boser, Bruce A. Wooley: The Design of Sigma-Delta Modulation Analog-to-Digital Converters, IEEE Journal of Solid-State Circuits, December 1988.
- Sudhir M. Mallya, Joseph H. Nevin: Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier , IEEE Journal of Solid-State Circuits, December 1989.
- http://www.wikipedia.org (on PLLs)
- Snorre Aunet: Second-Order Sigma Delta Modulator, Nordic VLSI, May 4, 1994.

Next Time, 13/4-10:

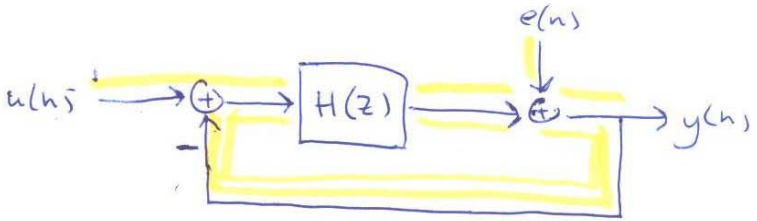
- More from Chapter 16; PLLs
- About report writing

23.03.2010	SA	Lille Aud.	Chapter 14; Oversampling Converters	preliminary...Slides Slides, two per page
30.03.2010				No teaching in week 13.
06.04.2010				No teaching in week 14, due to Easter holidays.

13.04.2010	SA	Lille Aud.	chapter 16; PLLs	Later... Slides. Slides, two per page.

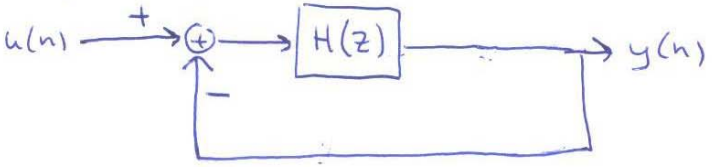


TRANSFER

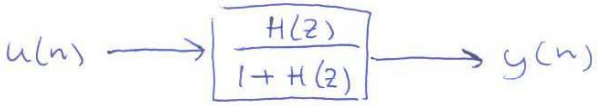


Johns & Martin are treating the linear model as having two independent inputs.

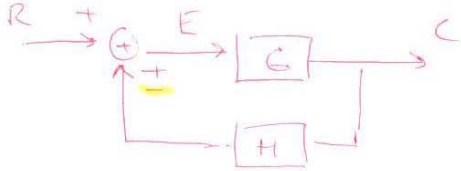
SIGNAL



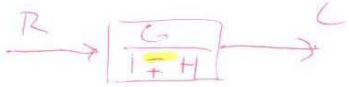
Eliminating the feedback loop:



ORIGINAL:



REDUCED:



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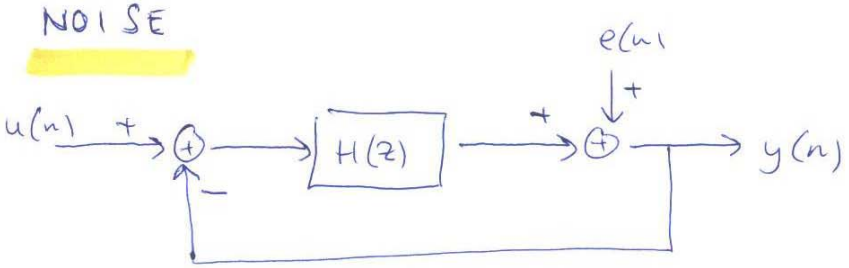
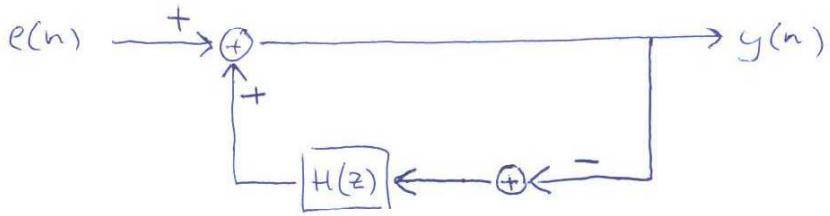
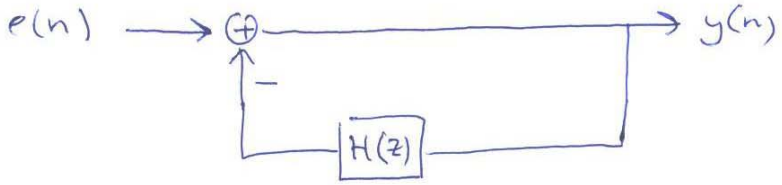
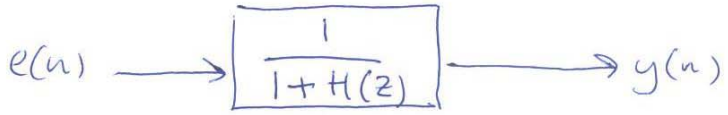
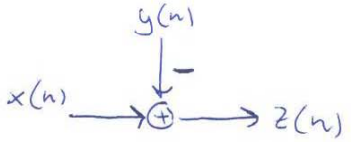
NOISE











$$z(n) = x(n) - y(n)$$

$$S_{TF}(z) \equiv \frac{Y(z)}{V(z)} \qquad (14.15)$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} \qquad (14.16)$$

THE OUTPUT SIGNAL CAN BE WRITTEN AS A COMBINATION OF THE INPUT SIGNAL AND THE NOISE SIGNAL EACH BEING FILTERED BY THE CORRESPONDING TRANSFER FUNCTION.

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