Last time – and today, Tuesday 13th of April:

March the 23rd:

14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
2nd order sigma delta design example
16.1 Basic Phase Locked Loop Architecture

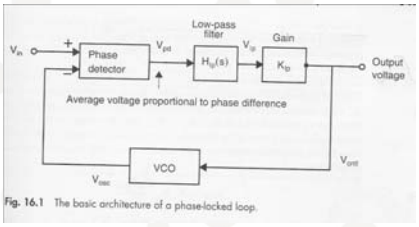

Fig. 16.1 The basic architecture of a phase-locked loop.

Today:
16.1Linearized small-signal analysis of general PLLs
16.2 PLLs with charge-pump phase comparators
16.3 Voltage controlled oscillators
16.4 Computer Simulations of PLLs
About writing the report

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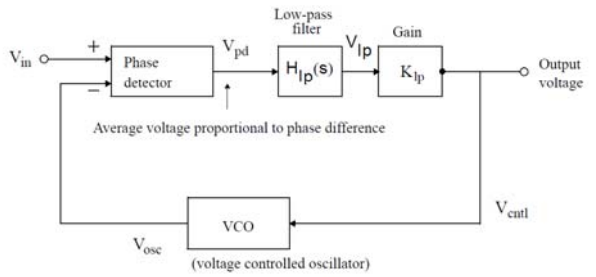
PLL Basic Architecture



- In general, output may be V_{cntl} or V_{osc}

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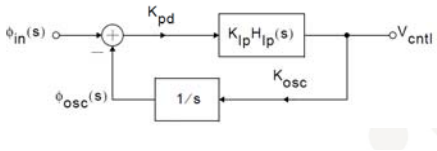
PLL linear model applying to almost every PLL



$$V_{cntl}(s) = K_{pd}K_{lp}H_{lp}(s)[\phi_{in}(s) - \phi_{osc}(s)]$$

$$\phi_{osc}(s) = \frac{K_{osc}V_{cntl}(s)}{s}$$

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p}$$

- Combining above 2 equations ...

$$\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{sK_{pd}K_{lp}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a highpass response from input phase to control voltage
- Can also be written as

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{K_{pd}K_{lp}K_{osc}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a lowpass response from input phase to output phase

- Differences between PLLs are determined only by what is used for the LP-filter ($H_{lp}(s)$), the Phase Detector (K_{pd}) or the oscillator (K_{osc}).

12. april 2010

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More on the 2nd order PLL model

2nd order transfer functions are often written in the form

$$H(s) = \frac{N(s)}{D(s)}$$

$$D(s) = 1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}$$

ω_0: resonant frequency

Transient time for the complete loop:

$$\tau_{pll} \approx \frac{1}{\omega_0}$$

Q: Q-factor, damping factor

Good settling: $Q = 0.5$

max. flat group delay: $Q = \frac{1}{\sqrt{3}} = 0.577$

max. flat amplitude resp: $Q = \frac{1}{\sqrt{2}} = 0.707$

$$\omega_0 = \frac{K_{pll}}{\sqrt{\tau_p}} \quad (16.32)$$

$$Q = \frac{\sqrt{\tau_p}}{\frac{1}{K_{pll}} + \tau_z K_{pll}}$$

$$K_{pll} = \sqrt{K_{pd} \cdot K_{lp} \cdot K_{osc}}$$

Usually, when $\omega_0 << \omega_{sr}$:

$$Q \approx \frac{1}{\omega_0 \tau_z} = \frac{\sqrt{\tau_p}}{\tau_z K_{pll}} \quad (16.35)$$

When $Q = 0.5$:

$$\tau_z = \frac{2\sqrt{\tau_p}}{K_{pll}} = \frac{2}{\omega_0}$$

12. a

5

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Capture range, lock range, false lock

- The maximum difference between the input signal's frequency and the oscillator's free-running frequency where lock can eventually be attained is defined as the capture range
- One lock is attained, as long as the input signal's frequency changes only slowly it will remain in lock over a range that is much larger than the capture range
- When a multiplier is used for the phase detector the loop may lock to harmonics (multiple of the frequency) of the input signal. This is called a false lock.

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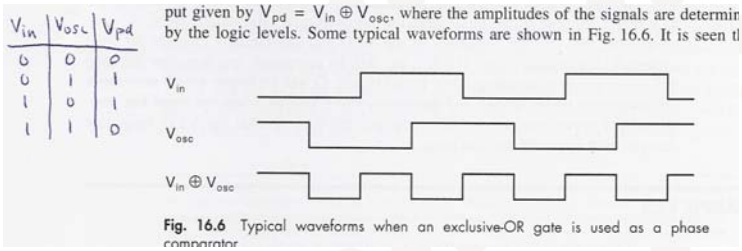
Exclusive-OR Phase comparators



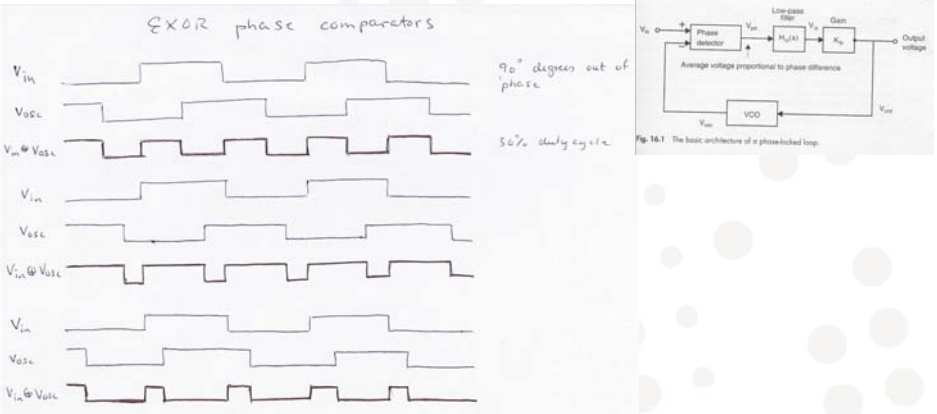
V_{in}	V_{osc}	V_{pd}
0	0	0
0	1	1
1	0	1
1	1	0

put given by $V_{pd} = V_{in} \oplus V_{osc}$, where the amplitudes of the signals are determir
by the logic levels. Some typical waveforms are shown in Fig. 16.6. It is seen tl

Fig. 16.6 Typical waveforms when an exclusive-OR gate is used as a phase comparator

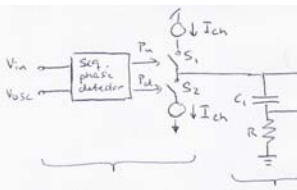
- When the waveforms are 90 degrees out of phase the output is a waveform at twice the frequency of the input signal and has a 50 percent duty cycle.
- If all waveforms are symmetric about 0 volts the average value extracted by the low-pass filter would be zero.

EXOR phase comp



- When the waveforms become more out of phase, the average value of the output signal is positive; whereas when they become more in phase, the average value of the output signal is negative

CHARGE-PUMP COMPARATOR



- no false lock, attains lock quickly
- V_{in} and V_{osc} are exactly in phase when the system is in lock.
- injects, leaves alone, or subtracts charge on the capacitor in the LP-filter, depending on P_u and P_d.
- S_1 closed: I_{ch} increases the control voltage into the VCO
  S_2 closed: I_{ch} flows out of the LP-filter, decreasing the control voltage.
  S_1 and S_2 open: steady state
- P_u and P_d are digital signals
- IF V_{in} goes to 1 before V_{osc}, then P_u will be 1 during the time that the signals are different. ⇒ injecting charge
  ELSE if V_{osc} goes to 1 before V_{in}, P_d will be 1 during the time that the inputs are different ⇒ S_2 will be closed, removing charge from the loop-filter and decreasing the VCO frequency.

OBS! Notice that P_u only goes high at the leading edges and is insensitive to the falling edges.

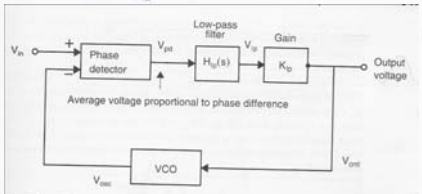
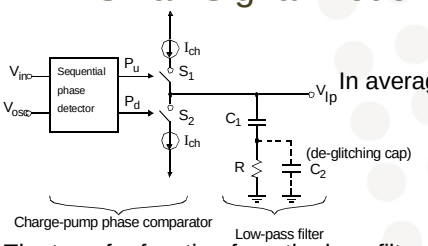


Fig. 16.1 The basic architecture of a phase-locked loop.

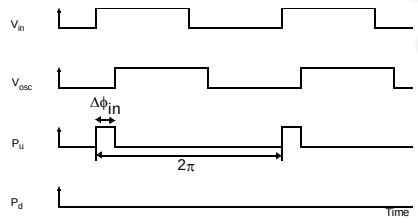
Small-Signal Model of the Charge-Pump PLL



In average the current from the CP is: $I_{avg} = \frac{\Delta\phi_{in}}{2\pi} I_{ch}$

The transfer function from the loop filter is (C2 ignored):

$$H_{lp}(s) = \frac{V_{lp}(s)}{I_{avg}(s)} = R + \frac{1}{sC_1} = \frac{1 + sRC_1}{sC_1}$$



$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{(1 + sRC_1)}{1 + sRC_1 + \frac{s^2 C_1}{K_{pd} K_{osc}}}$$

$$\omega_0 = \frac{1}{\tau_{pll}} = \sqrt{\frac{I_{ch} K_{osc}}{2\pi C_1}}$$

$$Q = \frac{1}{RC_1\omega_0} = \frac{1}{R}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}}$$

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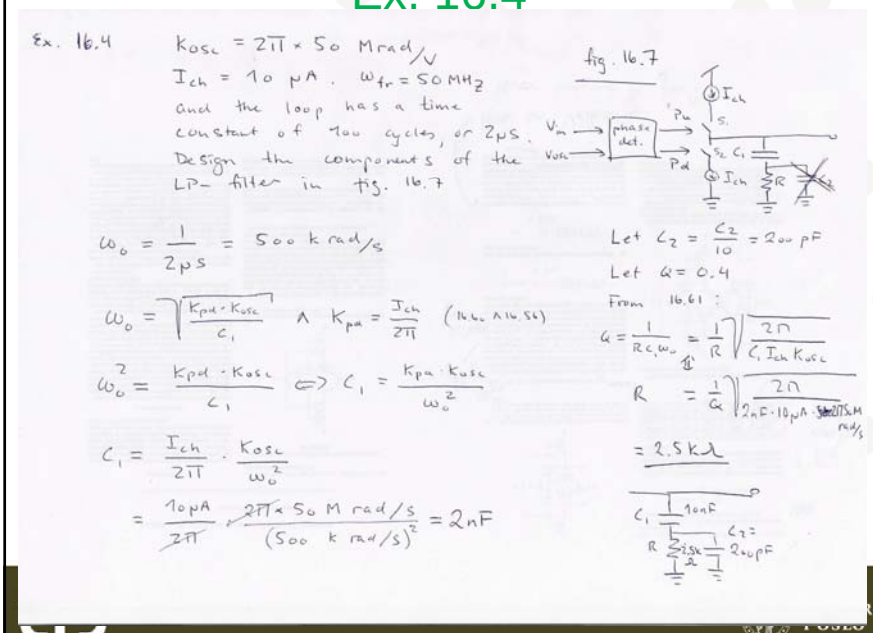
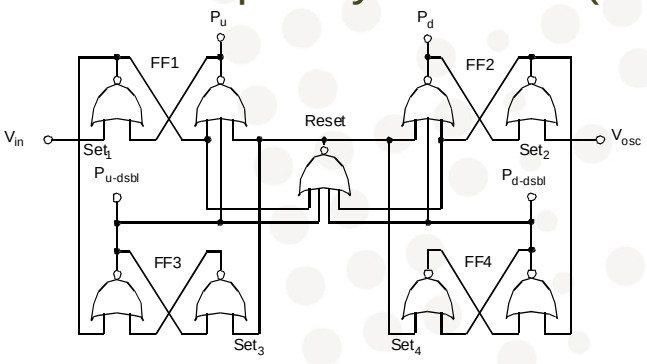
Ex. 16.4

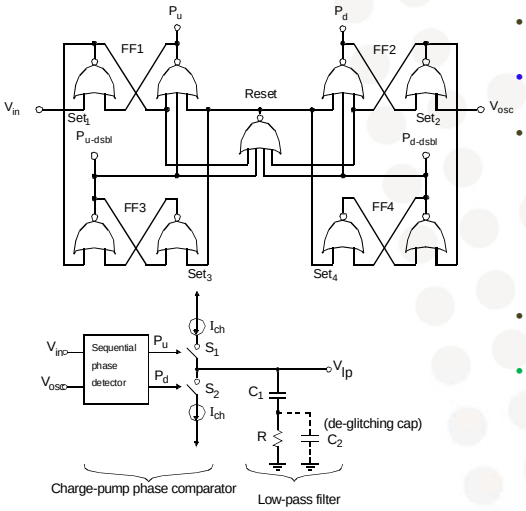


Phase Frequency Detector (PFD)



- Most commonly used sequential phase detector is the Phase Frequency Detector (PFD).
- This circuit handles phase differences up to 2π.

Phase Frequency Detector (PFD)



- Assume P_u, P_d, $P_{u\text{-}dsbl}$, $P_{d\text{-}dsbl}$, Reset, V_{in}, V_{osc} are low
- V_{in} goes high; FF1 set/ Pu goes high -> VCO frequency increases
- V_{osc} goes high; FF2 set temporarily, reset goes high, causing P_u and P_d go low after some delay. Reset going high causes FF3 and FF4 to be set and $P_{u\text{-}dsbl}$ and $P_{d\text{-}dsbl}$ go high, which later causes reset to go low. FF1 and FF2 are kept in reset mode and P_u and P_d low.
- V_{in} goes back to 0; FF3 reset and $P_{u\text{-}dsbl}$ is turned off.
- Similarly, when V_{osc} goes low, FF4 is reset goes low, FF4 is reset and $P_{d\text{-}dsbl}$ goes low. (back to original state).

  (The operation is very similar if V_{osc} leads V_{in})

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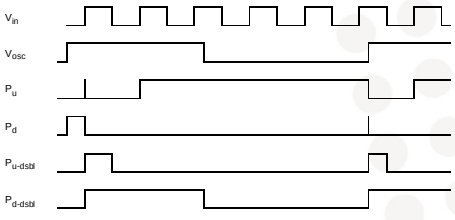
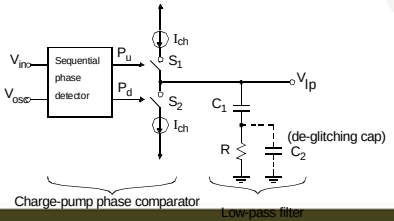
PFD waveforms – when V_{in} has a much higher frequency than Vosc





- Whenever a positive going edge of Vin occurs, Pu goes high causing the VCO frequency to increase, and stays high until both Vin and Vosc go to 1. Then reset goes high, setting both Pu-dsbl and Pd-dsbl, and causing Pu and Pd to go low. The next time Vin goes to o, FF1 is reset, which resets FF3, turning Pu-dsbl off.
- Most of the time (here) Pu is high, causing Vosc to quickly increase in frequency until lock is achieved.
- No false lock
- Only suitable for digital (non-sine) inputs

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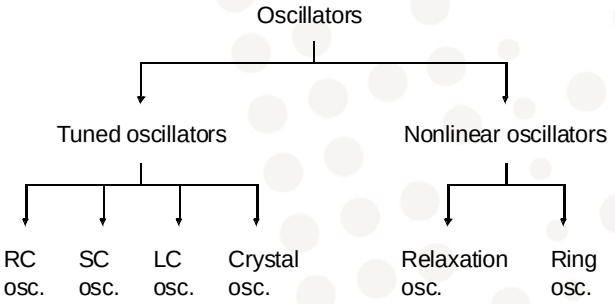
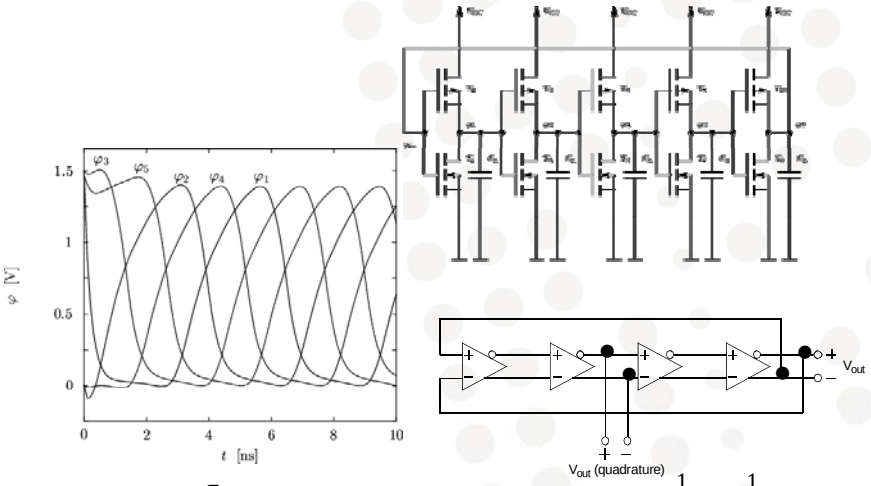
Voltage controlled oscillators (VCO)



- Sinusoidal output oscillators usually realized some frequency selective or tuned circuit in feedback configuration, while square-wave output oscillators are usually realized using a nonlinear feedback config.
- The tuned oscillators offers better frequency stability, but limited tuning range.

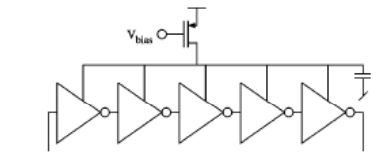
Ring oscillators



τ_{inv} is the delay of each inverter

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_{inv}}$$

0.2 V subthreshold VCO



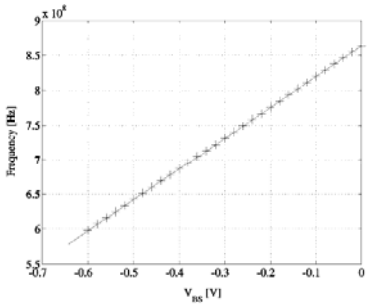


Figure 3. RVCO transfer function for a 5 stage RVCO simulated in Cadence

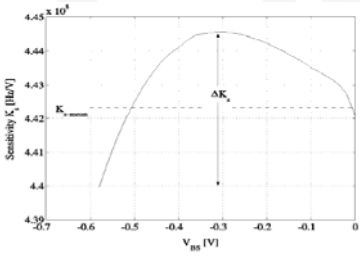


Figure 4. Sensitivity of the RVCO illustrates a nonlinearity of 0.5 %

Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion

Ulrik Wismar, Dag Wisland**, Pietro Andreani**

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Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

**Microelectronic Systems, Department of Informatics
University of Oslo, N-0316 Oslo, Norway

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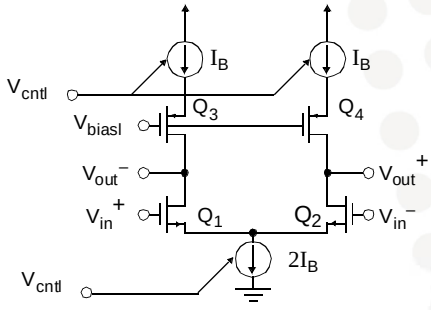
Differential inverter



- Programmable delay
- Cascode transistors Q3, Q4 to increase output impedance of programmable current sources for better PSRR
- I_B = Kbias Vcntl (proportional)
- Tau proportional to C_L / g_m, f_{osc} proportional to SQRT(V_{cntl}) ;nonlinear

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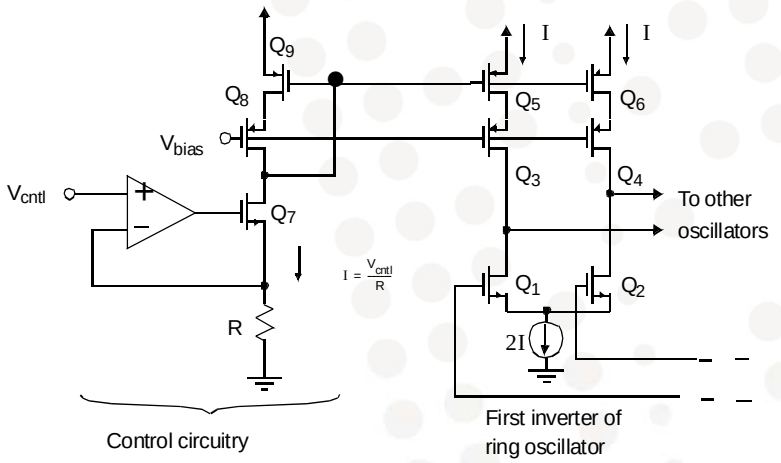
Bias circuit



Computer simulations of PLLs

- Nontrivial due to often very wide range of time constants present in PLLs.
- SPICE simulations only may be highly impractical and take too long time.
- Possible approach:

  Simulate the individual components using SPICE over a few periods of the VCO's output waveform before simulating the complete system using simplified models where continous time components are replaced by approximately equivalent difference-equation models;

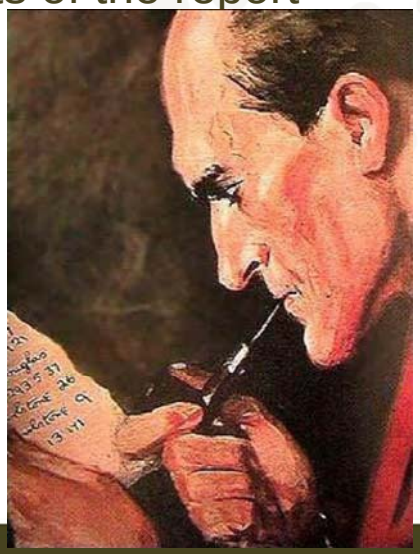
  Simulink in Matlab (easy, don't need much expertise)

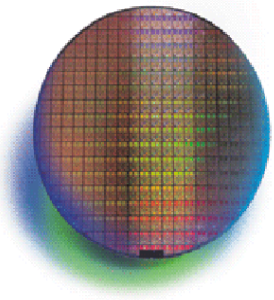
  or custom difference equations using for example C. (fast and may be modified for greater accuracy)

Additional litterature

- Ulrik Wismar, Dag T. Wisland, Pietro Andreani: Linearity of Bulk-Controlled Inverter Ring VCO in weak and strong inversion, Proceedings of IEEE Norchip Conference, 2005.
- http://www.eecg.toronto.edu/~johns/nobots/Book/book.html
- http://www.iue.tuwien.ac.at/phd/grasser/node83.html (Ring osc.)

Remember: Grading is based on the contents of the report





Some pointers

- http://www.idi.ntnu.no/~lasse/DM/SkriveTips.php

- **Preface**
- **(Acknowledgement)**
- **1 Introduction**
- **2 Theoretical background**
- **(2.1 Various approaches to Nifty Gadgets)**
- **2.2 Nifty Gadgets my way**
- **3 My implementation of a Nifty Gadget**
- **4 Nifty Gadget results**

5 Discussion

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Nifty Gadget / DAC chapter 3

- **3 My implementation of a Nifty Gadget**
- Can you describe your implementation in detail?
  Why did you use this technology?
  How does the theory relate to your implementation?
  What are your underlying assumptions?
  What did you neglect and what simplifications have you made?
  What tools and methods did you use?
  Why use these tools and methods?

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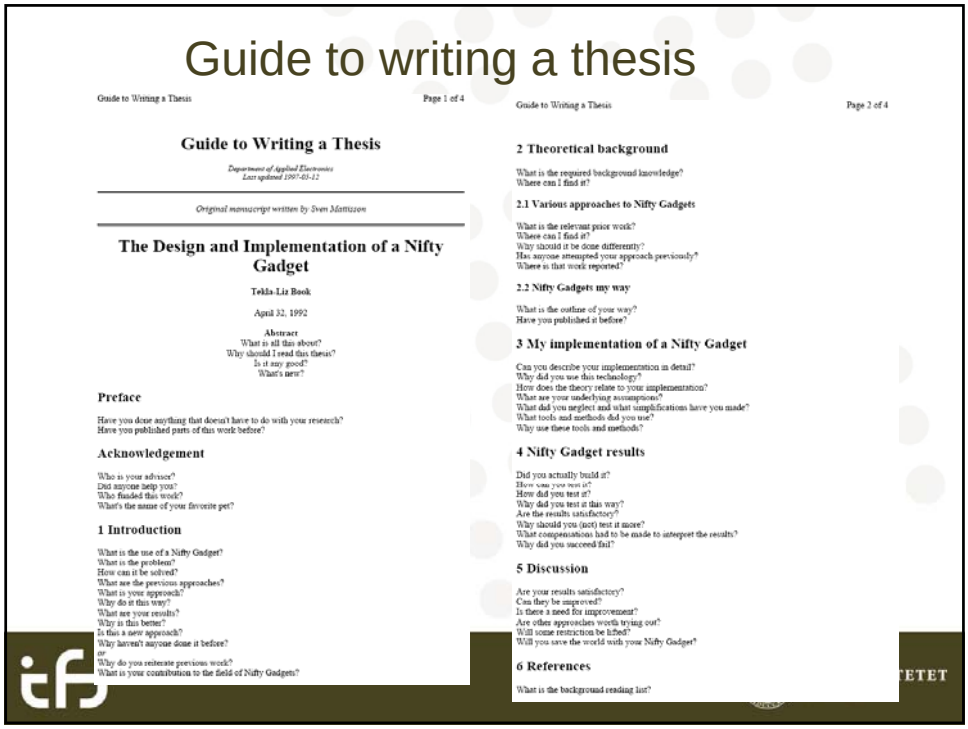
Nifty Gadget / DAC chapter 4

- **4 Nifty Gadget results**
- Did you actually build it?
  How can you test it?
  How did you test it?
  Why did you test it this way?
  Are the results satisfactory?
  Why should you (not) test it more?
  What compensations had to be made to interpret the results?
  Why did you succeed/fail?

Nifty Gadget / DAC chapter 5

- **5 Discussion**
- Are your results satisfactory?
  Can they be improved?
  Is there a need for improvement?
  Are other approaches worth trying out?
  Will some restriction be lifted?
  Will you save the world with your Nifty Gadget?

Guide to writing a thesis



Guide to Writing a Thesis Page 1 of 4

Guide to Writing a Thesis

Department of Applied Electronics
Last updated 1997-03-12

Original manuscript written by Sven Mattisson

The Design and Implementation of a Nifty Gadget

Tekla-Liz Book

April 32, 1992

Abstract
What is all this about?
Why should I read this thesis?
Is it any good?
What's new?

Preface

Have you done anything that doesn't have to do with your research?
Have you published parts of this work before?

Acknowledgement

Who is your advisor?
Did anyone help you?
Who finaded this work?
What's the name of your favorite pet?

1 Introduction

What is the use of a Nifty Gadget?
What is the problem?
How can it be solved?
What are the previous approaches?
What is your approach?
Why do it this way?
What are your results?
Why is this better?
Is this a new approach?
Why haven't anyone done it before?
or
Why do you reiterate previous work?
What is your contribution to the field of Nifty Gadgets?

Guide to Writing a Thesis Page 2 of 4

2 Theoretical background

What is the required background knowledge?
Where can I find it?

2.1 Various approaches to Nifty Gadgets

What is the relevant prior work?
Where can I find it?
Why should it be done differently?
Has anyone attempted your approach previously?
Where is that work reported?

2.2 Nifty Gadgets my way

What is the outline of your way?
Have you published it before?

3 My implementation of a Nifty Gadget

Can you describe your implementation in detail?
Why did you use this technology?
How does the theory relate to your implementation?
What are your underlying assumptions?
What did you neglect and what simplifications have you made?
What tools and methods did you use?
Why use these tools and methods?

4 Nifty Gadget results

Did you actually build it?
How can you test it?
How did you test it?
Why did you test it this way?
Are the results satisfactory?
Why should you (not) test it more?
What compensations had to be made to interpret the results?
Why did you succeed/fail?

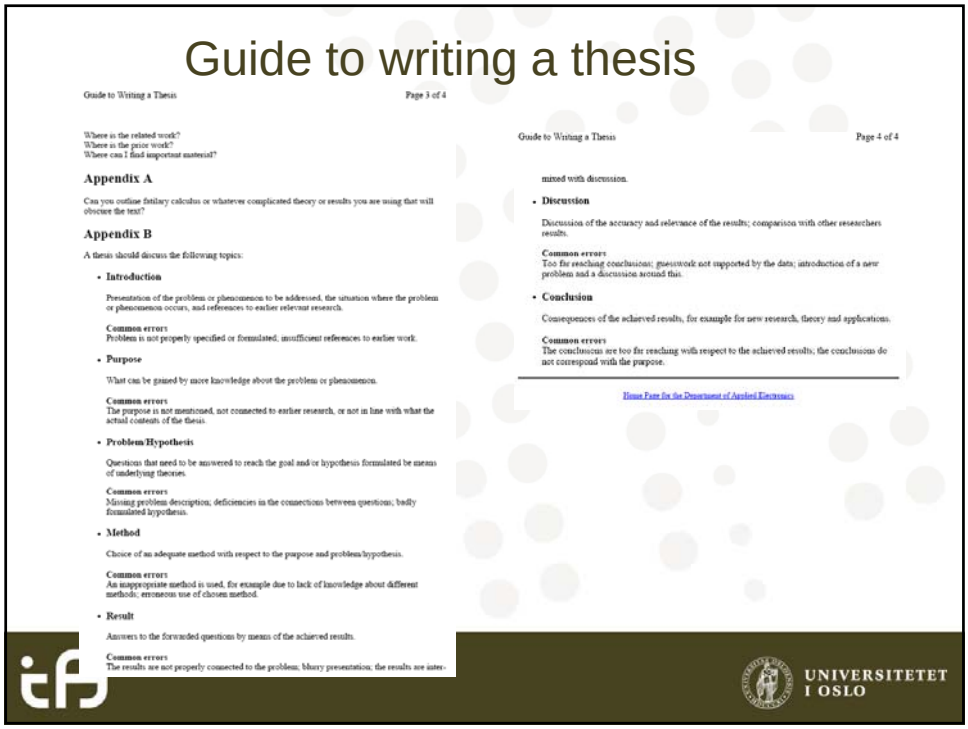
5 Discussion

Are your results satisfactory?
Can they be improved?
Is there a need for improvement?
Are other approaches worth trying out?
Will some restriction be lifted?
Will you save the world with your Nifty Gadget?

6 References

What is the background reading list?

Guide to writing a thesis



Guide to Writing a Thesis Page 3 of 4

Where is the related work?
Where is the prior work?
Where can I find important material?

Appendix A

Can you outline fatilary calculus or whatever complicated theory or results you are using that will obscure the text?

Appendix B

A thesis should discuss the following topics:

- **Introduction**

  Presentation of the problem or phenomenon to be addressed, the situation where the problem or phenomenon occurs, and references to earlier relevant research.

  Common errors
  Problem is not properly specified or formulated; insufficient references to earlier work.

- **Purpose**

  What can be gained by more knowledge about the problem or phenomenon.

  Common errors
  The purpose is not mentioned, not connected to earlier research, or not in line with what the actual contents of the thesis.

- **Problem/Hypothesis**

  Questions that need to be answered to reach the goal and/or hypothesis formulated be means of underlying theories.

  Common errors
  Missing problem description; deficiencies in the connections between questions; badly formulated hypothesis.

- **Method**

  Choice of an adequate method with respect to the purpose and problem/hypothesis.

  Common errors
  An inappropriate method is used, for example due to lack of knowledge about different methods; erroneous use of chosen method.

- **Result**

  Answers to the forwarded questions by means of the achieved results.

  Common errors
  The results are not properly connected to the problem; blurry presentation; the results are inter-

Guide to Writing a Thesis Page 4 of 4

mixed with discussion.

- **Discussion**

  Discussion of the accuracy and relevance of the results; comparison with other researchers results.

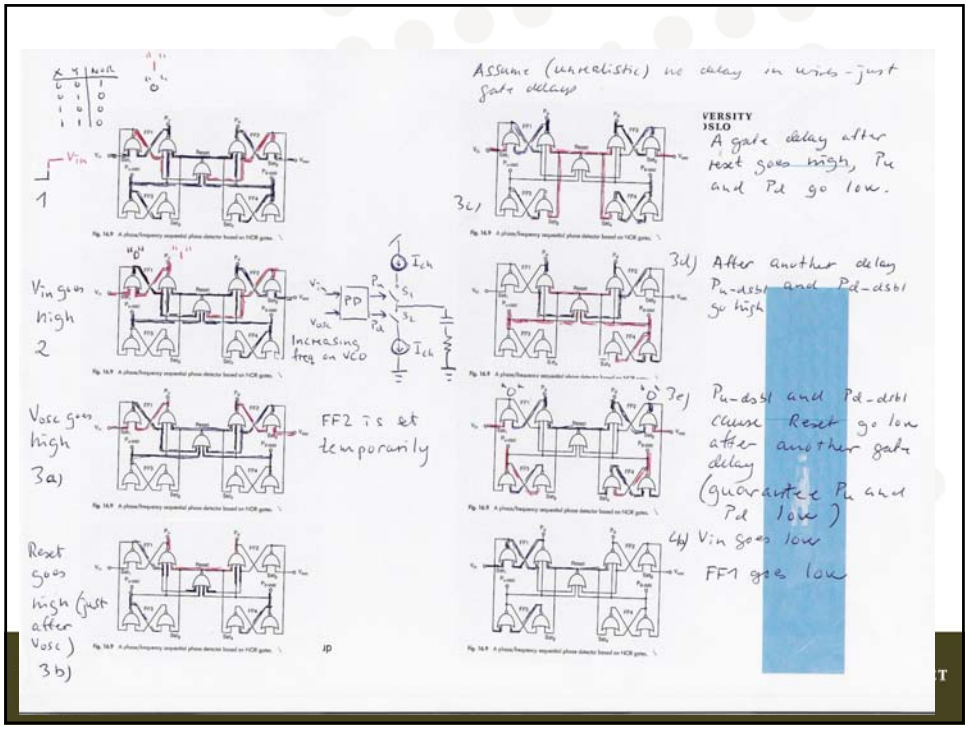
  Common errors
  Too far reaching conclusions; guesswork not supported by the data; introduction of a new problem and a discussion around this.

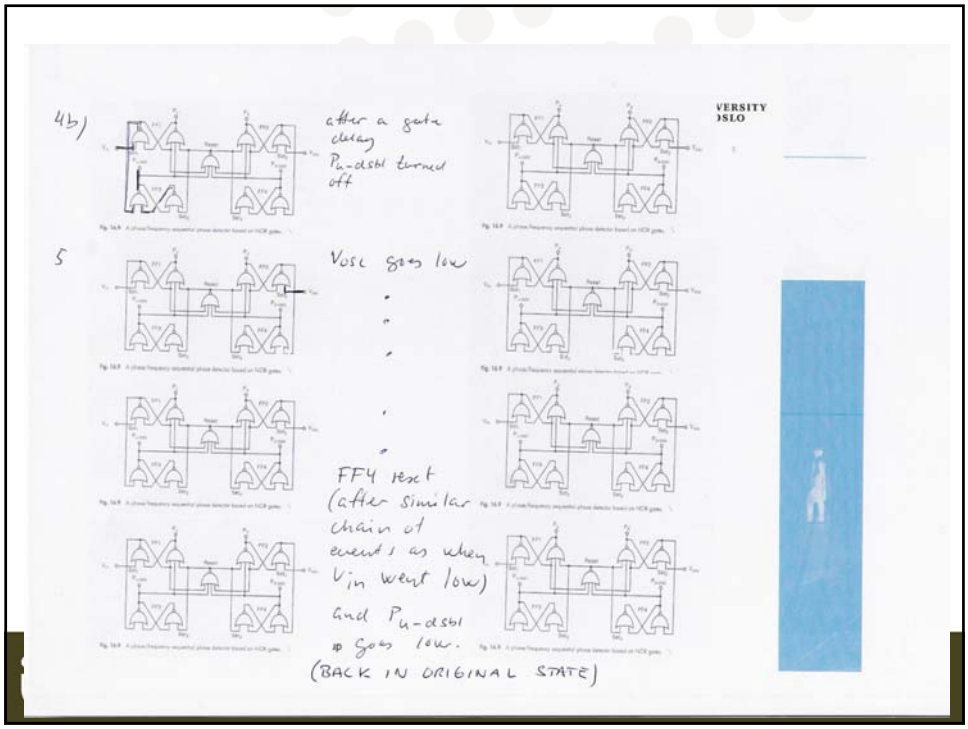
- **Conclusion**

  Consequences of the achieved results, for example for new research, theory and applications.

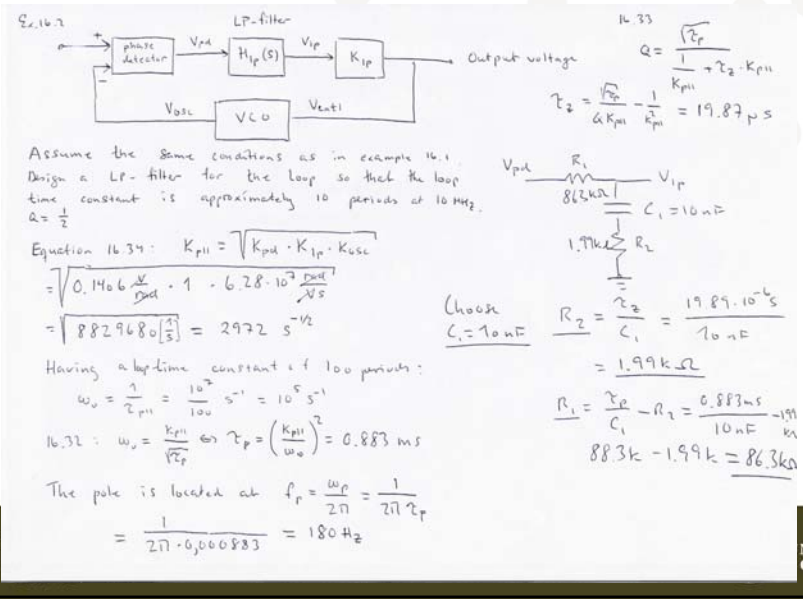
  Common errors
  The conclusions are too far reaching with respect to the achieved results; the conclusions do not correspond with the purpose.

Home Page for the Department of Applied Electronics


Assume (unrealistic) no delay in wires - just gate delays
A gate delay after Vosc goes high, Pu and Pd go low.
After another delay Pu-dsbl and Pd-dsbl go high
Pu-dsbl and Pd-dsbl cause Reset go low after another gate delay (guarantee Pu and Pd low)
Vin goes low
FF1 goes low
Vin goes high
2
Vosc goes high
3a)
FF2 is set temporarily
Reset goes high (just after Vosc)
3b)
Increasing freq on VCO
PD


4b)
after a gate delay Pu-dsbl turned off
5
Vosc goes low
FF4 reset (after similar chain of events as when Vin went low) and Pu-dsbl goes low.
(BACK IN ORIGINAL STATE)

Ex. 16.2



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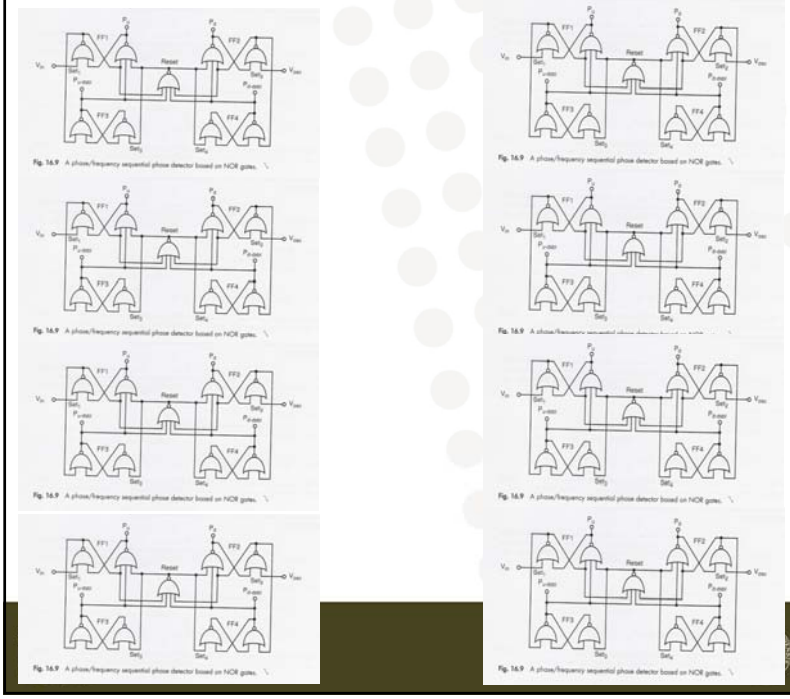

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