

# A 0.7-V 100-dB 870- $\mu$ W Digital Audio $\Sigma\Delta$ Modulator

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## Abstract

A high-precision, low-voltage, low-power  $\Sigma\Delta$  modulator has been designed using a delayed input feedforward architecture and a tracking multi-bit quantizer employing a single comparator. A 0.18- $\mu$ m CMOS experimental prototype achieves 100 dB of dynamic range, 100-dB peak SNR and 95-dB peak SNDR for a signal bandwidth of 25 kHz, while consuming only 870  $\mu$ W of total power from a 0.7-V supply at a 5-MHz sampling rate.

Keywords: A-to-D conversion, sigma-delta modulation, feedforward, chopper stabilization

## Introduction

The continuing CMOS technology scaling mandates the use of reduced supply voltages to ensure device reliability. Moreover, the proliferating demand for battery-operated systems requires low power dissipation. These two requirements impose significant challenges on the design of high-precision analog-to-digital interfaces owing to the reduced signal swings and voltage headroom.

The sigma-delta ( $\Sigma\Delta$ ) modulator proposed herein combines delayed input feedforward with a single-comparator tracking multi-bit quantizer and chopper stabilization to achieve high-resolution, low-voltage operation, and high power efficiency. An experimental prototype of the modulator has been integrated in a 0.18- $\mu$ m CMOS technology.

## Delayed Feedforward Architecture

The proposed modulator architecture, shown in Fig. 1, is a single-stage, second-order  $\Sigma\Delta$  modulator with delayed input feedforward and a single-comparator, 18-level multi-bit quantizer. The combination of input feedforward and multi-bit quantization results in very low voltage swings in the analog forward-path integrators, even for large input signals, because the integrators only process the quantization error [1].

To relax the timing requirements imposed by the modulator feedback loop, one sample delay is introduced into the input feedforward path. As a consequence, half of the

sampling period is then available for the operation of the quantizer and feedback DAC. However, because of the delay in the input feedforward path, the input signal is not completely removed from the input to the forward-path integrators. In general, a delayed input feedforward modulator loop with  $n^{\text{th}}$ -order shaping of the quantization error provides  $(n+1)^{\text{th}}$ -order shaping of the input component fed into the first integrator. Thus, in the proposed modulator the residual component of the input signal injected into the input of the first integrator undergoes approximately third-order shaping, and only a negligible component of the modulator input is processed by the forward-path integrators.

In order to reduce the power dissipation and area of the multi-bit quantizer, as well as the loading it imposes on the preceding circuits, a tracking multi-bit quantization approach is adopted [2]. Basically, because of the oversampling the input changes relatively slowly in comparison with the sampling rate. As a consequence, the number of comparators used in the quantizer can be reduced by providing dynamically adjusted comparator reference levels that depend on previous comparator outputs. Unfortunately, offset mismatch among the remaining comparators results in increased inband quantization error, harmonics, and integrator output voltage swings, as well as degraded tracking performance. To avoid this sensitivity to the comparator offset mismatch, the use of a single tracking comparator is proposed. To provide the required tracking, this comparator must perform three comparisons per cycle, each with a different reference level. As shown in Fig. 1, when tracking multi-bit quantization with a single comparator is used, data-weighted averaging (DWA) logic can be located in the slow modulator feedback path to further relax timing constraints [2].

## Circuit Implementation

The modulator architecture with reduced integrator input and output swings allows for the use of power-efficient, low-voltage integrators employing single-stage folded-cascode operational amplifiers (op amps) [1]. With reduced integrator input swings, op amp slewing is avoided. Since incomplete but linear settling of the op amps only introduces gain error, the first integrator in the experimental modulator uses a relatively low bandwidth op amp that settles for only 3.8 time constants, which significantly lowers the op amp power dissipation. Chopper stabilization is used for the first integrator op amp to suppress flicker noise. Chopping is performed at 2.5 MHz in the middle of integrator sampling phase so as not to interrupt integrator operation [3].

A simplified single-ended schematic and the control signals for the delayed input feedforward path, the analog summation circuitry and the quantizer are shown in Fig. 2. The actual implementation is fully differential. In the feedforward path, the modulator input is alternately sampled onto

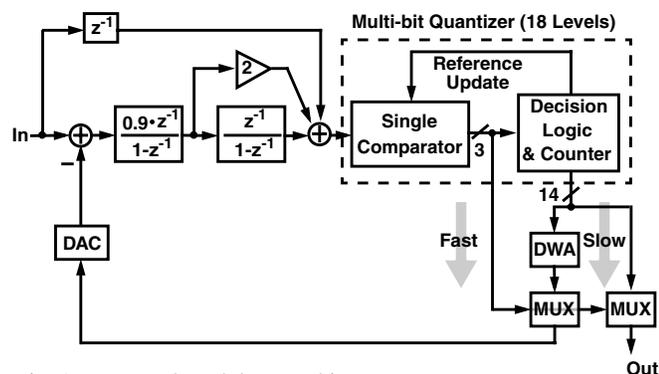


Fig. 1. Proposed modulator architecture.

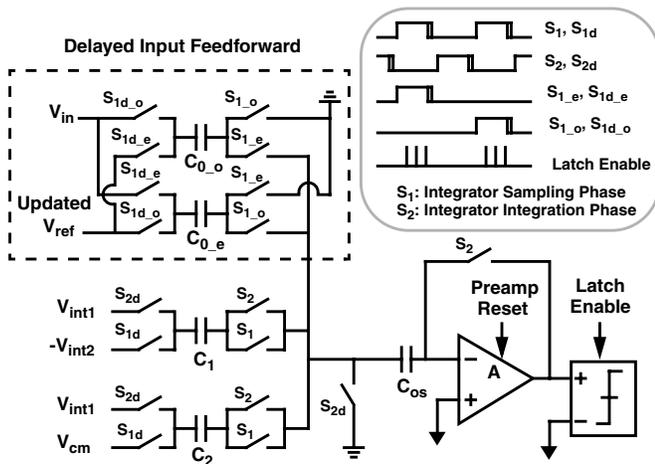


Fig. 2. Delayed input feedforward, analog summation and quantizer. sampling capacitors  $C_{0_o}$  and  $C_{0_e}$ . Because of extended time provided by delaying the input feedforward, the comparator speed needed to complete three comparisons per cycle is relaxed.

Although capacitive summation is power efficient, it is accompanied by substantial signal attenuation due to the charge sharing. Consequently there is a corresponding amplification of errors in the comparator when they are referred back to the input of the summation block. To suppress the potentially large offset in the comparator latch, a preamplifier with input offset storage and cancellation is used. The preamplifier block consists of two cascaded preamplifier stages to achieve increased gain-bandwidth product and provide a common mode level shift [1].

NMOS and PMOS switches are used, along with local clock bootstrapping [4] or local clock boosting where needed. Even with a supply voltage of only 0.7 V, circuit simulations confirm that with clock bootstrapping switches a total harmonic distortion of approximately  $-113$  dB can be achieved for the input sampling network.

### Measurement Results

The experimental  $\Sigma\Delta$  modulator has been fabricated in a  $0.18\text{-}\mu\text{m}$  CMOS technology. Fig. 3 is a photograph of the chip. Fig. 4 shows the measured SNR and SNDR for the experimental prototype. The dynamic range is 100 dB, the peak SNR is 100 dB, and the peak SNDR is 95 dB for a 25-

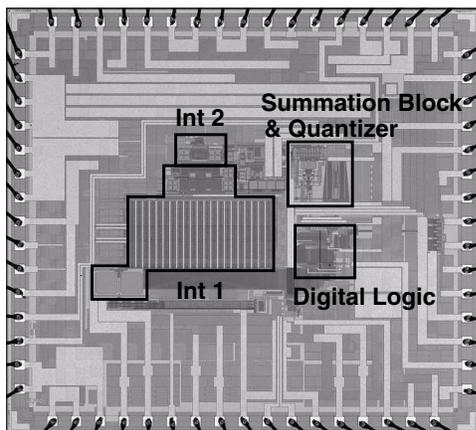


Fig. 3. Chip micrograph.

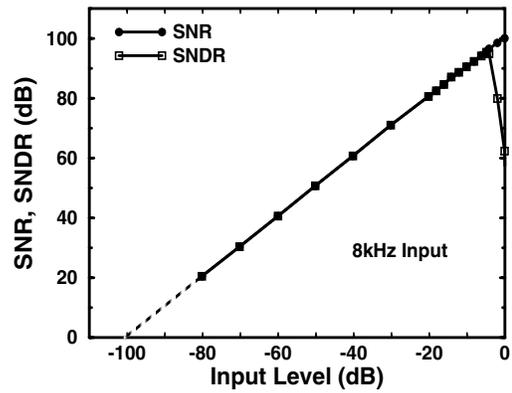


Fig. 4. Measured SNR and SNDR.

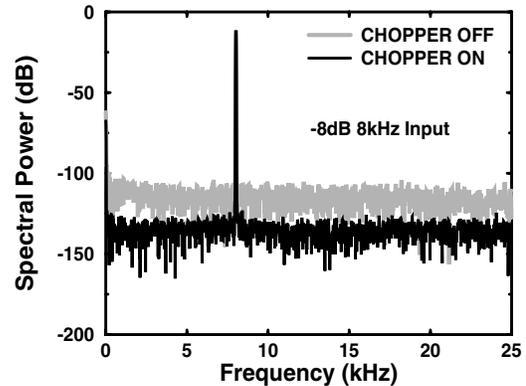


Fig. 5. Measured output spectrum.

kHz signal bandwidth. The prototype operates from a 0.7-V supply at a 5-MHz sampling rate. The measured analog and digital power dissipation is  $680\ \mu\text{W}$  and  $190\ \mu\text{W}$ , respectively. As shown in Fig 5, without chopper stabilization the dynamic range is limited to 79 dB.

With an analog supply voltage of only 0.5 V, the dynamic range achieved is 92 dB, the peak SNDR is 84 dB and total power dissipation is  $450\ \mu\text{W}$ . The total active die area, excluding bonding pads, decoupling capacitors and output drivers is approximately  $2.16\text{mm}^2$ .

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### References

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