Welcome to INF4420 Projects in Analog and mixed signal CMOS design !

Introduction, Tuesday 26th of January, 2010

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INF4420 – V2010:

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- kritr
- sindrso
- mshaugla
- geiraby
- anderhf
- toreivib
- mortenhr
- moradi
- anhtv
- michaol
- kklee

- Lærere:
- Amir Hasanbegovic
- Snorre Aunet

3. februar 2010 2

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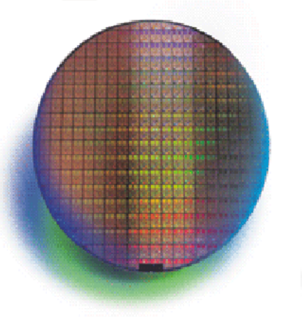
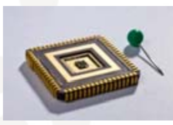
Outline – Tuesday 20th of January

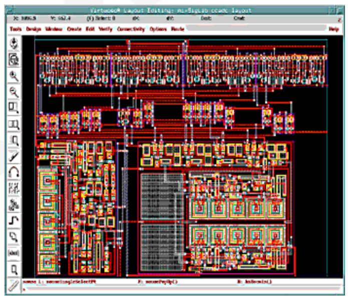
- Practical issues
- Learning goals
- Design project, tools and methods
- Syllabus
- Very brief introduction to various circuit building blocks (sample-and-holds, bandgap references, switched capacitor circuits, Nyquist- and oversampling data converters, phase-locked loops)

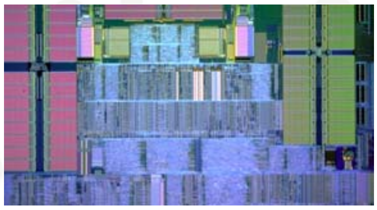


CMOS Integrated Circuits?

- Digital circuits exploit mainly transistors and interconnect
- Mixed-Signal (Digital AND Analog) also use resistors, capacitors and inductors
- Work-horse of modern Information Technology







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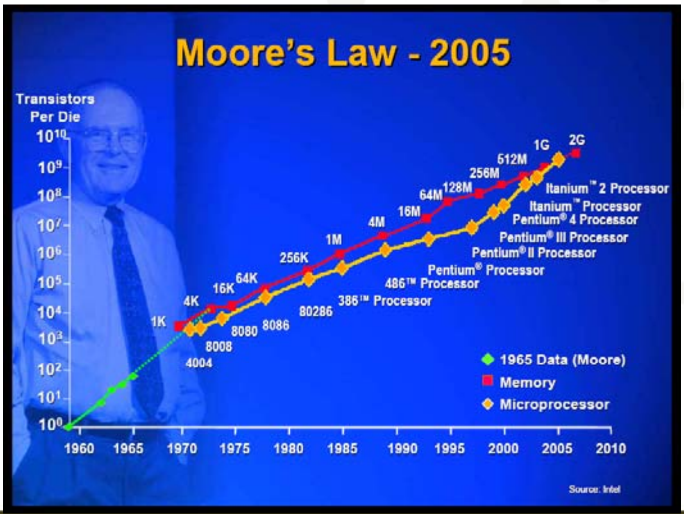
Moore's law: exponential increase in components per area



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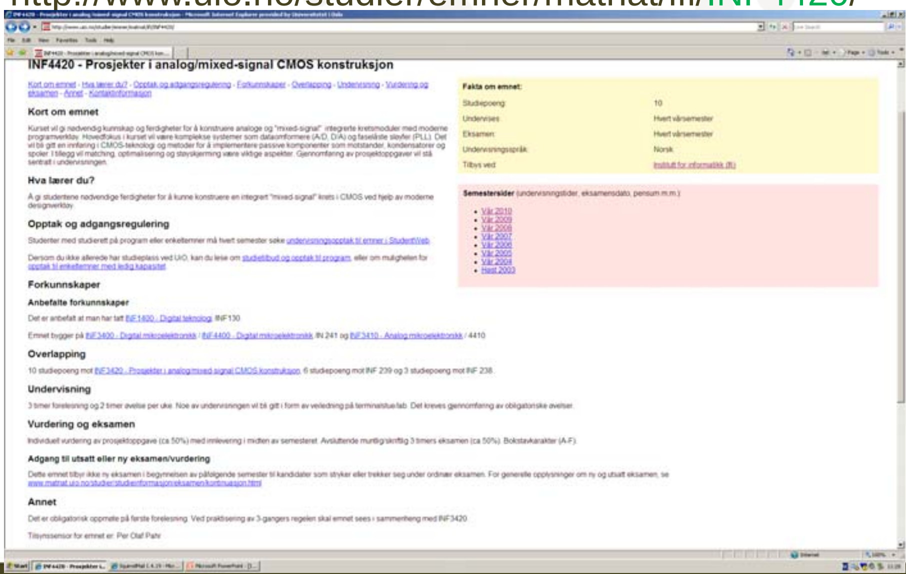
http://www.uio.no/studier/emner/matnat/ifi/INF4420/



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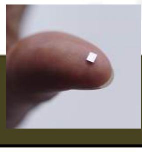
Why ASICs (Application Specific Integrated Circuits) ??

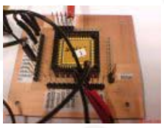
- Advantages:
  - Reduced size
  - Improved performance and functionality
  - Easier to hide ”company secrets”
  - Reduced cost
  - Reduced power consumption
  - Less radiated noise

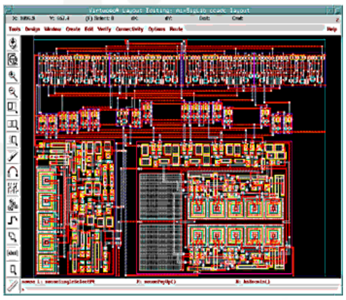
- Disadvantages:
  - Increased start-up cost
  - High power density - Heat
  - Hard to find top competence
  - Time consuming development and production
  - Time-to-market

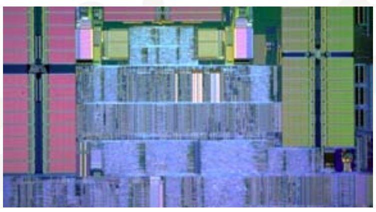


What is an integrated circuit?

- Transistors
  - Several options
- Capacitors
  - How to implement
  - Linearity
- Resistors
  - How to implement
  - Area
- Inductors
  - How to implement
  - Quality factor
- Parasitic components
  - Calculate
  - Minimize







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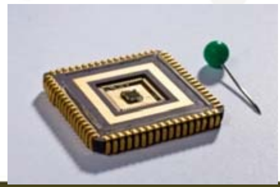
Design methods; digital from HDL, full custom analog

- Digital systems:
  - Automatic synthesis
    - VHDL
    - Schematic
- Analog systems:
  - Module based
  - Full-custom



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Low Power..

KISEL ELLER MJUKVARA

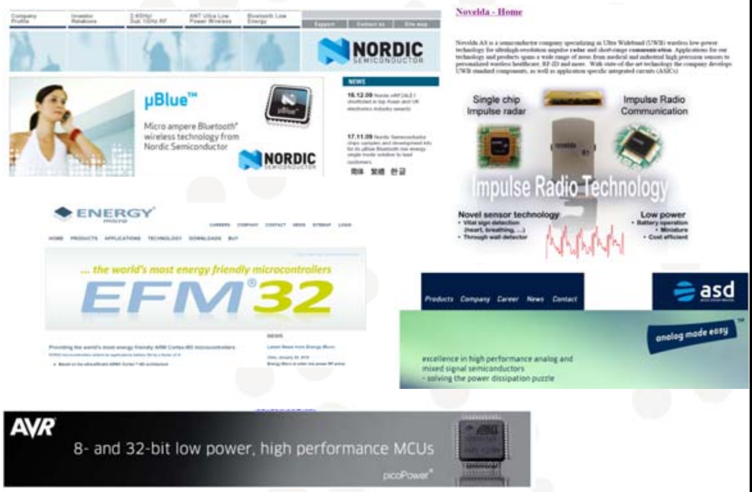
Och till slut – är pendeln på väg att svänga från mjukvara till hårdvara? Idag handlar allt om energiförbrukning och i valet mellan programmerbara system och "hårda" ASIC-lösningar är det ingen större tvekan om vad som är energieffektivast. Och det blir samtidigt allt lättare att konstruera med hjälp av färdiga IP-block.

Om det här hade jag ett långt och intressant samtal med Kathryn Kranen, vd för EDA-företaget Jasper. Kathryn Kranen hävdar med bestämdhet att hon ser allt fler halvledarkonstruktioner, inte färre. Till och med företag som inte tidigare gjort egna kretsar tar nu steget till kisel för att klara sina krav.

Det här är något som vi snart kommer att återkomma till. Ännu så länge saknas hårda data, men de exploderande mjukvarukostnaderna gör att hårdvara inte nödvändigtvis är dyrare än mjukvara. Hårdvarukonstruktörernas disciplin och effektiva verifiering kanske gör att det till slut lönar sig med hårdvara.

Men det återstår att se.

Göte Fagerfjäll



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Mandatory design project

- Design and implement mixed-mode circuit:
  - Example: ADC, SC-filter, PLL, DAC (2008)
  - System for automatic removal of mismatch (2009)
  - Milestones during the process
  - Teaching assistant, Amir Hasanbegovic, will follow up
- Write a project report
  - LaTeX or similar
- Submission: Early/Mid May
- Counts 40 % in the final grading (exam 60%)

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Challenge in 2008: Digital-to-Analog Converter (”DAC”)

INF 4420 – Prosjektoppgave: Digital til Analog Omformer – 2008

1 Introduksjon

Det skal lages en data-konverter av typen "Two-stage balanced current DAC", illustrert i figur lengre ned.

- DAC'en skal ha en oppløsning tilsvarende minimum 6 bit.
- Anta i utgangspunktet at maksimalt et en spenningsreferanse og en strømkilde er tilgjengelig, og dermed ikke trenger konstrueres.
- Digitalt ord inn (unipolart) skal være på følgende form, forutsatt 6 bit oppløsning: 00...0, 00...1, ..., 11...1.
- Utgangssignalet skal være nedad begrenset til 0.3 V og oppad begrenset til 0.7 V.
- Positiv forsyninsspenning ("Vdd") er 1.0 V. Negativ forsyningsspenning ("Vss") er 0 V.
- Maksimal DNL: +/- 1 LSB
- Kretsen slik den er i kretsskjema mangler buffer, for eksempel i form av en spenningsfølger, som gjør den i stand til å drive en kapasitiv last i form av I/O-celle ("pad"). Det er frivillig evt å lage et slikt buffer, ikke påkrevd.
- Søk en best mulig konstruksjon ut fra effektforbruk og areal.

2 Milepæler

For å sikre gjennomføring innenfor tidsrammen settes det delmål med oppgitte frister. Studentene har ansvaret for å få disse delmålene godkjent av gruppelærer.

11/3-08 Det skal leveres inn et dokument på inntil 2 sider som beskriver hvordan dere har forstått oppgaven, og skisserer hvordan dere har tenkt å løse den.

25/3-08 Testbenk for systemet skal være ferdig.

6/5 08 Design og simuleringsarbeidet for hele kretsen skal være ferdig for både skjema og utlegg, og LVS inkludert. Gruppelærer skal eventuelt godkjenne at kretsen fungerer tilfredsstillende på bakgrunn av demonstrasjon.

3 Krav til prosjektgjennomføring

Målsetningen er å lage en digital-til-analog omformer ("DAC") med minimum 6 bit nøyaktighet. Gruppens medlemmer må i fellesskap gå gjennom oppgaven og fordele arbeidsoppgaver, men samtlige skal kunne stå inne for, og redegjøre for konstruksjonen. Arbeidsfordelingen mellom deltakere i prosjektet skal rapporteres. Under følger noen tilleggsopplysninger og nærmere spesifisering.

3.1 Praktisk arbeid

1. Komplette skjema, ned til transistornivå, skal tegnes. Det skal lages symboler for de ulike byggeblokkene som inngår i det komplette systemet som utgjør dataomformeren.

2. Benytt statistiske ("Monte-Carlo") simuleringer for å verifisere funksjonalitet under prosessvariasjoner.

3. Når simuleringsresultatene er tilfredsstillende skal det tegnes fysisk utlegg ("layout") for hver av byggeblokkene, som til slutt settes sammen til den komplette kretsen.

4. Det er en del spesielle utfordringer i forbindelse med design av systemer som inneholder mixed-signal (analoge og digitale) byggeblokker. Identifiser slike utfordringer og foreta tiltak for å løse disse.

5. Benytt Layout Versus Schematic ("LVS") for delkretser og totalsystem, for å verifisere samsvar mellom kretsskjema og tilsvarende utlegg, og lette konstruksjonen. Resultatene fra LVS skal vedlegges prosjektrapporten.

4. Krav til rapport.

Sentralt i bedømmingen av arbeidet vektlegges rapportens kvalitet. Skriv den i LaTeX eller tilsvarende program. De ulike fasene av prosjektet skal dokumenteres. Dette inkluderer bla plot av skjematikk samt simueringsresultater som demonstrerer funksjonalitet hos de ulike byggeblokkene. LVS rapporter fra Cadence hører også hjemme her. Begrunn og dokumenter de ulike valgene dere har gjort. Dette inkluderer blant annet dimensjonering av aktive og passive komponenter, problematikk omkring matching, tiltak mot støy, samt layout.

Husk at bidrag fra de ulike gruppemedlemmene skal være identifiserbare.

Rapporten skal også inneholde informasjon om hvor Cadence-filer ligger tilgjengelige for etterkontroll av resultater.

Sensor bedømmer rapporten. Derfor er det viktig at denne er mest mulig forståelig for sensor.

5. frister for innlevering.

Prosjektet skal være avsluttet og rapport innlevert senest 9/5-2008 kl. 12:00. Alle gruppene må presentere resultatene av prosjektet etter innlevering. Følg med på fagets hjemmeside for evt andre beskjeder. Vurdering baseres på en bedømming av arbeidets kvalitet, og rapportens kvalitet, slik dette framgår av sistnevnte. En prosentuell score vektes inn i endelig karakter for faget.

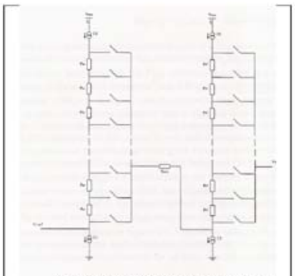

Fig 4.6 Diagram, two-stage balanced current DAC.

Fra "High-Speed Data Converters Fully Integrated in CMOS", Leif Hanssen, dr. scient. avhandling., Ifi, UiO, 1990.

Lykke til!!

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INF4420 Project 2009 (1/2)

INF4420 project description

Some years from now, you have been hired by an undisclosed chip maker as their mixed signal designer, partly because of your acheivements in the INF4420 course. The company is currently working hard towards finishing their new flagship product. The system designers in your group already have very promising high level simulation results of the product. From these simulations they have derived the specifications for each building block.

The OTAs are central components in this system, as a lot of the specifications for the final product relies on OTA performance. Your group's analog designer already have a working folded cascode OTA which almost meets the spec, except for the offset voltage. This is not easily correctable in the layout because the required transitor sizing would be impractical and incur other unacceptable side effects.

At the next meeting, you suggest doing a digital calibration loop[1] for the OTA's offset voltage. The OTA's designer advice you that the trimming can be done easily by drawing a compensation current from the input-stage differential pair.

For this product, timing is not tight so you should have plenty of time for running the calibration. However, if you can make it faster, it will be much easier to apply to future products, without having to go through an expensive redesign.

1 Measuring the OTA performance

The existing OTA is available from `/hom/jorgenam/cadence_stm90/INF4420`. Use the library manager to add this path (Edit → Library path…). Using an ideal 100 fF capacitor as load, connect the OTA in a closed loop unity gain feedback, and measure the following:

- Gain-bandwidth product (GBW)
- Phase margin (PM)

If you like, you can also measure

- Noise
- Slew rate (how does this compare to the theory?)
- Output swing
- Settling behaviour
- Or other relevant parameters

[1] The workings of the calibration loop will be described later.

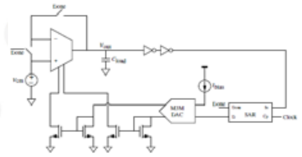

Figure 1: Digital trimming of the OTA's offset voltage (All NMOS are 0.5/0.5 μm)

Next, set up a testbench to find the variation in offset voltage. Use a montecarlo (MC) analysis with 100 runs.

- What is the standard deviation, σ, of the offset voltage?
- If we cover 6σ variation, how many percent of the manufactured OTAs will function to spec?
- What is the 6σ value?

Remembering that g_m is the transistor parameter that relates a change in gate voltage to a change in drain current, we can find the maximum required compensation current as $I_{bias} = 6\sigma \times g_m$. To find the g_m you can use an operating point analysis (remember to save operating point) and the results browser which you find under the tools-menu in ADE.

- What is the value of g_m of transistor M1 or M2 in the OTA?
- What is the value of I_{bias}?

2 Simulating the calibration loop

It's now time to simulate the entire calibration loop using the supplied components `OTA_trim`, `DAC_ideal`, and `SAR`. `OTA_trim` is the same as `OTA` but with an added current-mode trimming port. `DAC_ideal` is an ideal 7 bit D/A converter with radix 1.77 (sub-binary resolution).

If we run the OTA in open loop, an offset voltage will cause the output to rail (assuming sufficient gain). We can use this to detect if the offset voltage is too high or low. To properly buffer the output to a clean digital level, we can add inverters as buffers.

The DAC outputs a differential current approximately proportional to the input word (it does have some redundancy). This current is applied to the trimming port of

2

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INF4420 project 2009 (2/2)

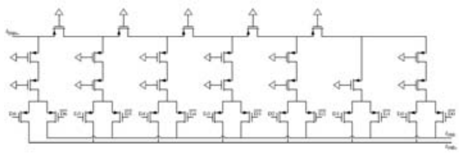

Figure 2: M3M DAC schematics (all PMOS are 0.5/0.2 μm)

the OTA through a current mirror. Thus, we now have a digital input for trimming the OTA's offset voltage. To find the suitable digital correction word, we will use a successive approximation register (SAR). The SAR tests each bit, starting at the MSB. If the OTA output swings above the common mode output voltage, the tested bit is cleared. After testing each bit, the SAR signals that it is done, and that normal system operation can resume. Thus, this signal can be used to switch the OTA between open loop and closed loop unity gain feedback.

- Simulate the system to verify its functionality
- What is the offset voltage after calibration?
- What is the σ of the offset voltage now?

Make a testbench and measure how the added trimming circuitry affect the performance of the OTA.

- Is the performance different compared to your previous measurements?
- What can be done to counter this?

3 DAC design

- Draw ideal transfer functions for a radix 2 converter and a radix 1.77 converter in the same plot.

Figure 3 depicts the schematics of a so called M3M DAC. The mosfets are all in the triode region.

- How does this structure compare to the more familiar R2R DAC?
- Make a testbench where you compare the transfer function of the ideal DAC with the M3M DAC.

3

Replace the ideal DAC in your calibration loop test bench with the M3M DAC.

- How does this affect the performance of the calibration loop?

Draw layout for the M3M DAC and the current mirror, remember to verify its correctness using DRC and LVS. Finally, do a parasitic extraction of the layout.

- Simulate the calibration loop with the extracted netlists.

4 Project requirements

The transistor sizing given in this document are reasonable guidelines to get you started. You are free to change this if neccessary.

Document everything, including but not limited to, all relevant schematics, layout, and simulation results. Discuss the choices you have made in designing and testing. Everything should be clear just from reading the documentation.

5 Deliverables

1. Do the first part of the project, described in Sect 1. Deadline March 19.
2. Do the second part of the project, described in Sect 2. Deadline April 2.
3. Finalize the project by completing the third and final part of the project, described in Sect 3, and write your final report. Deadline May 11.

In the first two deliverables, write a short report observing the guidelines in Sect 4. The final report must be comprehensive and document the entire project (i.e. include all deliverables). Only this final report will contribute towards your final grade. Please make all schematics and layout available for inspection.

JAM, February 12, 2009

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Cadence (http://www.cadence.com/)

- Widely used IC design tool worldwide, both in companies and academia
- Very large system
  - PCB-design
  - IC-design
    - Synthesis
    - Schematic entry
    - Simulator (Analog Environment / Spectre)
    - Layout (Virtouso)
- DRC and LVS performed by Calibre (Mentor)

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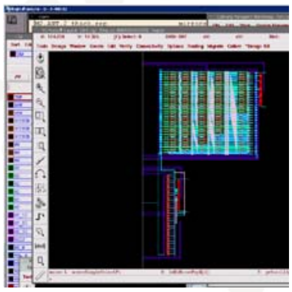
Full-custom ("handmade") design flow



- Design and calculation
  - Design equations
  - Dimensioning for matching
- Schematic entry
  - Simulations on cells and top level
  - Several interactions
- Layout
  - Module interface
  - Symmetry/hierarchy
  - Post Layout Simulations on critical modules
- Next module….

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Cadence forts.

- Start-up:
  - Web manual
- Standard libraries:
  - tsmcN90rf
  - analogLib
- Design views:
  - Symbol
  - Schematic
  - Layout

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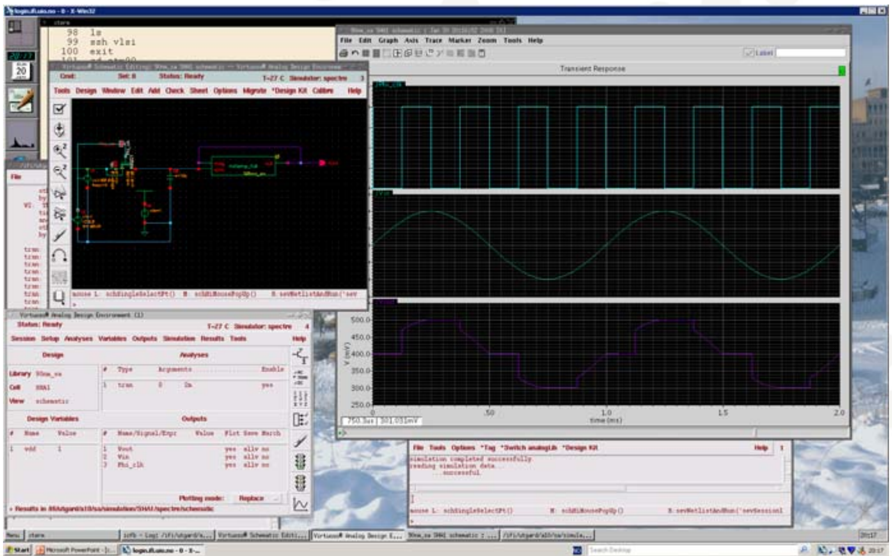
Schematic entry and simulations in Cadence



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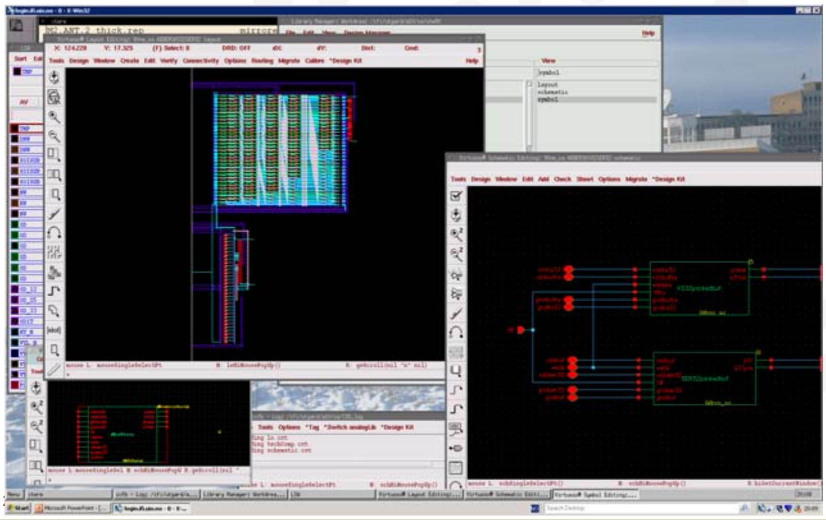
Symbol, schematic and layout (Cadence)



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Process

- TSMC 90 nm low power CMOS:
  - Minimum gate length: 90nm
  - 1 Poly-layer
  - 9 Metal-layers
  - True triple well
  - Three different threshold voltages
  - Supply voltage: 1.2 V typ.
  - Very advanced process

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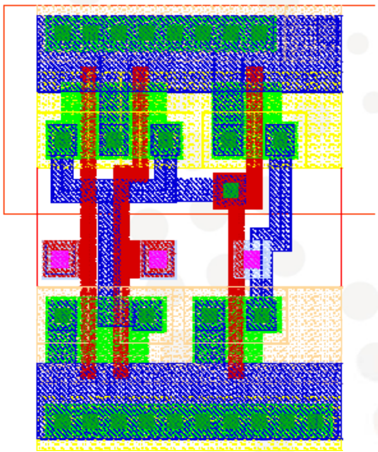
AND-gate



Challenges regarding the project

- Project administration
- Theoretical analysis and circuit design
- Design errors
  - LVS
- Parasitic components
  - Extraction and Post Layout Simulation (PLS)
- Process variations
  - Simulations (Corner + Monte-Carlo)
- Noise
  - Component and crosstalk
- Good layout practice / Symmetry

Practical information

- Lectures:
  - Tuesdays . 9.15 – 11.00 (should not collide with FYS3240).
  - From. 26/2: Tuesday . 9.15 – 12.00 (Might be 9:15 – 11:00 in most cases)
- Syllabus:
  - Johns and Martin: Analog Integrated Circuit design (Kap. 2, 8-14, 16. Not bipolar)
  - Selected additional material and lecture notes
  - LTH: Cadence 4.4
  - IFI: Lokal guide til Cadence
- Exercises
  - 2 hours per week – Time will be set next week. Amir Hasanbegovic, amirh@ifi.uio.no
- Projectsupervision/design lab
  - 2/4 hours each week – Time may be adjusted. Amir H., amirh@ifi.uio.no .
  - Room 3217 (?)
- Software:
  - Cadence 5.00 or 6.00 ((?))
  - TSMC 90 nm design kit
- Where to run the software:
  - Win PC running X-Win connected to Linux server /remote desktop and Linux
  - Linux computer
- Student reference group
  - 1-2 students

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What do we expect from you?

- The course is demanding
- Theoretical background
  - INF3410 analog microelectronics, or similar
  - FYS3220 linear circuit theory, or similar
  - INF3440 signal processing, or similar
- Prepare for the lectures
- Exercises
- Use the reference group and course evaluations to provide feedback

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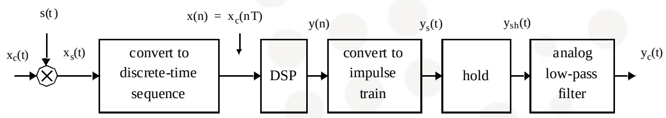
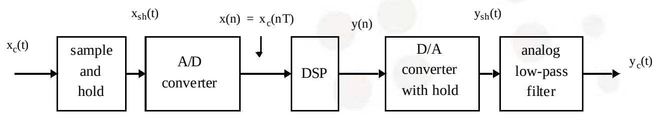
Final exam – a few words

- Thursday 3rd of June, starting 14:30 (3 hours)
- Problems usually related to every single of the relevant chapters in the book (2,8,9,…,14,16), and material from the lectures





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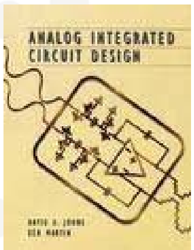
Syllabus; chapters 2,8,9,10,11,12,13,14,16



- Chapter 2 Processing and layout
- Chapter 8 Sample and Holds, Voltage references, and translinear circuits
- Chapter 9 Discrete-Time Signals
- Chapter 10 Switched-capacitor circuits
- Chapter 11 Data converter fundamentals
- Chapter 12 Nyquist-rate D/A converters
- Chapter 13 Nyquist-rate A/D converters
- Chapter 14 Oversampling converters
- Chapter 16 Phase-locked loops (in lectures, tuesdays)

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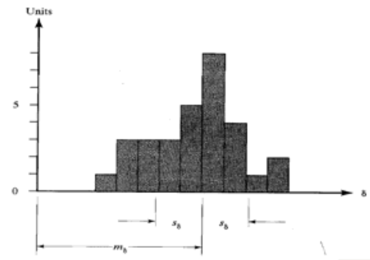
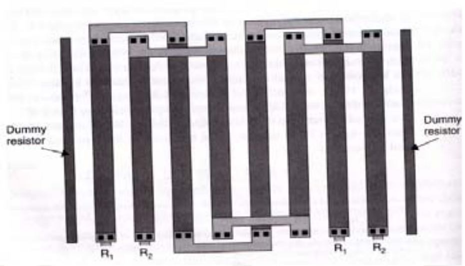
Syllabus; chapter 2





- CMOS processing
- Relative matching far better than absolute accuracy in CMOS
- CMOS layout and design rules
- ”*Matching is the Achilles heel of analog*” C. Diorio, Impinj / Washington State University
- A bad layout can ruin about any analog circuit.

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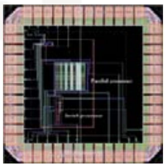
Chapter 8 Sample and Holds, Voltage References



- Performance of S/H
- S/H basics
- Bandgap voltage reference basics
- Circuits for bandgap references

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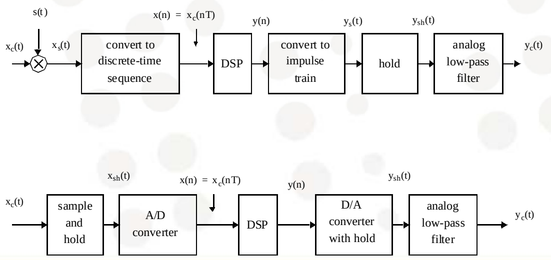
Chapter 9 Discrete-Time Signals

- Signal spectra
- Laplace transform of discrete-time signals
- Z-transform
- Downsampling and upsampling
- Discrete-time filters
- S/H response



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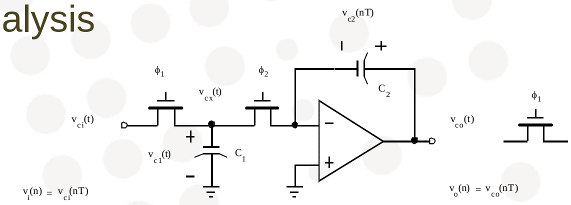
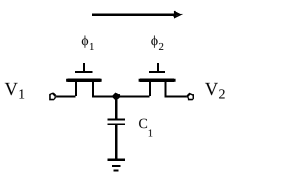
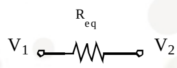
Chapter 10 Switched-Capacitor Circuits

- Building blocks
- Operation and analysis
- First-order filters
- Biquad filters







$\Delta Q = C_1(V_1 - V_2)$ every clock period

$R_{eq} = \frac{T}{C_1}$

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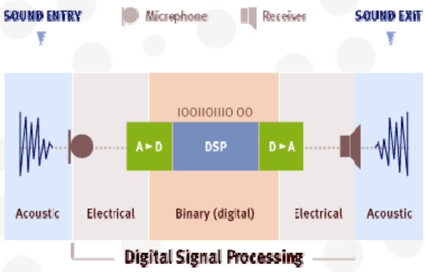
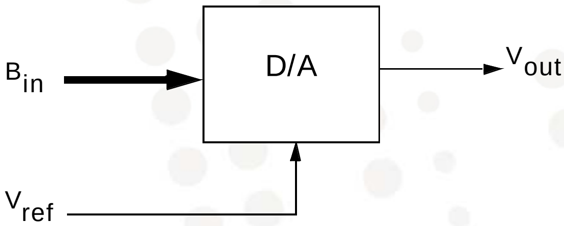
Chapter 11 Data converter fundamentals

- Ideal D/A and A/D
- Quantization noise
- Signed codes
- Performance limitations



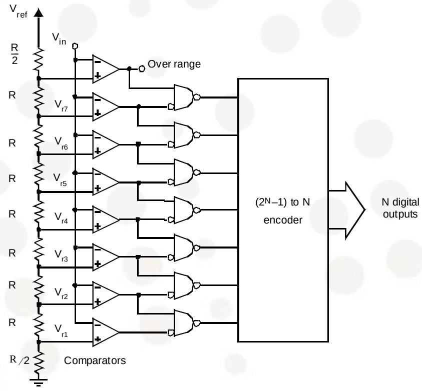
Chapter 12 Nyquist-Rate D/A Converters

- Decoder-based converters
- Binary-scaled converters
- Thermometer-code converters
- Hybrid conv.



Chapter 13 Nyquist-Rate A/D Converters

- Integrating converters
- Successive approx. converters
- Algorithmic converters
- Flash (parallell) conv.
- Two-step, interpolating,
- Folding, pipelined conv.



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Two consequences of the Nyquist-theorem and anti-aliasing filters (Wikipedia):

- If the highest frequency *B* in the original signal is known, the theorem gives the lower bound on the sampling frequency for which perfect reconstruction can be assured. This lower bound to the sampling frequency, 2*B*, is called the Nyquist rate.
- If instead the sampling frequency is known, the theorem gives us an upper bound for frequency components, $B<fs/2$, of the signal to allow for perfect reconstruction. This upper bound is the Nyquist frequency, denoted *fN*.
- An **anti-aliasing filter** is a filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. Since the theorem states that unambiguous interpretation of the signal from its samples is possible only when the power of frequencies outside the Nyquist bandwidth is zero, the anti-aliasing filter would have to have perfect stop-band rejection to completely satisfy the theorem. Every realizable anti-aliasing filter will permit some aliasing to occur; the amount of aliasing that does occur depends on how good the filter is.

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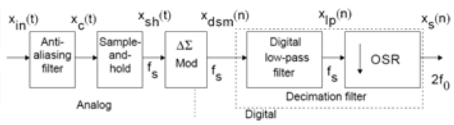
Chapter 14 Oversampling Converters

- Oversampling (>> 2 Nyquist bandwidth) relaxes requirements for matching
- High resolution, low to medium speed
- Noise shaping & oversampling
- N+1 order modulator gives a certain SNR for lower OSR
  than N-order mod.
- 24 bit Audio conv.



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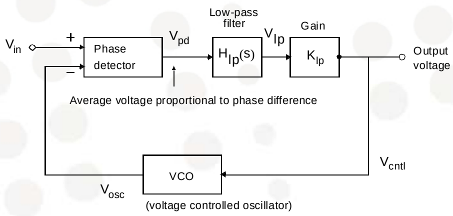
Chapter 16 Phase-locked loops

- Application examples:
- clock multiplication,
  - Freq. generation: The PLL output is a signal with frequency N times the input frequency where N may be a fractional number
  - FM demodulation (The input is a FM signal (IF) The output is the demodulated baseband signal
  - Products: TV and wireless



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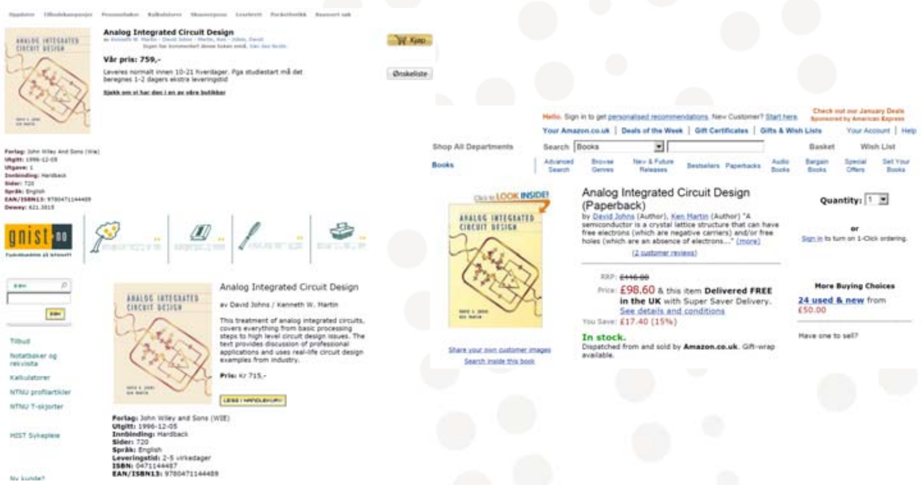
www.akademika.no / www.gnist.no / www.amazon.co.uk



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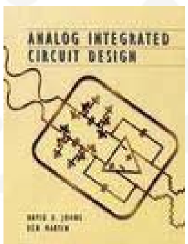
Next week:

- Sample and Hold circuits (chapter 8)
- Questions: sa@ifi.uio.no



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Sample and Hold Circuits (chapter 8)

Tuesday 2nd of February, 2010

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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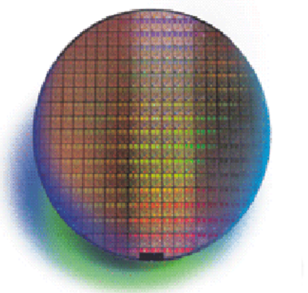
Last time – Tuesday 26th of January

- Practical issues
- Learning goals
- Design project, tools and methods
- Syllabus
- Very brief introduction to various circuit building blocks (sample-and-holds, bandgap references, switched capacitor circuits, nyquist- and oversampling data converters, phase-locked loops)



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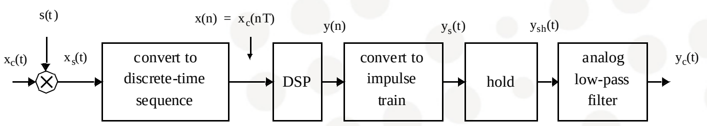
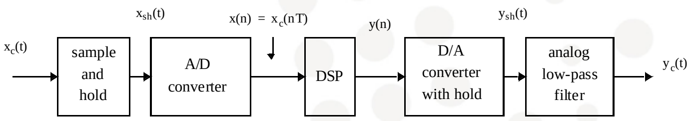
Sample and Holds (S/H) – What are the purposes?

- Mainly used in Analog-to-Digital Converters (ADC)
  - Samples analog input signal and holds value between clock cycles
  - Stable input value is required in many ADC-topologies
  - Reduces ADC-error caused by internal ADC delay variations
- Sometimes referred to as Track and Hold (T/H)
- Important parameters for S/H's
  - Hold step: Voltage error during S/H-transition
  - Signal isolation in hold mode
  - Input signal tracking speed in sample mode
  - Droop rate in hold mode: Small change in output voltage
  - Aperture jitter: Sampling time uncertainty

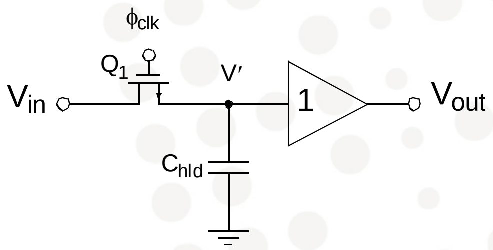
Overview of signal spectra – conceptual and physical realizations





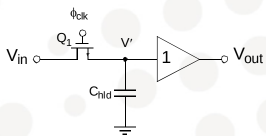
- An anti-aliasing filter (not shown) is assumed to band limit the continous time signal, $x_c(t)$.
- DSP ("discrete-time signal processing") may be accomplished using fully digital processing or discrete-time analog circuits (ex.: SC-circ.)

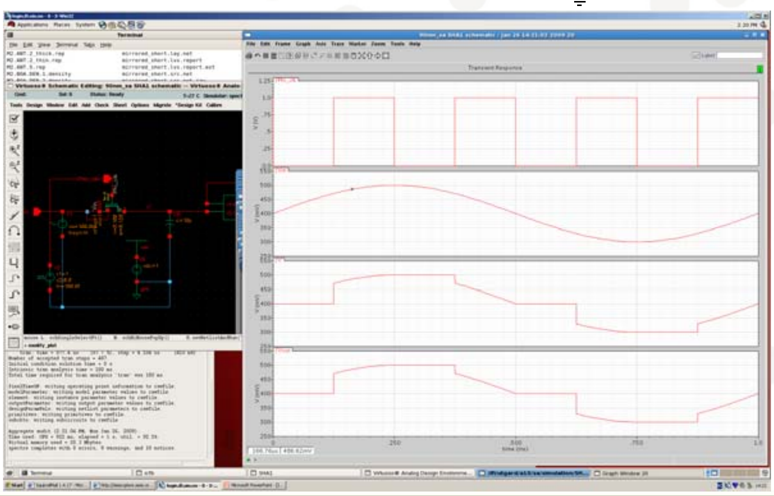
Basic S/H-topology



- Hold step:
  - Switch charge injection causes signal dependent hold step
- Aperture jitter:
  - Sampling-time variations causes signal dependent errors

Basic S/H-topology

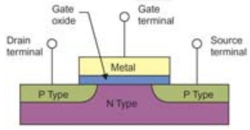




Charge injection due to channel capacitance

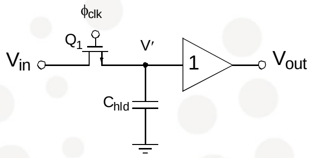
When ϕ_{clk} goes low, the channel charge of Q_1 is equally distributed between source and drain, leaving 50% of the charge across Chld:

$$\Delta Q_{C_{hld}} = \frac{Q_{CH}}{2} = \frac{C_{ox} W L V_{eff\text{-}1}}{2}$$



$$V_{eff\text{-}1} = V_{GS1} - V_{tn} = V_{DD} - V_{tn} - V_{in}$$

$$\Delta V' = \frac{\Delta Q_{C\text{-}hld}}{C_{hld}} = -\frac{C_{ox} W L (V_{DD} - V_{tn} - V_{in})}{2C_{hld}}$$

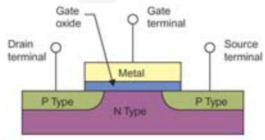


- $\Delta V'$ is linearly related to V_{in}, resulting in a gain error for the S/H. There is also a linear relationship to Vtn, which is nonlinearly related to Vin (through Vsb) resulting in distortion for the overall S/H.

Charge injection due to the gate overlap capacitance:

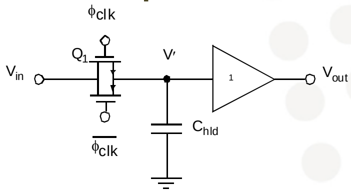
-

$$\Delta V' \cong -\frac{C_{ox} W L_{ov} (V_{DD} - V_{SS})}{C_{hld}}$$

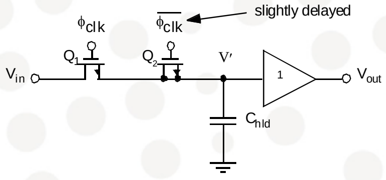


- (See eq. 7.8) This component is usually smaller than that due to the channel charge, and appears as an offset, since it's signal independent. Thus it may be removed in most systems.
- The clock signal should be relatively noise free, as the power-supply rejection of this S/H might be poor. (if for example clock signal comes from an inverter with common Vdd and Vss)

Hold step reduction



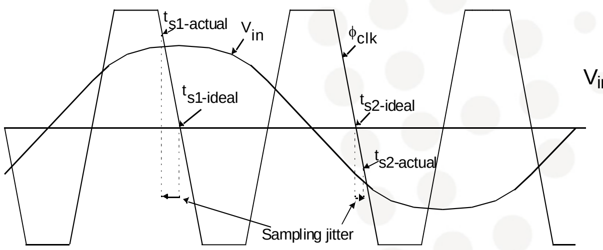
CMOS transmission gate

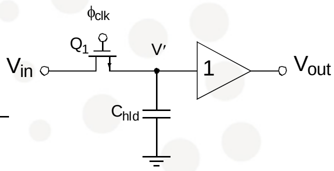


Dummy switch

- Transmission gate reduces charge injection since the charge carriers in the NMOS and PMOS have inversed polarity -> The negative charge from the NMOS cancels the positive charge from the PMOS
  - PMOS and NMOS are however hard to match in size, reducing the benefit.
- A NMOS dummy switch (S and D short-circuited) of half channel area clocked on inverted clock may be used to absorb charge
  - Hold step reduced by approximately 80%
  - The dummy switch clock must be slightly delayed to ensure that no charge leaks through Q1 while it is still open

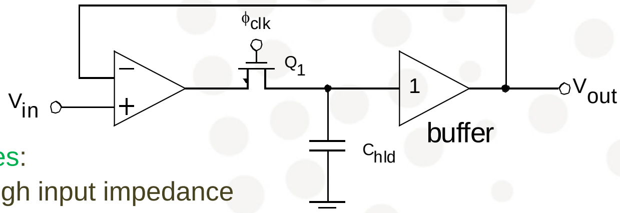
Aperture jitter





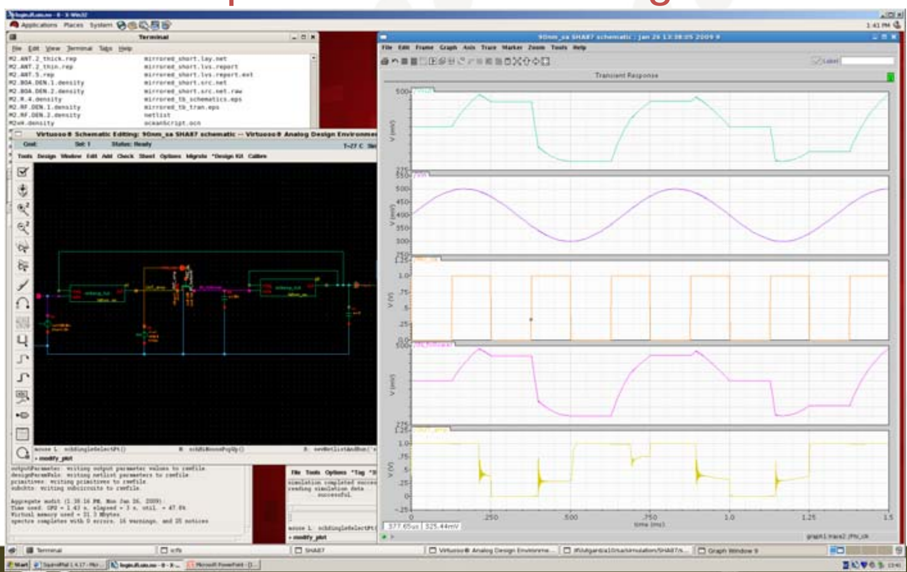
- If the input voltage is lower than the capacitor voltage, V_{in} is the source of the transistor used as a switch
- Vgs is then depending on V_{in}. For high values of V_{in}, the switch turns off too fast while for low values of V_{in} it turns off too late causing **distortion**

S/H (fig. 8.7)

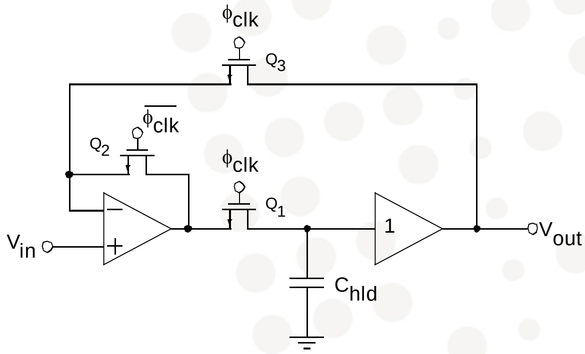


- Advantages:
  - High input impedance
  - Buffer offset voltage is divided by the gain of the input opamp, due to negative feedback. Simple voltage follower may be used at the output.
- Disadvantages:
  - Errors due to finite clock rise- and fall-times (PMOS and NMOS are not switched off at the same time)
  - Signal dependent charge injection -> Distortion
  - Feedback loop and need for stability limit maximum speed
  - In Hold mode, the first opamp output goes to either rail. Must slew back

Sample-and-Hold from fig. 8.7



Increased speed (fig. 8.8)



- During hold mode the opamp output is tracking the input
  - Leads to increased speed
- Disadvantages in common with the previous circuit

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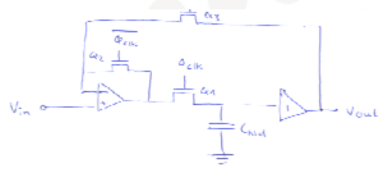
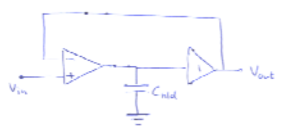
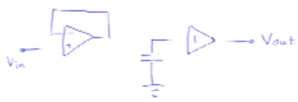
SAMPLE (= Track) / HOLD modes (fig 8.8)



TRACK (SAMPLE):



HOLD :



Q2 keeps the output of the 1st opamp close to the voltage it will need to be at when track (sample) mode is entered.

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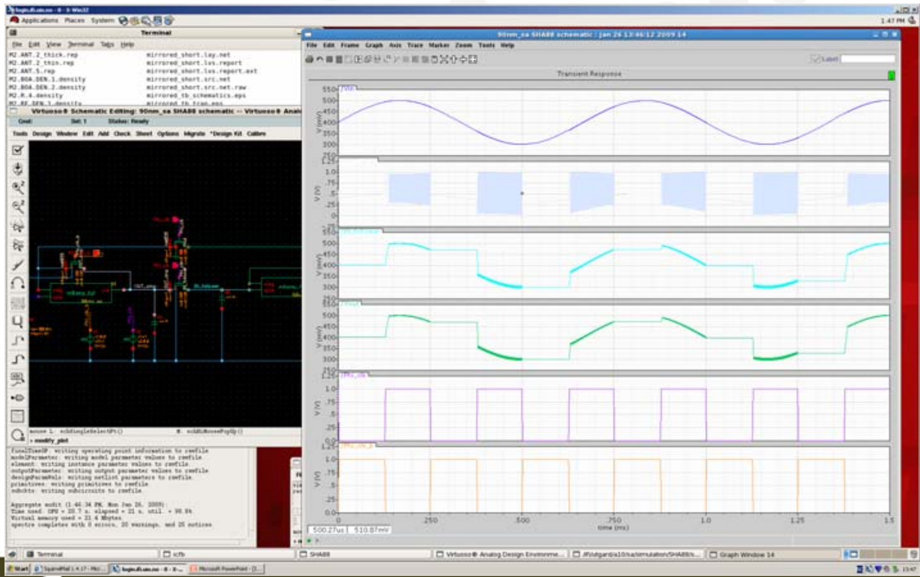
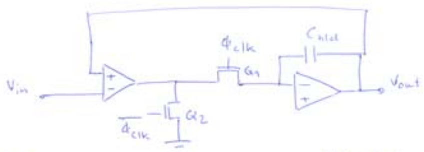
Sample-and-Hold from fig. 8.8

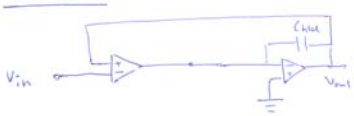


Another S/H: Fig 8.9 (Improved version of the S/H from fig. 8.8)

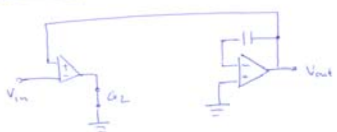
Fig. 8.9:



SAMPLE:

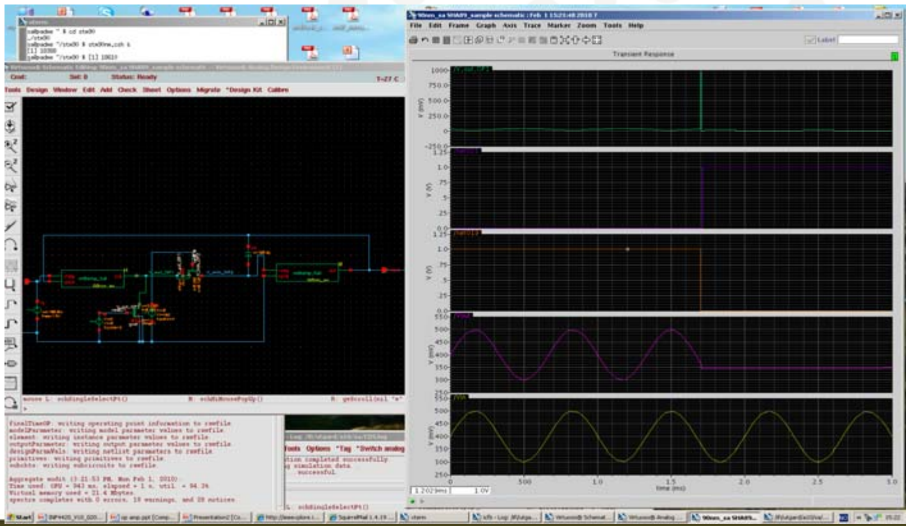


HOLD:



Q_2 grounds the output of OPAMP1 during HOLD.
Then the output is close to where it will be when changing to SAMPLE-/TRACK-

Sample (track) mode to Hold mode (the S/H in fig. 8.9) signals, from top: $V_{outopamp1}$, $V_{(Q2)}$, $V_{(Q1)}$, V_{out} , V_{in}



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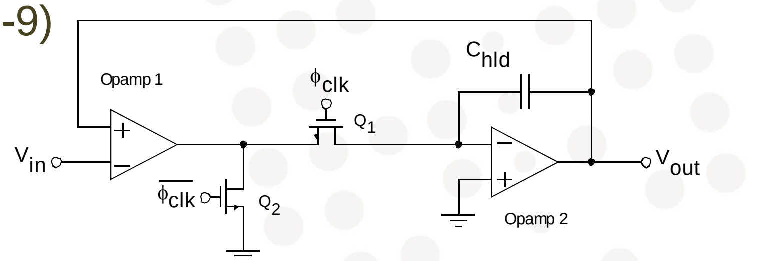
S/H with hold step independent of input signal (fig. 8-9)



+ : Both sides of Q_1 are nearly signal independent, so that the charge injection is (nearly) signal independent, provided a sufficient gain in the 2nd Opamp. The charge injection on C_{hld} causes the output of the 2nd Opamp to have a positive hold step, which is just a dc offset, with no signal distortion, and signal independent.

+: Sampling time will not change due to finite slopes of the sampling clock → less aperture jitter / aperture uncertainty → sample value closer to the ideal one.

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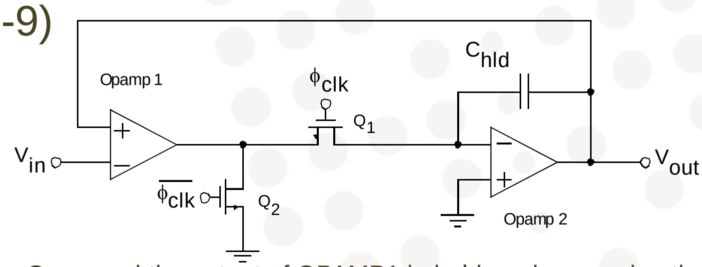
S/H with hold step independent of input signal (fig. 8-9)



+ : Q_2 ground the output of OPAMP1 in hold mode, meaning that it's close to (and quickly getting to) the voltage it should have in S. mode, which improves speed.

- Preventing instability reduces speed
- Worsened due to two opamps in the feedback loop

- More relevant information: K. R. Stafford, P. R. Gray, R. A. Blanchard: "A Complete Monolithic Sample/Hold Amplifier", IEEE Journal of Solid-State Circuits, Dec. 1974. (available from http://ieeexplore.ieee.org , when on UiO IP-address)

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"New(er) architecture"

FIGURE 9. Closed-Loop Architecture with Integrator Output

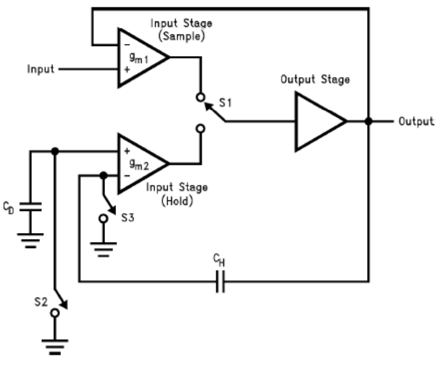

FIGURE 10. Current Multiplexed Architecture

A new architecture which combines the speed of the open-loop configuration and the accuracy of the closed-loop configuration is the current-multiplexed architecture shown in *Figure 10*. The LF6197, National's High Performance VIP™ Sample-and-Hold Amplifier used this architecture. This architecture provides for a cancellation of charge injection, allowing one to use a small hold capacitor to get high speeds without the disadvantage of a large hold step.

Specifications and Architectures of Sample-and-Hold Amplifiers

National Semiconductor
Application Note 775
July 1992

3. februar 2010 20

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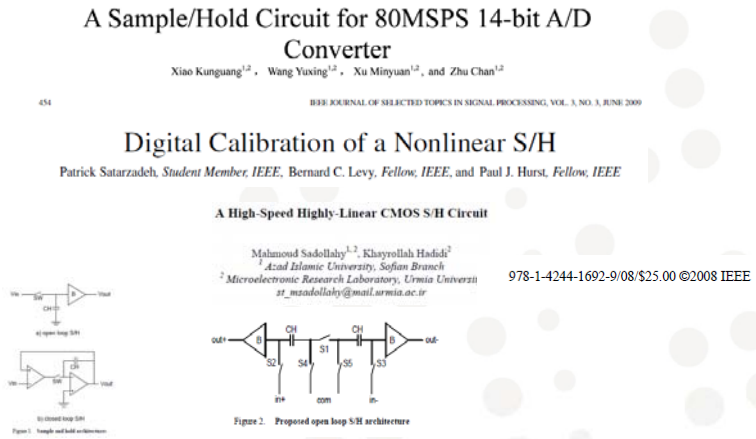
Continous efforts to improve S/H circuits..


A Sample/Hold Circuit for 80MSPS 14-bit A/D Converter

Xiao Kunguang[1,2], Wang Yuxing[1,2], Xu Minyuan[1,2], and Zhu Chan[1,2]

454 IEEE JOURNAL OF SELECTED TOPICS IN SIGNAL PROCESSING, VOL. 3, NO. 3, JUNE 2009

Digital Calibration of a Nonlinear S/H

Patrick Satarzadeh, *Student Member, IEEE*, Bernard C. Levy, *Fellow, IEEE*, and Paul J. Hurst, *Fellow, IEEE*

A High-Speed Highly-Linear CMOS S/H Circuit

Mahmoud Sadollahy[1,2], Khayrollah Hadidi[2]

[1] *Azad Islamic University, Sofian Branch*

[2] *Microelectronic Research Laboratory, Urmia Universi*

st_msadollahy@mail.urmia.ac.ir

978-1-4244-1692-9/08/$25.00 ©2008 IEEE

Figure 2. Proposed open loop S/H architecture

- IEEEXplore may provide State-of-the-Art solutions

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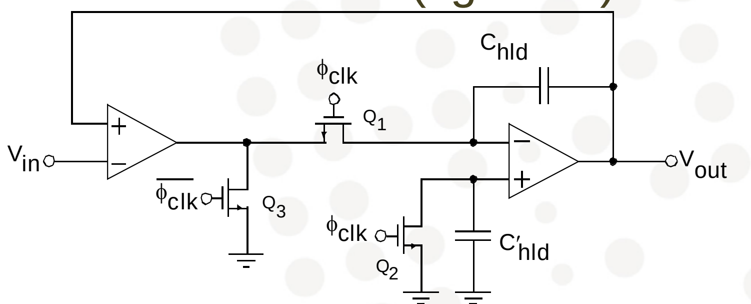
Reduced DC-error (fig. 8-10)



- Improved version of previous circuit (in fig. 8.9)
  - By placing a copy of Q1 and Chld in parallel between ground and the positive input of the second opamp, the voltage change due to charge injection will be equal on both inputs. Error is cancelled by opamp CMRR.
    The **common-mode rejection ratio** (CMRR) of a differential amplifier (or other device) measures the tendency of the device to reject input signals common to both input leads.

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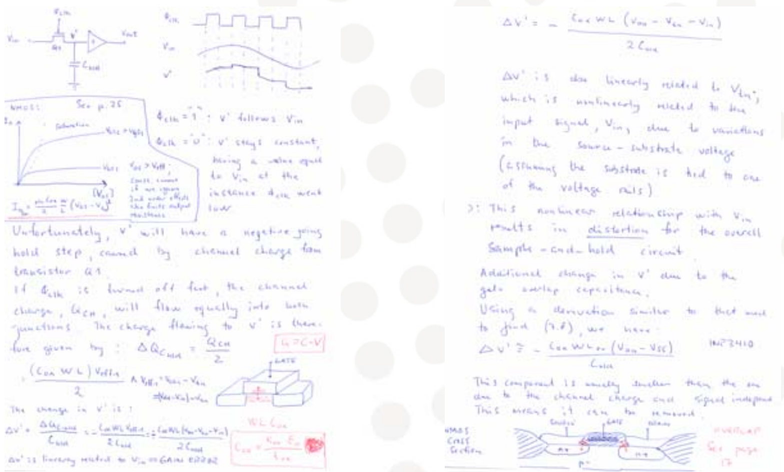
Additional Background Litterature, S/H circuits

- A. S. Sedra, K. C. Smith: "Microelectronic Circuits", Saunders College Publishing, 1991.
- R. Gregorian, G. C. Temes: "Analog MOS Integrated Circuits for signal processing", Wiley, 1986.
- K. R. Stafford, P. R. Gray, R. A. Blanchard: "A Complete Monolithic Sample/Hold Amplifier", IEEE Journal of Solid-State Circuits, Dec. 1974.
- F. F. Kuo:"Network Analysis and Synthesis", Wiley, 1966.
- S. Soma: "Grunnbok i elektronikk", Universitetsforlaget, 1979.
- National Semiconductor: "Specifcations and Architectures of Sample-and-Hold Architectures", App. Note 775, July 1992.
- S. Aunet: "BiCMOS Sample-and-Hold for Satelittkommunikasjon", hovedfagsoppgave, UiO, 1993.

S/H stuff..



Bandgap References and Discrete Time Signals (chapter 8 + 9)

Tuesday 9th of February, 2010

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Nanoelectronics Group, Dept. of Informatics
Office 3432

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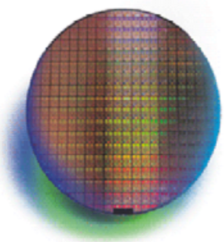
Last time – Tuesday 2nd of February, and today, February the 9th:

- 8.1 performance of Sample-and-Hold Circuits
- 8.2 MOS Sample-and-Hold circuits
- 8.3 Examples of CMOS S/H circuits
- 8.5 Bandgap Voltage Reference Basics
- 8.6 Circuits for Bandgap References
- Chapter 9 Discrete-Time Signals
- 9.1 Overview of some signal spectra
- 9.2 Laplace Transforms of Discrete-Time Signals
- 9.3 Z-transform



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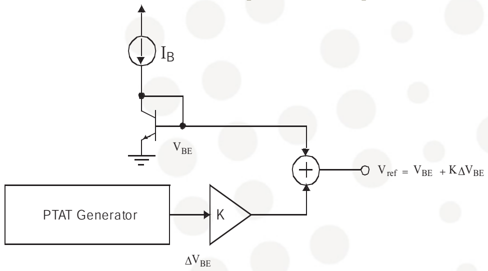
Voltage references (chapter 8.5)

- Purpose:
  - Generate a constant on-chip voltage which is independent of temperature, supply voltage, aging etc.
- Different approaches:
  - 1) Breakdown voltage of a reverse-biased zener diode
    - Too high voltage for CMOS
  - 2) Threshold voltage difference between CMOS enhancement and depletion transistors
    - Depletion-mode transistors unavailable in most CMOS processes
  - 3) Bandgap references: Canceling the negative temperature dependence of a forward-biased pn-junction (CTAT) with a positive temperature dependence (PTAT) (proportional-to-absolute-temperature) circuit
    - Most commonly used
    - CTAT: Conversely proportional to temperature
    - PTAT: Proportional to temperature

More about todays Bandgap Reference agenda (including, but not limited to):

- About the fundamental equations giving the relationship between the output voltage of a bandgap reference and temperature.
- How to design a bandgap reference for a ”most stable” reference voltage at a particular temperature.
- How to estimate temperature dependence at another temperature that the BG reference was designed for.
- Practical implementations

Basic principle



- The voltage V_{BE} is CTAT
- The voltage ΔV_{BE} is PTAT
- ΔV_{BE} is scaled by K to get the same slope as V_{BE}
- By adding V_{BE} and K ΔV_{BE}, the output V_{ref} becomes independent of temperature

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Bandgap reference example

A High Precision Curvature Compensated Bandgap Reference without Resistors

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A High Precision Curvature Compensated Bandgap Reference with
Jianghua Chen; Xuewen Ni; Bangxian Mo; Zhanfei Wang;
Solid-State and Integrated Circuit Technology, 2006. ICSICT '06. 8th Inte
23-26 Oct. 2006 Page(s):1748 - 1750
Digital Object Identifier 10.1109/ICSICT.2006.306414
AbstractPlus | Full Text: PDF(124 KB) IEEE CNF
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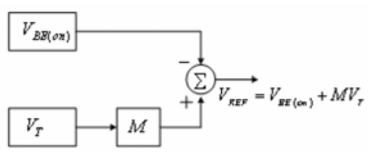

Figure 1 General bandgap reference architecture.

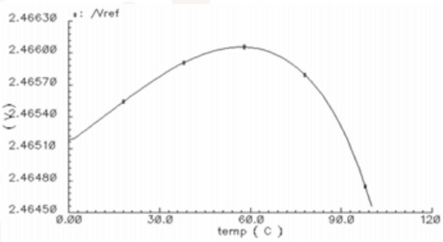

Figure 4 Output reference Verf vs. temperature.

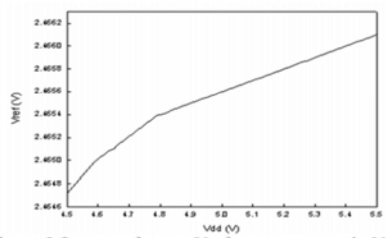

Figure 5 Output reference Vref vs. power supply Vdd.

9. februar 2010

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Theory

- Collector current

$$I_C = I_s e^{V_{BE}/((kT)/q)}$$

- Solved with respect to V_{BE}:

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_C}{J_{C0}}\right)$$

- The junction current equals the effective area of the base-emitter junction times the junction current density, Jc:

-

$$I_C = A_E J_C$$

The difference between two base-emitter junctions biased at different densities (proportional to temperature):

$$\Delta V_{BE} = V_2 - V_1 = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

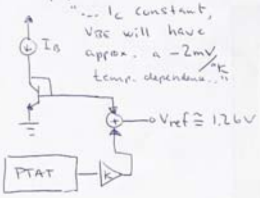
Example 8.3

Ex. 8.3 Assume two trans. biased at current-density ratio of 10:1 at 300 °K. What is the difference in their base-emitter voltages and what is its temperature dependence?

likn. 8.12 : $\underline{\Delta V_{BE}} = \frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$ ← eq. 8.12 p. 354

$$= \frac{1.38 \cdot 10^{-23}\,(300)}{1.602 \cdot 10^{-19}}\ln(10) = \underline{\underline{59.5\ mV}}$$

page 354:
"... I_C constant, V_{BE} will have approx. a $-2mV/°K$ temp. dependence..."



$$V_{ref} = V_{BE2} + K\,\Delta V_{BE}$$

Since this voltage is proportional to absolute temperature, after a 1°K temp. increase, the voltage difference will be $\Delta V_{BE} = 59.5\ mV \cdot \frac{301}{300} = 59.7 mV$

Thus, the voltage dependence is $59.5\ mV/300°K$ or $0.198\ mV/°K$.

Since the temperature dependence of a single V_{BE} is $-2mV/°K$, if it is desired to cancel the temp. dependence of a single V_{BE} then ΔV_{BE} should be amplified by about a factor of 10.

Theory

- Assuming that:

$$\frac{J_i}{J_{i0}} = \frac{T}{T_0}$$

- V_{ref} can then be written as:

$$V_{ref} = V_{BE2} + K\,\Delta V_{BE}$$
$$= V_{G0} + \frac{T}{T_0}(V_{BE0\text{-}2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

- For a given temperature V_{ref} may be independent of changes in the temperature if a proper vaule of K is assigned
- This (equation 8.16) is the fundamental equation giving the relationship between the output voltage of a bandgap voltage reference and temperature.

From V_{BE} as a function of collector current and temperature to Vout for BG ref. (part 1 of 2)

Pp 354–355

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{J_c}{J_{c0}}\right) \quad (8.10)$$

$\Updownarrow$ (using $\frac{J_i}{J_{i0}} = \frac{T}{T_0}$)

$$V_{BE} = V_{G0} - V_{G0}\frac{T}{T_0} + V_{BE0}\frac{T}{T_0} + \frac{mkT}{q}\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\ln\left(\frac{T}{T_0}\right)$$

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + \frac{mkT}{q}\left[\ln T_0 - \ln T\right] + \frac{kT}{q}\left[\ln T - \ln T_0\right]$$

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + \frac{mkT}{q}\ln T_0 - \frac{mkT}{q}\ln T + \frac{kT}{q}\ln T - \frac{kT}{q}\ln T_0$$

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + \frac{mkT}{q}\ln T_0 - \frac{mkT}{q}\ln T - \left(\frac{kT}{q}\ln T_0 - \frac{kT}{q}\ln T\right) \quad \boxed{\ln\left(\frac{a}{b}\right) = \ln a - \ln b = -\ln b + \ln a = -(\ln b - \ln a)}$$

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + \frac{mkT}{q}\ln T_0 - \frac{mkT}{q}\ln T - \frac{kT}{q}\ln\frac{T_0}{T}$$

OBS! "Unneccessary rewriting from 2nd to 3rd eq.

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + \frac{mkT}{q}\ln\frac{T_0}{T} - \frac{kT}{q}\ln\frac{T_0}{T}$$

$\Updownarrow$

$$V_{BE} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + (m-1)\frac{kT}{q}\ln\frac{T_0}{T}$$

$\Rightarrow$ SIMILAR TO ALL BUT LAST PART OF EQ 8.16.

From V_{BE} as a function of collector current and temperature to Vout for BG ref. (part 2 (of 2))

8.16 $\quad V_{ref} = V_{BE2} + K\,\Delta V_{BE}$

$$= V_{G0} + \frac{T}{T_0}\left(V_{BE0\text{-}2} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) \quad (8.16)$$

$$+ K\left[\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)\right] \quad (\text{using } 8.12)$$

This equation (8.16) is the fundamental equation giving the relationship between the output voltage of a bandgap reference and temperature.

Differentiating eq. 8.16 with respect to temperature, getting eq. 8.17

$$\left[V_{G0} + \frac{T}{T_0}\left(V_{BE0\text{-}2} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)\right]'$$

$$\boxed{\begin{array}{l} y = u+v,\ y' = u'+v' \\ y = uv,\ y' = u'v + uv' \\ y = \ln x,\ y' = \frac{1}{x} \end{array}}$$

$$= \cancel{(V_{G0})'} + \left(\frac{T}{T_0}\right)'\left(V_{BE0\text{-}2} - V_{G0}\right) + \cancel{\frac{T}{T_0}\left(V_{BE0\text{-}2} - V_{G0}\right)'} + \cancel{(m-1)'\left[\frac{kT}{q}\ln\left(\frac{T_0}{T}\right)\right]} + (m-1)\left[\frac{kT}{q}\ln\left(\frac{T_0}{T}\right)\right]'$$

$$+ \left(K\frac{kT}{q}\right)'\ln\left(\frac{J_2}{J_1}\right) + \cancel{K\frac{kT}{q}\left(\ln\left(\frac{J_2}{J_1}\right)\right)'}$$

$$\frac{\partial V_{ref}}{\partial T} = \left(\frac{T}{T_0}\right)'\left(V_{BE0\text{-}2} - V_{G0}\right) + \underbrace{(m-1)\left[\frac{kT}{q}\ln\left(\frac{T_0}{T}\right)\right]'}_{A} + \underbrace{\left(K\frac{kT}{q}\right)' \cdot \ln\left(\frac{J_2}{J_1}\right)}_{B}$$

Noen mellomregninger:

$$\left(\frac{T}{T_0}\right)' = \left(T \cdot \frac{1}{T_0}\right)' = 1 \cdot \frac{1}{T_0} + T \cdot 0 = \frac{1}{T_0}$$

$$y = \ln\frac{T_0}{T} = \ln T_0 - \ln T$$

$$y' = (\ln T_0)' - (\ln T)' = -\frac{1}{T}$$

$$\underline{A} = (m-1)\cdot\left(\frac{kT}{q}\right)'\cdot\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\left(\ln\frac{T_0}{T}\right)' = (m-1)\frac{k}{q}\cdot\ln\left(\frac{T_0}{T}\right) + \frac{kT}{q}\left(-\frac{1}{T}\right) = (m-1)\frac{k}{q}\cdot\ln\left(\frac{T_0}{T}\right) - \frac{k}{q}$$

$$= \underline{(m-1)\frac{k}{q}\left(\ln\left(\frac{T_0}{T}\right) - 1\right)}$$

$$B = \left[\left(K\frac{k}{q}\right)'\cdot T + K\frac{k}{q}\cdot T'\right]\cdot\ln\left(\frac{J_2}{J_1}\right) = K\frac{k}{q}\cdot\ln\left(\frac{J_2}{J_1}\right)$$

$$\Rightarrow: \quad \frac{\partial V_{ref}}{\partial T} = \frac{1}{T_0}\left(V_{BE0\text{-}2} - V_{G0}\right) + K\frac{k}{q}\cdot\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\left[\ln\left(\frac{T_0}{T}\right) - 1\right] \quad \text{eq. } 8.18$$

Setting equation 8.17 = 0, and T = T_0 getting eq. 8.18, giving the needs for zero temperature dependence at the reference temp.

Setter $\frac{\partial V_{ref}}{\partial T} = 0 \quad \wedge \quad T = T_0$ $\boxed{\ln 1 = 0}$

$$0 = \frac{1}{T_0}(V_{BE0-2} - V_{G0}) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}\left[\ln\left(\frac{T_0}{T_0}\right) - 1\right]$$

$$\Updownarrow$$

$$0 = \frac{1}{T_0}(V_{BE0-2} - V_{G0}) + K\frac{k}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{k}{q}(-1)$$

$$\Updownarrow$$

$$0 = (V_{BE0-2} - V_{G0}) + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right) + (m-1)\frac{kT_0}{q}(-1)$$

$$\Updownarrow$$

$$V_{BE0-2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right) = V_{G0} - (m-1)\frac{kT_0}{q}(-1)$$

$$\Updownarrow$$

$$V_{BE0-2} + K\frac{k}{q}T_0\ln\left(\frac{J_2}{J_1}\right) = V_{G0} + (m-1)\frac{kT_0}{q} \qquad (8.18)$$

Setting T=T_0 in eq. 8.16 gives the left side of eq. 8.18

8.16 : $V_{ref} = V_{BE2} + K\Delta V_{BE}$

$$= V_{G0} + \frac{T}{T_0}(V_{BE0-2} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T_0}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right)$$

Letting $T = T_0$:

$$V_{ref} = V_{G0} + \frac{T_0}{T_0}(V_{BE0-2} - V_{G0}) + (m-1)\frac{kT_0}{q}\ln\left(\frac{T_0}{T_0}\right) + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)$$

$$= V_{G0} + (V_{BE0-2} - V_{G0}) + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)$$

$$= \underline{V_{BE0-2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)}$$

For $T = T_0$, the left side of eq 8.18 equals the result above.

8.18 : $\underline{V_{BE0-2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)} = V_{G0} + (m-1)\frac{kT_0}{q}$

For zero temperature dependence at T=T0. At 300 K (8.18, 8.19, 8.20):

$$V_{BE0-2} + K\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right) = V_{G0} + (m-1)\frac{kT_0}{q} \qquad (8.18)$$

$[°C] = [K] - 273.15$

$300[K] - 273.15[K]$

$\approx 27\,°C$

The left side of eq 8.18 is the output voltage V_{ref} at $T = T_0$ (as we have shown).

For zero temperature dependence at $T = T_0$, we need

$$V_{ref-0} = V_{G0} + (m-1)\frac{kT_0}{q} \qquad (8.19)$$

For the special case of $T_0 = 300\,K$ and $m = 2.3$ (8.19) implies that, for zero temperature dependence

$$V_{ref-0} = V_{G0} = 1{,}206\,V + (2.3-1)\cdot\frac{1.38\times10^{-23}(300)}{1.602\times10^{-19}}$$

$$= 1.206\,V + 1.3\times25.8\,mV$$

$$\underline{= 1.24\ V}$$

Note that this value is independent of the current densities chosen.

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Required value for K at 300K (eq. 8.21):

From eq (8.20) we got $V_{ref-0} = 1{,}24\ V$ for zero temp. dependence at 300 °K. This value is independent of the current densities chosen.

K from equation 8.18:

$$K = \frac{V_{G0} + (m-1)\frac{kT_0}{q} - V_{BE0-2}}{\frac{kT_0}{q}\ln\left(\frac{J_2}{J_1}\right)} = \frac{1.24\,V - V_{BE0-2}}{25.8\,mV\cdot\ln\left(\frac{J_2}{J_1}\right)}$$

The output of a bandgap reference is given by the bandgap voltage, V_{G0}, plus a small correction to account for 2nd-order effects.

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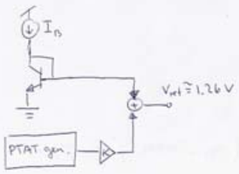
Output voltage for temperatures different from the reference; get (8.22) and then differentiate …

The fundamental equation giving the relationship between the output voltage of a bandgap reference and temperature is equation 8.16, page 355:

$$\boxed{\begin{aligned} V_{ref} &= V_{BE2} + K\,\Delta V_{BE} \\ &= V_{G0} + \frac{T}{T_0}\left(V_{BE0-2} - V_{G0}\right) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + K\frac{kT}{q}\ln\left(\frac{J_2}{J_1}\right) \end{aligned}}$$



The output voltage of the reference for temperatures different from the reference is found after backsubstituting (8.18) and (8.19) into (8.16) and some manipulation:

$$V_{ref} = V_{G0} + (m-1)\frac{kT}{q}\left[1 + \ln\left(\frac{T_0}{T}\right)\right] \quad (8.22)$$

(8.22) differentiated with respect to T, getting (8.23):

Differentiating 8.22: $\boxed{\log_a\left(\frac{u}{v}\right) = \log_a u - \log_a v}$ $\boxed{\begin{array}{l} y = uv \\ y' = u'v + uv' \end{array}}$ $\boxed{\begin{array}{l} y = \ln x \\ y' = \frac{1}{x} \end{array}}$

$$\underline{\frac{\partial V_{ref}}{\partial T}} = (V_{G0})' + \underbrace{\left[(m-1)\frac{kT}{q}\right]'}_{u'}\underbrace{\left[1 + \ln\left(\frac{T_0}{T}\right)\right]}_{v} + \underbrace{(m-1)\frac{kT}{q}}_{u}\underbrace{\left[1 + \ln\left(\frac{T_0}{T}\right)\right]'}_{v'}$$

$$= (m-1)\frac{k}{q}\left[1 + \ln\left(\frac{T_0}{T}\right)\right] + (m-1)\frac{k\cancel{T}}{q}\cdot\left(\frac{-1}{\cancel{T}}\right)$$

$$= \text{———} \;\;\text{''}\;\; \text{———} + (-m+1)\frac{k}{q}$$

$$= \text{———} \;\;\text{''}\;\; \text{———} \div (m-1)\frac{k}{q}$$

$$= (m-1)\frac{k}{q}\left[\cancel{1} + \ln\left(\frac{T_0}{T}\right) - \cancel{1}\right] = \underline{(m-1)\frac{k}{q}\ln\left(\frac{T_0}{T}\right) \quad (8.23)}$$

Equations 8.22 and 8.23 may be used to estimate the temperature dependence at temperatures different from the reference temperature

Example 8.4

Ex. 8.4
p. 757

Estimate the temperature dependence at 0°C for a bandgap reference that was designed to have zero temperature dependence at 20°C. Present the result as ppm/°K.

Using eq. 8.23 : $\frac{\partial V_{ref}}{\partial T} = (m-1)\frac{k}{q}\ln\left(\frac{T_0}{T}\right)$

°K corresponds to −273°C. $T_0 = 293°K$, $T = 273°K$

$$\frac{\partial V_{ref}}{\partial t} = (2.3-1)\frac{1.38\cdot10^{-23}}{1.6\cdot10^{-19}}\ln\left(\frac{293}{273}\right)\left[\mu V/°K\right] = \underline{8\ \mu V/°K}$$

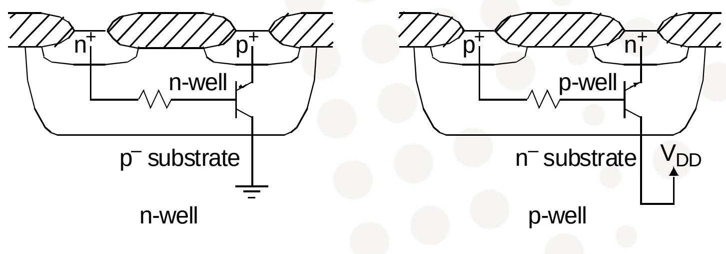
For a reference voltage of 1.24 V, a dependency of 8 µV/°K results in $\frac{8\mu V/°K}{1.24\,V} = 6.5\cdot10^{-6}$ parts/°K

$= \underline{6.5\ ppm/°K}$

"ppm": parts per million

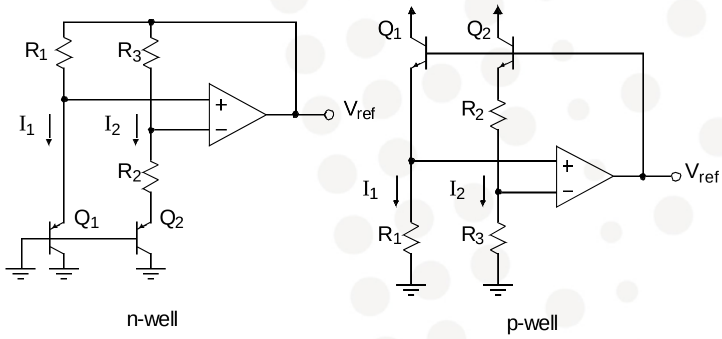
NB! Ideally: 0 ppm/°K, typically 4 - 10 × the value here..

CMOS Bandgap References



- Vertical CMOS well transistors in an n-well and p-well process (pnp in –well, npn in p-well)

CMOS BGR Circuits

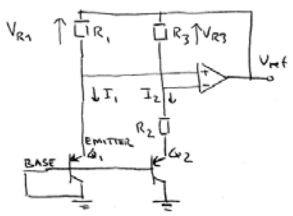


- CMOS bandgap references implemented with well transistors

Design equations, BG ref.

DESIGN EQUATIONS

Fig. 8.27



The voltage drop due to I_1:

$$V_{ref} = V_{EB1} + V_{R1} \quad (8.35)$$

Since $V_{R1} = V_{R3}$, assuming an ideal OP-AMP:

$$V_{R2} = V_{EB1} - V_{EB2} = \Delta V_{EB} \quad (8.36)$$

I_2 runs through both R_3 and R_2, so that

$$(8.37) \quad V_{R3} = \frac{R_3}{R_2} V_{R2} = \frac{R_3}{R_2} \cdot \Delta V_{EB} \quad (V_{R2} = \Delta V_{EB})$$

Substituting (8.37) into (8.35):

$$V_{ref} = V_{EB1} + V_{R1} = V_{EB1} + V_{R3} = V_{EB1} + \frac{R_3}{R_2} \Delta V_{EB} \quad (8.38)$$

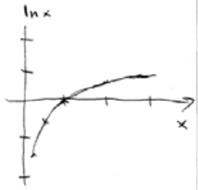
In integrated realizations the bipolar transistors are often taken the same size, and different current densities are realized by taking $R_3 > R_1$, causing $I_1 > I_2$. In this case

$$\cancel{\frac{I_1}{I_2}} \quad \frac{J_1}{J_2} = \frac{R_3}{R_1} \quad (8.39)$$

ln x

x	0,2	0,5	0	1	2	e
ln x	-1,61	-0,69	invalid	0	0,69	1

ln x



Recalling from 8.12 that $\Delta V_{EB} = V_{EB1} - V_{EB2} = \frac{kT}{q} \ln \frac{J_2}{J_2}$ (8.40)

(8.39) into (8.38): $V_{ref} = V_{EB1} + \frac{R_3}{R_2} \frac{kT}{q} \ln\left(\frac{R_3}{R_1}\right)$. $K = \frac{R_3}{R_2}$ (8.42)

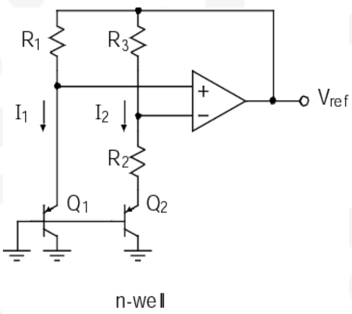
Design Equations

$$V_{ref} = V_{EB1} + V_{R1}$$

$$V_{R2} = V_{EB1} - V_{EB2} = \Delta V_{EB}$$

$$V_{R3} = \frac{R_3}{R_2} V_{R2} = \frac{R_3}{R_2} \Delta V_{EB}$$

$$V_{ref} = V_{EB1} + \frac{R_3}{R_2} \Delta V_{EB}$$



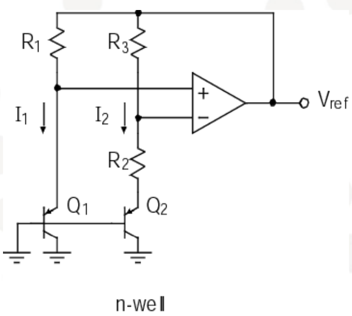
Design Equations

$$\frac{J_1}{J_2} = \frac{R_3}{R_1}$$

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = \frac{kT}{q} \ln\left(\frac{J_1}{J_2}\right)$$

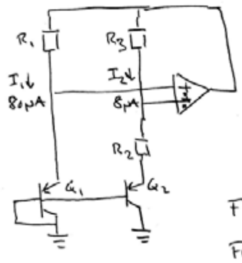
$$V_{ref} = V_{EB1} + \frac{R_3 kT}{R_2 q} \ln\left(\frac{R_3}{R_1}\right)$$

$$K = \frac{R_3}{R_2}$$



EXAMPLE 8.5

Find the resistances of a bandgap reference based on fig. 8.27 a), where $I_1 = 80\ \mu A$, $I_2 = 8\ \mu A$, and $V_{EB1-0} = 0.65V$ at $T = 300°K$



Assuming that the sizes of Q_1 and Q_2 are the same

$$\Delta V_{EB} = \frac{kT_0}{q} \ln \frac{I_1}{I_2} = \frac{kT_0}{q} \cdot 2.30259 = 59.4\ mV$$

$$R_2 = \frac{V_{R2}}{I_2} = \underline{\underline{7.44\ k\Omega}} = \frac{59.4\ mV}{8\mu A}$$

From (8.20) we know that $V_{ref-0} = 1.24\ V$ at $T_0 = 300°K$

From (8.35) we get $V_{R1} = V_{ref-0} - V_{EB1-0} = 1.24V - 0.65V$

$\Downarrow$

$V_{R1} = 0.59V$. $\underline{\underline{R_1}} = \frac{0.59V}{80\mu A} = \underline{\underline{7.38k\Omega}}$, $\underline{\underline{R_3}} = \frac{0.59V}{8\mu A} = \underline{\underline{73.8k\Omega}}$

Example 8.5 (2)

$V_{R2} = \Delta V_{EB} = \frac{kT}{q} \ln(10)$, since the sizes of Q_1 and Q_2 are assumed to be the same (equations 8.36 and 8.40)

$\Rightarrow$: $V_{R2} = \frac{1.38 \cdot 10^{-23}}{1.62 \cdot 10^{-19}} (300) \cdot \ln(10) = 59.5\ mV$ $\quad (V_{R2} = \Delta V_{EB})$

$U = RI \Leftrightarrow R = \frac{59.5\ mV}{8\mu A} = 7.44\ k\Omega$ $\quad \underline{R_2 = 7.44\ k\Omega}$

Remember from 8.20 that for 300°K and $m = 2.3$, (8.19) implies that $V_{ref-0} = V_{G0} + (m-1)\frac{kT_0}{q} = 1.24V$ $\quad (V_{G0} = 1.206V)$

Then we can get K from (8.21):

$$K = \frac{V_{G0} + (m-1)\frac{kT_0}{q} - V_{EB1-0}}{\frac{kT_0}{q}\ln\left(\frac{J_1}{J_2}\right)} = \frac{1.24\ V - 0.65\ V}{0.0258\ \ln(10)} = 9.93$$

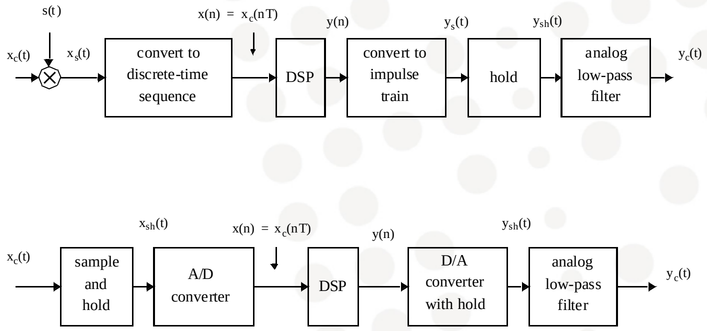
8.42 says that $K = \frac{R_3}{R_2} \Leftrightarrow \underline{R_3} = K \cdot R_2 = \underline{73.9\ k\Omega}$

8.39: $\frac{J_1}{J_2} = \frac{R_3}{R_1} \left(= \frac{I_1}{I_2}\right) \Leftrightarrow \frac{R_3}{R_1} = \frac{80\mu A}{8\mu A} \Leftrightarrow \underline{R_1} = \frac{R_3}{10} = \underline{7.39\ k\Omega}$

Chapetr 9; Discrete-time signals

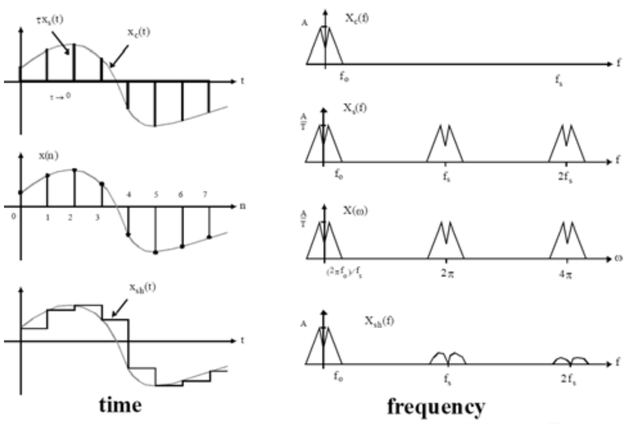
- Discrete-time signal processing is heavily used in the design and analysis of oversampling A/D and D/A converters as well as switched capacitor filtering ;"SC-circuits".
- Switched Capacitor filters are classified as analog, since they use continous time analog values.

Overview of signal spectra – conceptual and physical realizations



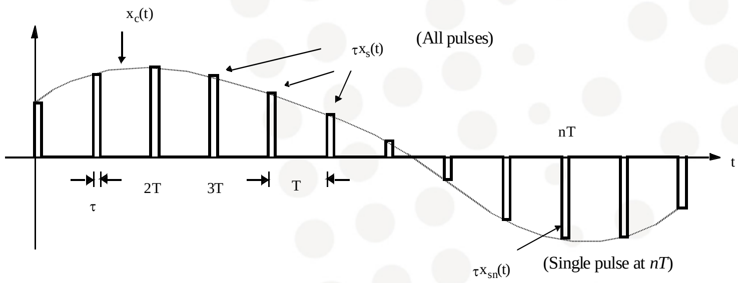
- An anti-aliasing filter (not shown) is assumed to band limit the continous time signal, $x_c(t)$.
- DSP ("discrete-time signal processing") may be accomplished using fully digital processing or discrete-time analog circuits (ex.: SC-circ.).

Signals in time, and frequency spectra



- S(t): periodic impulse train with period T (T=1/f_s)
- $x_s(t)$ has the same frequency spectrum as $x_c(t)$, but the baseband spectrum repeats every f_s (assuming no aliasing)
- x(n) has the same frequency spectrum as $x_c(t)$, but the sampling frequency is normalized to 1
- The frequency spectrum of $x_{sh}(t)$ is equal to that of $x_s(t)$ multiplied by the sin(x)/x response of the S/H.

Laplace Transform of Discrete-Time Signals (1/3)



- The signal must be defined for all time
- For t=nT:

$$x_s(nT) = \frac{x_c(nT)}{\tau}$$

- τ is chosen such that the area under $x_s(nT)$ equals the value of $x_c(nT)$
- As τ approaches 0, the height of $x_s(nT)$ goes to ∞

Laplace Transform of Discrete-Time Signals (2/3)

- A single pulse at t=nT may be defined as:

- $\vartheta(t)$ is the step function: $$\vartheta(t) \equiv \begin{cases} 1 & (t \geq 0) \\ 0 & (t < 0) \end{cases}$$

- $x_s(t)$ may then be rewritten as a linear combination of a series of pulses, xfs(t), where xsn(t) is zero everywhere except for a single pulse at nT:

$$x_{sn}(t) = \frac{x_c(nT)}{\tau}[\vartheta(t-nT) - \vartheta(t-nT-\tau)]$$

$x_s(t)$ is now defined for all time: $$x_s(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t)$$

Laplace Transform of Discrete-Time Signals (3/3)

- The Laplace transform for $x_{sn}(t)$ is:

$$X_{sn}(s) = \frac{1}{\tau}\left(\frac{1-e^{-s\tau}}{s}\right)x_c(nT)e^{-snT}$$

- Since there is a linear relationship between $x_s(t)$ and $x_{sn}(t)$, the Laplace transform of $x_s(t)$ is:

$$X_s(s) = \frac{1}{\tau}\left(\frac{1-e^{-s\tau}}{s}\right)\sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$$

- When τ approaches 0, the term before the sum equals 1 (eq. 9.7):

$$X_s(s) = \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$$

$$z \equiv e^{sT}$$

$$X(z) \equiv \sum_{n=-\infty}^{\infty} x_c(nT)z^{-n}$$

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Spectra of Discrete-Time Signals (1/2)

- The frequency spectrum of $x_s(t)$ may be found by replacing s by $j\omega$ in the Laplace transform (eq. 9.7).
- Another more intuitive approach is to use the property that multiplication in the time domain equals convolution in the frequency domain. Using this and $\tau \to 0$, Xs(t) can be rewritten

$$x_s(t) = x_c(t)s(t)$$

- Define a pulse-train:
- The sampled signal is now:

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

- The Fourier-transform of s(t) is:

$$S(j\omega) = \frac{2\pi}{T}\sum_{k=-\infty}^{\infty}\delta\left(\omega - k\frac{2\pi}{T}\right)$$

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Spectra of Discrete-Time Signals (2/2)

- Writing (9.8) in the frequency domain:

$$X_s(j\omega) = \frac{1}{2\pi} X_c(j\omega) \otimes S(j\omega)$$

- The frequency spectrum of $x_s(t)$ is then (eq. 9.12):

$$X_s(j\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X_c\left(j\omega - \frac{jk2\pi}{T}\right)$$

which is periodic with period f_s (9.13:).

No aliasing occurs if f<fs/2

$$X_s(f) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X_c(j2\pi f - jk2\pi f_s)$$

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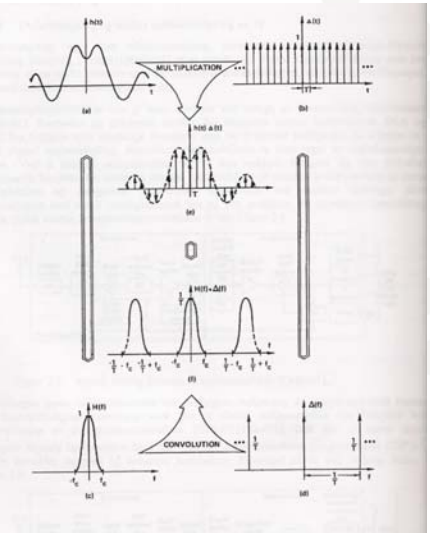
Multiplication in the time domain equals convolution in the frequency domain



Figur 2.7: Sammenhengen mellom sampling i tids- og frekvensdomenet. Produktet av h(t), figur 2.7 a), og Δ(t), i figur b), er lik den samplede kurveformen i figur c). Fouriertransformene av h(t) og Δ(t) er gitt i henholdsvis figur 2.7 c) og d). Frekvenskonvolusjonsteoremet er illustrert ved at Fouriertransformen av h(t)*Δ(t) er lik h(t)Δ(t) [Brig74].

- Figure from E. O. Brigham: "The Fast Fourier Transform", Prentice Hall Inc., 1974., in S. Aunet: "BiCMOS sample-and-hold for satellitt-kommunikasjon", Cand. Scient. Thesis, University of Oslo, 1993.

- Wikipedia; Convolution:
- In mathematics and, in particular, functional analysis, **convolution** is a mathematical operation on two functions *f* and *g*, producing a third function that is typically viewed as a modified version of one of the original functions. Convolution is similar to cross-correlation.
- Computing the inverse of the convolution operation is known as deconvolution.

- In mathematics, the **Fourier transform** (often abbreviated **FT**) is an operation that transforms one complex-valued function of a real variable into another. In such applications as signal processing, the domain of the original function is typically time and is accordingly called the *time domain*. That of the new function is frequency, and so the Fourier transform is often called the *frequency domain representation* of the original function. It describes which frequencies are present in the original function.

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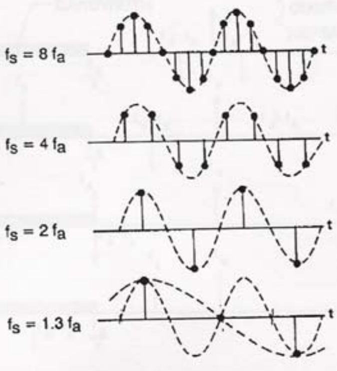
Sampling at different frequencies

2.2 Signaler i tids- og frekvensdomenet, for ulike samplingsfrekvenser



Figur 2.4: Sampling ved ulike frekvenser, sett i tidsdomenet. f_s er samplingsfrekvensen, også kalt samplingsraten, mens f_a er frekvensen for det analoge signalet som samples.[Kest91].

Aliasing and potential degrading of signal / noise

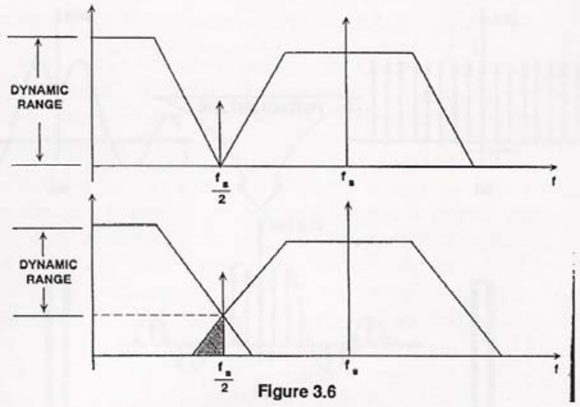


Figure 3.6

Figur 2.6: Aliasing og dynamisk område [Kest91] I det øverste tilfellet samples det slik at det dynamiske området beholdes. I det andre tilfellet overlapper frekvensspekterne slik at dynamisk område, eller signal/støy -forhold, reduseres.

Z-Transform

- Discrete-time systems are most often analyzed using the z-transform which is equivalent to the Laplace-transform with the following substitution:

- Then the z-transform is defined as :

$$z \equiv e^{sT}$$

$$X(z) \equiv \sum_{n=-\infty}^{\infty} x_c(nT) z^{-n}$$

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Z-Transform

- Two important properties of the z-transform:
  - 1) If $x(n) \leftrightarrow X(z)$, then $x(n-k) \leftrightarrow z^{-k} X(z)$
  - 2) Convolution in the time-domain is equal to multiplication in the freq. domain (If y(n)=h(n) $\otimes$ x(n), then Y(z) = H(z)X(z). Similarly, multiplication in the time-domain equals convolution in the frequency domain
  - X(z) is only related to the sampled sequence of numbers, while $X_s(s)$ is the Laplace transform of $x_s(t)$ when τ -> 0
  - The frequency response of $X_s(f)$ is related to $X(\omega)$ the following way: $X_s(f) = X(\frac{2\pi f}{f_s})$
  - Thus, the following scaling has been applied:

$$\omega = \frac{2\pi f}{f_s}$$

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Z-Transform

- Important observation:
  - Discrete-time signals have ω in units of radians/sample
  - The original continuous-time signal have frequency units of cycles/second (Hertz) or radians / second. (2 π Radians ~ 360 degrees)
- Example:
  - A continuous-time sinusoidal signal of 1kHz when sampled at 4 kHz will change by $\pi/2$ radians between each sample. In such case the discrete time signal is defined to have a frequency of $\pi/2$ radians per sample

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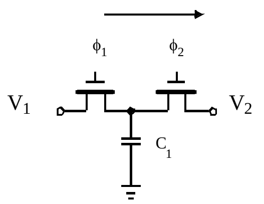
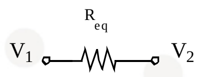
Next time, Tuesday 16th of February

- Chapter 9; 9.4 – 9.6
- Chapter 10; Switched Capacitor Circuits



$\Delta Q = C_1(V_1 - V_2)$ every clock period



$R_{eq} = \frac{T}{C_1}$

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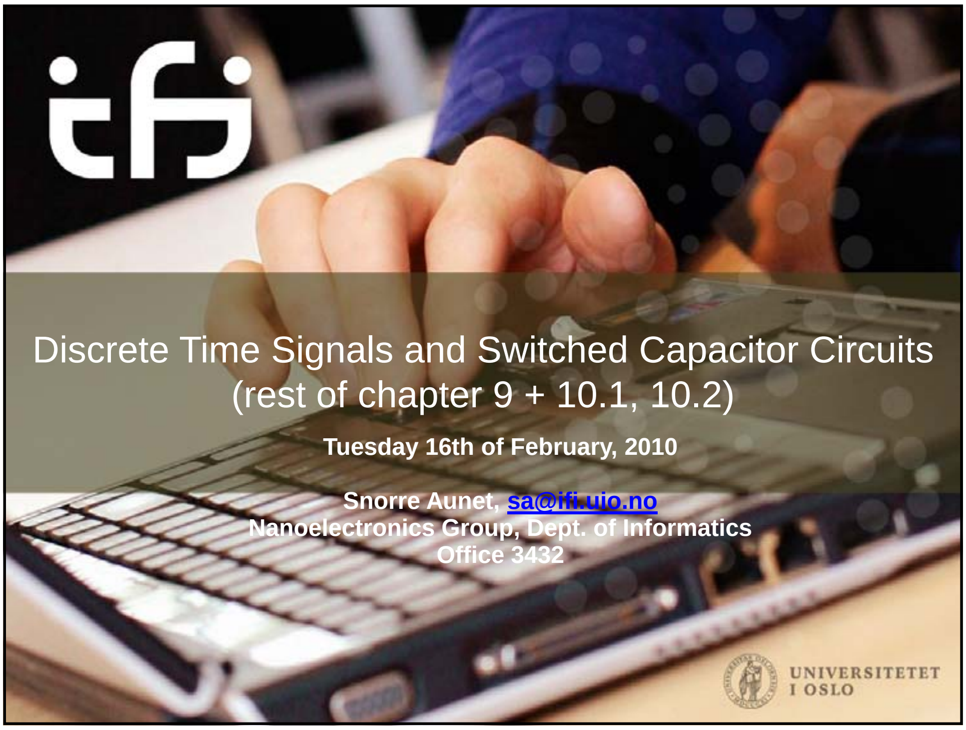

Discrete Time Signals and Switched Capacitor Circuits (rest of chapter 9 + 10.1, 10.2)

Tuesday 16th of February, 2010

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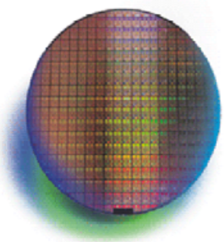
Last time – Tuesday 9th of February, and today, February the 16th:

- 8.5 Bandgap Voltage Reference Basics
- 8.6 Circuits for Bandgap References
- Chapter 9 Discrete-Time Signals
- 9.1 Overview of some signal spectra
- 9.2 Laplace Transforms of Discrete-Time Signals

- 9.2 -9.6
- 10.1-10.2 (10.3((?)))



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9.2 LAPLACE – TRANSFORM OF DISCRETE TIME SIGNALS

The sampled signal, $x_s(t)$ is related to the continuous – time signal, $x_c(t)$, as shown in Fig. 9.3.

Conceptual (See fig. 9.1)

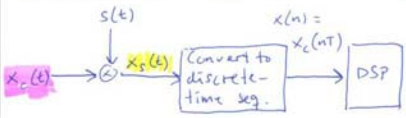
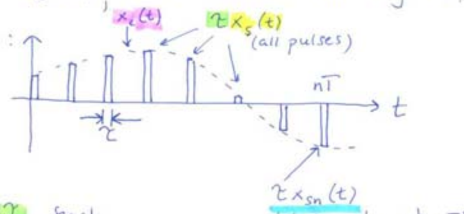


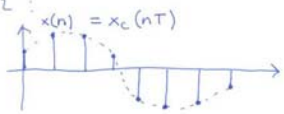
FIG. 9.3 :



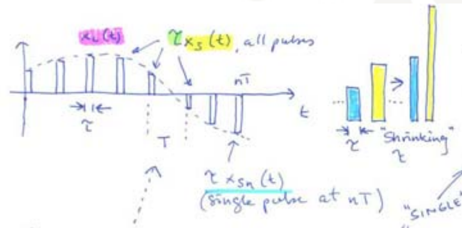
In Fig. 9.3 $x_s(t)$ is scaled by τ such that the area under the pulse equals the value of $x_c(nT)$.

At $t = nT$ we then have $x_s(nT) = \dfrac{x_c(nT)}{\tau}$ such that the area under the pulse, $\tau x_s(nT)$, equals $x_c(nT)$

Fig. 9.2 :



As $\tau \to 0$, the height of $x_s(t)$ at time nT goes to ∞



$\tau x_s(t)$ plotted

$\vartheta(t)$ is defined to be the step function given by

$$\vartheta(t) = \begin{cases} 1 & (t \geq 0) \\ 0 & (t < 0) \end{cases}$$

$x_s(t)$ can be represented as a linear combination of a series of pulses, $x_{sn}(t)$, where $x_{sn}(t)$ is zero everywhere except for a single pulse at nT.

The single-pulse signal, $x_{sn}(t)$, can be written

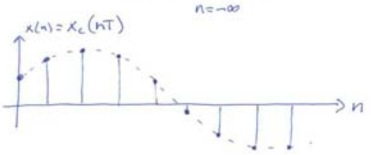
"SINGLE"

$$x_{sn}(t) = \frac{x_c(nT)}{\tau}\left[\vartheta(t-nT) - \vartheta(t-nT-\tau)\right]$$

so that we can now write $x_s(t)$ as

"ALL"

$$x_s(t) = \sum_{n=-\infty}^{\infty} x_{sn}(t)$$



These signals are defined for <u>all time</u> so that the LAPLACE – transform may be found ~~in~~ for $x_s(t)$ in terms of $x_c(t)$

Laplace transform $X_{sn}(s)$ for $x_{sn}(t)$:

$$X_{sn}(s) = \frac{1}{\tau}\left(\frac{1-e^{-s\tau}}{s}\right) x_c(nT)\,e^{-snT}$$

Since $x_s(t)$ is a linear combination of $x_{sn}(t)$, we also have

$$X_s(s) = \frac{1}{\tau}\left(\frac{1-e^{-s\tau}}{s}\right) \sum_{n=-\infty}^{\infty} x_c(nT)\,e^{-snT}$$

When $\tau \to 0$ the term before the summation goes to unity, so in this case:

(eq 9.7): $$X(s) = \sum_{n=-\infty}^{\infty} x_c(nT)\,e^{-snT}$$

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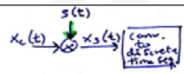
pp. 376

$\otimes$: convolution

SPECTRA OF DISCRETE-TIME SIGNALS



eq. 9.7: $$X_s(s) = \sum_{n=-\infty}^{\infty} x_c(nT)\,e^{-snT}$$

The spectrum of the sampled signal, $x_s(t)$, can be found by replacing s by $j\omega$ in (9.7).

A more intuitive approach is to recall that $\boxed{\text{if } y(n) = h(n) \otimes x(n), \text{ then } Y(z) = H(z)\cdot X(z)}$

Using this fact, for $\tau \to 0$, $x_s(t)$ can be written as the product

$$x_s(t) = x_c(t)\,s(t) \qquad (9.8)$$

where $s(t)$ is a periodic pulse train, or

$$s(t) = \sum_{n=-\infty}^{\infty} \delta(t-nT)$$

where $\delta(t)$ is the impulse function (DIRAC DELTA FUNC.)

It is well known that the Fourier transform of a periodic impulse train is another periodic impulse train:

(9.10) $$S(j\omega) = \frac{2\pi}{t} \sum_{k=-\infty}^{\infty} \delta\left(\omega - k\cdot\frac{2\pi}{T}\right)$$

(Spectrum of $s(t)$)

Writing (9.8) in the frequency d.:

(9.11): $$X_s(j\omega) = \frac{1}{2\pi} X_c(j\omega) \otimes S(j\omega)$$

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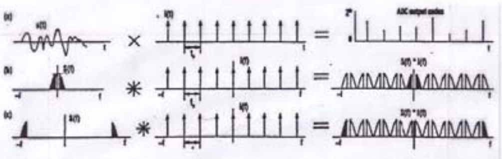
$X_s(j\omega) = \frac{1}{2\pi} X_c(j\omega) \otimes S(j\omega)$



Figur 2.10: Grafisk fremstilling av sampling, i tids- og frekvensdomenet.

By performing this convolution either mathematically or graphically, the spectrum of $X_s(j\omega)$ can be seen to be given by

$$X_s(j\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X_c\left(j\omega - \frac{jk2\pi}{T}\right) \quad (9.12)$$

or equivalently

$$X_s(f) = \frac{1}{T}\sum_{k=-\infty}^{\infty} X_c\left(j2\pi f - jk2\pi f_s\right) \quad (9.13)$$

9.12 and 9.13 show that the spectrum for the sampled signal, $x_s(t)$, equals a sum of shifted spectra of $x_c(t)$.
No aliasing occurs if $X_c(j\omega)$ is bandlimited to $\frac{f_s}{2}$

(9.13) confirms the example spectrum for $X_s(f)$, shown in Fig. 9.2.
Note that, for a discrete-time signal, $X_s(f) = X_s(f \pm kf_s)$, where k is an arbitrary integer as seen by substitution in (9.13).

9.3 Z-TRANSFORM pp 377 in "J&M"

(9.7): $X(s) = \sum_{n=-\infty}^{\infty} x_c(nT)\, e^{-snT} \quad \wedge \quad z \equiv e^{sT}$

(9.15) $X(z) \equiv \sum_{n=-\infty}^{\infty} x_c(nT)\, z^{-n}$; the z-transform of the samples $x_c(nT)$

TWO PROPERTIES, deduced from Laplace-tr. properties:

1) If $x(n) \Leftrightarrow X(z)$ then $x(n-k) \Leftrightarrow z^{-k}\cdot X(z)$
2) Conv. in the time domain equals mult. in the freq domain
Mult. — " — — " — Conv. — " —
If $y(n) = h(n) \otimes x(n)$ then $Y(z) = H(z)\cdot X(z)$

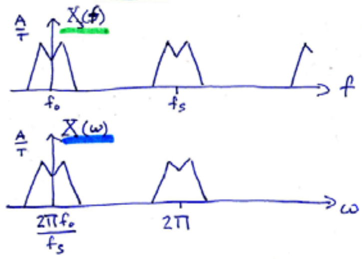
Note that $X(z)$ is not a function of the sampling rate but only to the numbers $x_c(nT)$.
The signal $x(n)$ is simply a series of numbers that may (or may not) have been obtained by sampling

"$x(n)$ is simply a series of numbers..." (pp. 377)

One way of thinking about this series of numbers is that the original sample time, T, has been effectively normalized to 1.

The scaling justifies the spectral relation between $X(s)(f)$ and $X(\omega)$ shown in Fig. 9.2

From fig. 9.2:



ω: radians/sample

Relationship between $X_s(f)$ and $X(\omega)$:

$$\cancel{X(s)} \quad X_s(f) = X\left(\frac{2\pi f}{f_s}\right) \quad (9.16)$$

Alternatively:

$$\omega = \frac{2\pi f}{f_s}$$

At Nyquist rate:

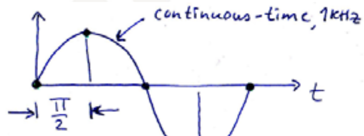
$$\omega = \frac{2\pi f}{f_s} = \frac{2\pi f}{2f} = \pi \left[\frac{\text{radians}}{\text{sample}}\right]$$

f: cycles/second (Hz)

ω: radians/sample

See fig. 9.4

Normally discrete-time signals are defined to have frequency components only between $-\pi$ and π $\frac{\text{rad.}}{\text{sample}}$

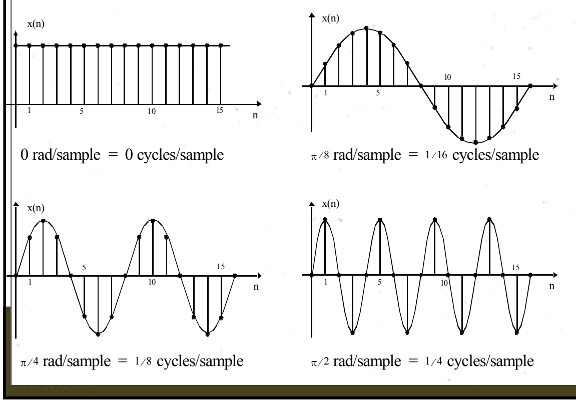


$f = 1\text{kHz}$, $f_s = 4\text{kHz}$

The signal changes $\frac{\pi}{2}$ radians between each sample

$\Rightarrow$ Such a discrete-time signal is defined to have a frequency of $\frac{\pi}{2}$ $\frac{\text{rad.}}{\text{sample}}$

Note: Discrete-time signals are not unique since addition of 2π results in the same signal. (For example, a discrete-time signal having a freq. of $\frac{\pi}{4}$ $\frac{\text{rad.}}{\text{sam.}}$ is identical to that of $\frac{9\pi}{4}$ $\frac{\text{rad.}}{\text{sample}}$)



0 rad/sample = 0 cycles/sample

$\pi/8$ rad/sample = $1/16$ cycles/sample

$\pi/4$ rad/sample = $1/8$ cycles/sample

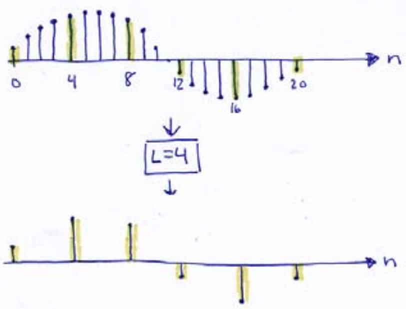
$\pi/2$ rad/sample = $1/4$ cycles/sample

9.4 DOWNSAMPLING AND UPSAMPLING

DOWNSAMPLING To reduce the sample rate (without inform. loss)

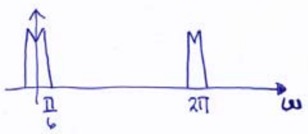
UPSAMPLING to increase — || —.

DOWNSAMPLING: achieved by keeping every Lth sample and discarding the others.

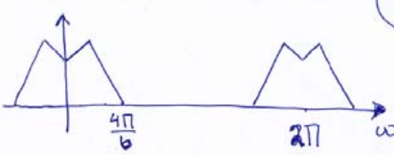


Noninteger rates can be achieved, but here L being integer is considered only.

FREQUENCY DOMAIN:



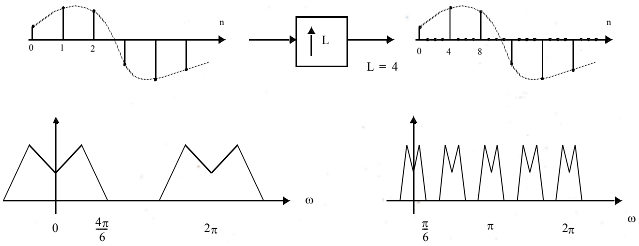
Original spectra expanded by L: (See fig. 9.6 pp. 379)



SIGNAL MUST BE BAND LIMITED TO $\frac{\pi}{L}$ BEFORE DOWNS. TO AVOID ALIASING

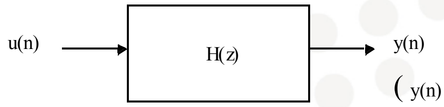
UPSAMPLING – increasing the effective f_s (pp 379)

Upsampling is accomplished by inserting L-1 zero values between samples (as shown in fig. 9.7)



- The spectra of the resulting upsampled signal are identical to the original signal but with a renormalization along the frequency axis.
- When a signal is upsampled by L, the frequency axis is scaled by L such that 2π now occurs where L2π occured in the original signal.

9.5 Discrete-Time Filters (pp. 382 in "J&M")



(Discrete-time filter)

(y(n) equals h(n) if u(n) is an impulse)

- An input series of numbers is applied to a filter to create a modified output series of numbers
- Discrete-time filters are most often analyzed and visualized in terms of the z-transform
- In this figure (Fig. 9.9) the output signal is defined to be the impulse response, h(n), when the input, u(n), is an impulse (i.e. 1 for n = 0 and 0 otherwise. Transfer function; H(z) being the z-transform of the impulse response, h(n) .

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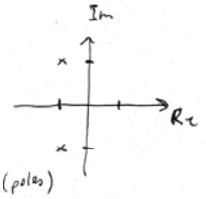
Continuous time LP-filter

PP 382 "Johns & Martin"

The transfer function for discrete-time filters appear similar to those for continuous-time filters, except that, instead of polynomials in s, polynomials in z are obtained. For example, the transfer function of a Low-pass, continuous time filter, $H_c(s)$ might appear as



$$H_c(s) = \frac{4}{s^2 + 2s + 4}$$

$$ax^2 + bx + c$$

$$x = \frac{-b \pm \sqrt{b^2 - 4 \cdot a c}}{2a}$$

$$s = \frac{-2 \pm \sqrt{2^2 - 4 \cdot 1 \cdot 4}}{2 \cdot 1} = \frac{-2 \pm \sqrt{-3 \cdot 4}}{2} = \frac{-2 \pm 2\sqrt{-3}}{2}$$

$s = -1 \pm j\sqrt{3}$, roots of the denominator.

This LP-filter is also defined to have to zeros at ∞ since the denominator polynomial is two orders higher than the numerator polynomial. To find the frequency response of $H_c(s)$ the poles and zeros may be plotted (fig. 9.10 a))

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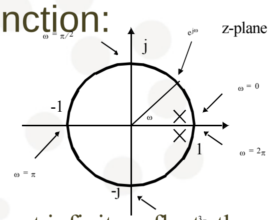
Discrete-Time Transfer Function

- Assume the following (LP-) transfer function:

$$H(z) = \frac{0{,}05}{z^2 - 1{,}6z + 0{,}65}$$



- Poles: Complex conjugated at 0.8+/-0.1j
- Zeros: Two zeros at infinity (Defined). The number of zeros at infinity reflects the difference in order between denominator and nominator
- In the discrete time somain z=1 corresponds to the freq. response at both dc (ω= 0) and $\omega = 2\pi$.
- The frequency respons need only be plotted for $0 \leq \omega \leq \pi$ (frequency response repeats every 2π.
- The unit circle, $e^{j\omega}$, is used to determine the frequency response of a system that has it's input and output as a series of numbers.
- (The magnitude is represented by the product of the lengths of the zero-vectors divided by the product of the lengths of the pole-vectors.
- The phase is calculated using addition and subtraction)

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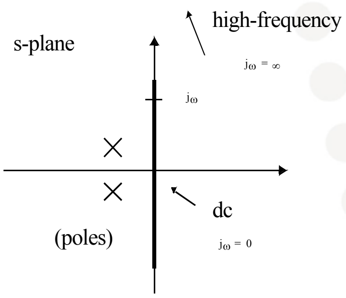
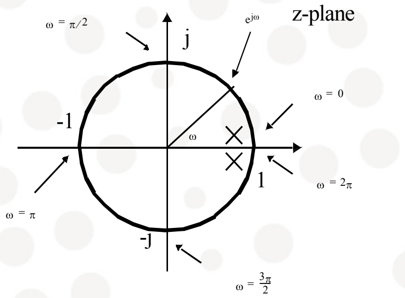
Frequency response





- The frequency response of discrete-time filters are similar to the response of continuous-time filters. The poles and zeroes are located in the z-plane instead of the s-plane
- DC/2π equals z=1, fs/2 equals z=-1
- The response is periodic with period 2π

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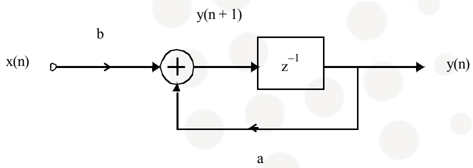
Stability of Discrete-Time Filters



- The filters are described by finite difference equations $y(n+1) = bx(n) + ay(n)$
- In the z-domain: $zY(z) = bX(z) + aY(z)$

$$H(z) \equiv \frac{Y(z)}{X(z)} = \frac{b}{z-a}$$

- H(z) has a pole in z=a. a<=1 to ensure stability
- In general a LTI system is stable if all the poles are located inside or on the unit circle

Test for stability

- Let the input, x(n) be an impulse signal (i.e. 1 for n=0, and 0 otherwise), which gives the following output signal, according to 9.25, y(0) = k, where k is some arbitrary initial state for y.
- y(n+1)=bx(n) + ay(n)
- y(0+1) = b x(0) + a y(0) = b 1 + ak = b + ak,
- y(2) = b x(1) + a y(1) = b 0 + a (b + ak) = ab + a^2k
- Y(3) = b x(2) + a y(2) = b 0 + a y(2) = a (ab + a^2k) = a^2b +a^3k
- Y(4) = a^3b +a^4k
- Response, h(n) = 0 for (n < 0),
- k for (n=0)
- (a^{n-1}b+a^nk) for n>=1
- This response remains bounded only when |a|<=1 for this 1st order filter, and unbounded otherwise.
- In general, an arbitrary, time invariant, discrete time filter, H(z), is stable if, and only if, all its poles are located within the unit circle.

IIR and FIR Filters

- Infinite Impulse Response (IIR) filters are discrete-time filters whose outputs remain non-zero when excited by an impulse:
  - Can be more efficient
  - Finite precision arithmetic may cause limit-cycle oscillations
- Finite Impulse Response (FIR) filters are discrete-time filters whose outputs goes precisely to zero after a finite delay:
  - Poles only in z=0
  - Always stable
  - Exact linear phase filters may be designed
  - High order often required

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Bilinear transform

Bilinear transform

In many cases it is desirable to convert a continuous-time filter into a discrete-time filter or vice versa.

Assuming that $H_c(p)$ is a continuous time transfer function (where p is the complex variable equal to $\sigma_p + j\Omega$), the bilinear transform is defined to be given by

$$p = \frac{z-1}{z+1}$$

Finding the inverse transformation:

$$p(z+1) = z-1 \Leftrightarrow pz + p = z-1 \Leftrightarrow pz - z = -1-p \Leftrightarrow z(p-1) = -p-1 \Leftrightarrow z = \frac{-(p+1)}{p-1} \Leftrightarrow$$

$$z = \frac{-(p+1)}{p-1} \Leftrightarrow z = \frac{-(1+p)}{-(1-p)} \Leftrightarrow z = \frac{1+p}{1-p}$$

z-plane locations of 1 and −1 (i.e. dc and $f_s/2$) are mapped to p-plane locations of 0 and ∞, respectively.

The bilinear transform also maps the unit circle, $z = e^{j\omega}$ in the z-plane to the entire $j\Omega$-axis in the p-plane. To see the mapping:

$$p = \frac{e^{j\omega}-1}{e^{j\omega}+1} = \frac{e^{j\frac{\omega}{2}}(e^{j\frac{\omega}{2}} - e^{-j\frac{\omega}{2}})}{e^{j\frac{\omega}{2}}(e^{j\frac{\omega}{2}} + e^{-j\frac{\omega}{2}})}$$

$$= \frac{2j\sin(\frac{\omega}{2})}{2\cos(\frac{\omega}{2})} = j\tan(\frac{\omega}{2})$$

$$\boxed{\cos\varphi = \frac{e^{j\varphi}+e^{-j\varphi}}{2} \quad \sin\varphi = \frac{e^{j\varphi}-e^{-j\varphi}}{2j}}$$

Points on the unit circle in the z-plane are mapped to locations on the $j\Omega$-axis in the p-plane, and we have $\Omega = \tan(\omega/2)$

Bilinear Transform

- In many cases it is desirable to convert a continuous-time filter into a discrete-time filter or vice-versa.
- $H_c(p)$ is a CT transfer function with p = $\sigma_p + j\Omega$ .Then

$$p = \frac{z-1}{z+1} \qquad z = \frac{1+p}{1-p}$$

- The bilinear transforms map the z-plane locations of 1(DC) and -1(fs/2) to the p-plane locations 0 and ∞ .

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Bilinear Transform

- The unit-circle $z = e^{j\omega}$ in the z-plane is mapped to the entire jΩ-axis in the p-plane:

$$p = \frac{e^{j\omega}-1}{e^{j\omega}+1} = \frac{e^{j(\omega/2)}(e^{j(\omega/2)}-e^{-j(\omega/2)})}{e^{j(\omega/2)}(e^{j(\omega/2)}+e^{-j(\omega/2)})}$$

$$= \frac{2j\sin(\omega/2)}{2\cos(\omega/2)} = j\tan(\omega/2)$$

- The following frequency mapping occurs:

$$\Omega = \tan(\omega/2)$$

- Then $H(z) \equiv H_c((z-1)/(z+1))$ and $H(e^{j\omega}) = H_c(j\tan(\omega/2))$

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Sample-and-Hold Response (1/3)

- A sampled and held signal is related to the sampled continuous-time signal as follows:

$$x_{sh}(t) = \sum_{n=-\infty}^{\infty} x_c(nT)[\vartheta(t-nT) - \vartheta(t-nT-T)]$$

- Taking the Laplace-transform:

$$X_{sh}(s) = \frac{1-e^{-sT}}{s} \sum_{n=-\infty}^{\infty} x_c(nT)e^{-snT}$$

$$= \frac{1-e^{sT}}{s} X_s(s)$$

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Sample-and-Hold Response (2/3)

- The hold transfer function $H_{sh}(s)$ is due to the previous result equal to:

$$H_{sh}(s) = \frac{1-e^{-sT}}{s}$$

- The spectrum is found by setting s=jω:

$$H_{sh}(j\omega) = \frac{1-e^{-j\omega T}}{j\omega} = T \times e^{-\frac{j\omega T}{2}} \times \frac{\sin\left(\frac{\omega T}{2}\right)}{\left(\frac{\omega T}{2}\right)}$$

- Finally the magnitude is given by:

$$|H_{sh}(j\omega)| = T\frac{\left|\sin\left(\frac{\omega T}{2}\right)\right|}{\left|\frac{\omega T}{2}\right|} \qquad |H_{sh}(f)| = T\frac{\left|\sin\left(\frac{\pi f}{f_s}\right)\right|}{\left|\frac{\pi f}{f_s}\right|}$$

- This response sin(x)/x is usually referred to as the *sinc-response*.

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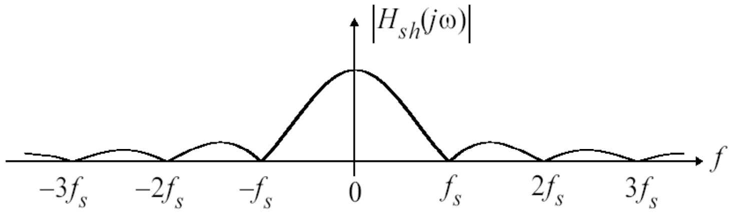
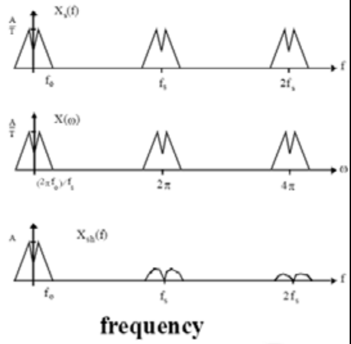
Sample-and-Hold Response (3/3)



- Shaping only occurs for continuous-time signals, since a sampled signal will not be affected by the hold function.
- A S/H before an A/D converter does not reduce the demand of an anti-aliasing filter preceeding the A/D-converter, but simply allow the A/D to have a constant input value during the conversion.



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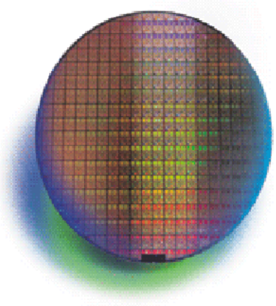
Tuesday 16th of February:

- Discrete Time Signals (from chapter 9)

Today: as far as we get with:

10.1 Basic building blocks (Opamps, Capacitors, Switches, Nonoverlappingg clocks)

10.2 Basic operation and analysis (Resistor equivalence of a Switched Capacitor, Parasitic Insensitive Integrators)



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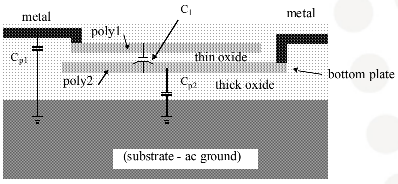
Properties of SC circuits

- Popular due to accurate frequency response, good linearity and dynamic range
- Easily analyzed with z-transform
- Typically require aliasing and smoothing filters
- Accuracy is obtained since filter coefficients are determined from capacitance ratios, and relative matching is good in CMOS
- The overall frequency response remains a function of the clock, and the frequency may be set very precisely through the use of a crystal oscillator
- SC-techniques may be used to realize other signal processing blocks like for example gain stages, voltage-controlled oscillators and modulators

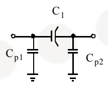
Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators (chapter 10.1)

- DC gain typically in the order of 40 to 80 dB (100 – 10000 x)
- Unity gain frequency should be > 5 x clock speed (rule of thumb)
- Phase margin > 70 degrees (according to Johns & Martin)
- Unity-gain and phase margin highly dependent on the load capacitance, in SC-circuits. In single stage opamps a doubling of the load capacitance halves the unity gain frequency and improve the phase margin
- The finite slew rate may limit the upper clock speed.
- Nonzero DC offset can result in a high output dc offset, depending on the topology chosen, especially if correlated double sampling is not used

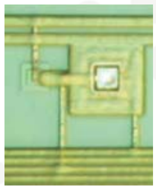
Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators



cross-section view

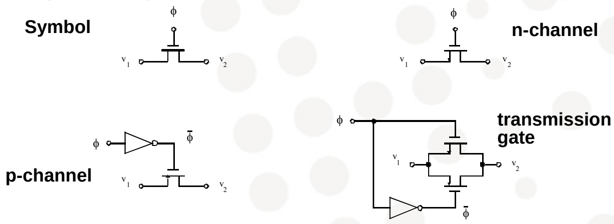


equivalent circuit



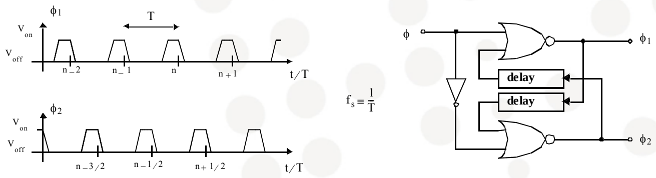
- Typically constructed between two polysilicon layers
- Parasitics; Cp1, Cp2.
- Parasitic Cp2 may be as large as 20 % of the desired, C1
- Cp1 typically 1- 5 % of C1. Therefore, the equivalent model contain 3 capacitors

Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators



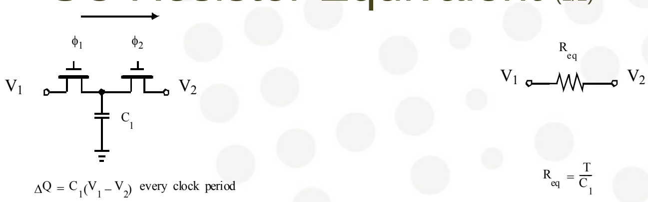
- Desired: very high off-resistance (to avoid leakage), relatively low on-resistance (for fast settling), no offset
- Phi, the clock signal, switches between the power supply levels
- Convention: Phi is high means that the switch is on (shorted)
- Transmission gate switches may increase the signal range
- Some nonideal effects: nonlinear capacitance on each side of the switch, charge injection, capacitive coupling to each side

Basic building blocks in SC circuits; Opamps, capacitors, switches, clock generators



- Must be nonoverlapping; at no time both signals can be high
- Convention in "Johns & Martin"; sampling numbers are integer values
- Location of clock edges need only be moderately controlled (assuming low-jitter sample-and-holds on input and output of the overall circuit)
- Delay elements above can be an even number of inverters or an RC network

SC Resistor Equivalent (1/2)



$$Q_x = C_x V_x$$

C1 is first charged to V1 and then charged to V2 during one clock cycle

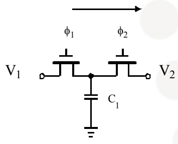
$$\Delta Q_1 = C_1(V_1 - V_2)$$

The average current is then given by the change in charge during one cycle

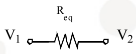
$$I_{avg} = \frac{C_1(V_1 - V_2)}{T}$$

Where T is the clock period (1/fs)

SC Resistor Equivalent (2/2)



$\Delta Q = C_1(V_1 - V_2)$ every clock period



$R_{eq} = \frac{T}{C_1}$

The current through an equivalent resistor is given by:

Combining the previous equation with **Iavg**:

$$I_{eq} = \frac{V_1 - V_2}{R_{eq}}$$

The resistor equivalence is valid when fs is much larger than the signal frequency. In the case of higher signal frequencies, z-domain analysis is required :

$$R_{eq} = \frac{T}{C_1} = \frac{1}{C_1 f_s}$$

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Example of resistor implementation

- What is the resistance of a 5 pF capacitance sampled at a clock frequency of 100 kHz?
- Note the large resistance that can be implemented. Implemented in CMOS it would take a large area for a resistor of the same resistance

$$R_{eq} = \frac{1}{(5 \times 10^{-12})(100 \times 10^{3})} = 2M\Omega$$

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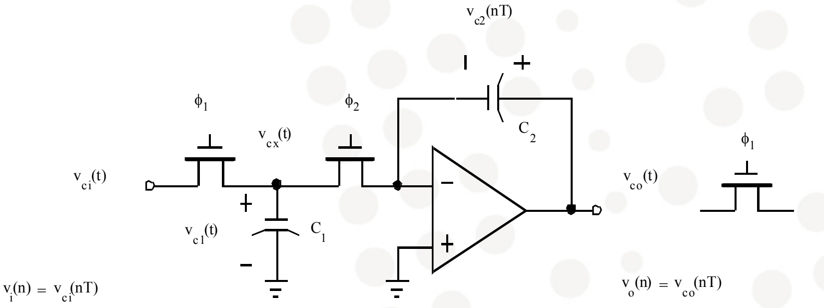
An inverting integrator



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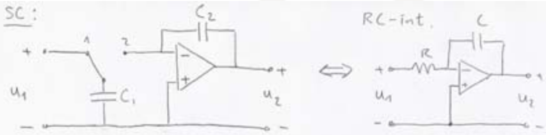
Transfer function for simple discrete time integrator in chapter 10.2



$\boxed{Q = C \cdot V}$

$f = \frac{1}{T}$

Svitsjen er ved tidspunkt $t = (n-1)T$ i posisjon 1, og det blir tatt en punktprøve ("et sampel") av $u_1(t)$, da C_1 blir ladet til :

$$q_1[(n-1)T] = C_1 \cdot u_1[(n-1)T]$$

Ladningen på C_2 er (samtidig):

$$q_2[(n-1)T] = C_2 \cdot u_2[(n-1)T]$$

Ved tidspunkt $t = n \cdot T$ blir ladningen på C_1 overført til C_2 ved at svitsjen er i posisjon 2.
Hele ladningen på C_1 blir ført over til C_2 fordi operasjonsforst. tvinger spenningen over C_1 til å bli null.

Ladn. på C_1 subtraheres dermed fra ladn. på C_2.

ref.: Nils Haaheim: "Analog CMOS", Universitetet i Trondheim - NTH, 1994

Ladn. på C_2 ved $t = nT$ blir dermed:

$$q_2[nT] = q_2[(n-1)T] - q_1[(n-1)T]$$
$$\Updownarrow$$
$$C_2 \cdot u_2[nT] = C_2 \cdot u_2[(n-1)T] - C_1 u_1[(n-1)T]$$
$$\Updownarrow$$
$$u_2[nT] = u_2[(n-1)T] - \frac{C_1}{C_2} \cdot u_1[(n-1)T]$$

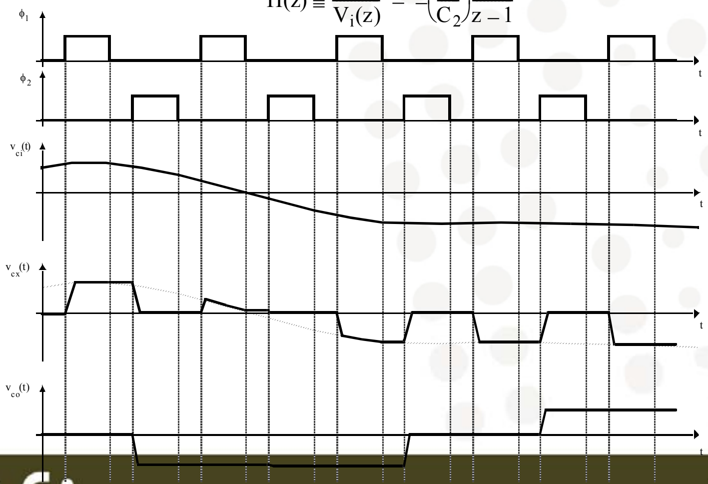
Kan benytte z-transform

obs! If $x(n) \leftrightarrow X(n)$, then $x(n-k) \leftrightarrow z^{-k} X(z)$

$$U_2(z) = U_2(z) \cdot z^{-1} - \frac{C_1}{C_2} U_1(z) z^{-1}$$
$$\Updownarrow$$
$$H(z) = \frac{U_2(z)}{U_1(z)} = -\frac{C_1}{C_2} \cdot \frac{z^{-1}}{(1 - z^{-1})}$$

Example waveforms. H(z) rewritten to eliminate terms of z having negative powers. Equation representative just before end of phi1 only

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$



Frequency response (Low frequency)

$$H(z) = -\left(\frac{C_1}{C_2}\right)\frac{z^{-1/2}}{z^{1/2} - z^{-1/2}}$$

$$z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T)$$

$$z^{1/2} = \cos\left(\frac{\omega T}{2}\right) + j\sin\left(\frac{\omega T}{2}\right)$$

$$z^{-1/2} = \cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)$$

$$H(e^{j\omega T}) = -\left(\frac{C_1}{C_2}\right)\frac{\cos\left(\frac{\omega T}{2}\right) - j\sin\left(\frac{\omega T}{2}\right)}{j2\sin\left(\frac{\omega T}{2}\right)}$$

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Example 10.2 (2/2)

- Assuming low frequency i.e. :

$$\omega T \ll 1$$

- The gain-constant is depending only on the capacitor-ratio and clock frequency:

$$H(e^{j\omega T}) \cong -\left(\frac{C_1}{C_2}\right)\frac{1}{j\omega T}$$

$$K_I \cong \frac{C_1}{C_2}\frac{1}{T}$$

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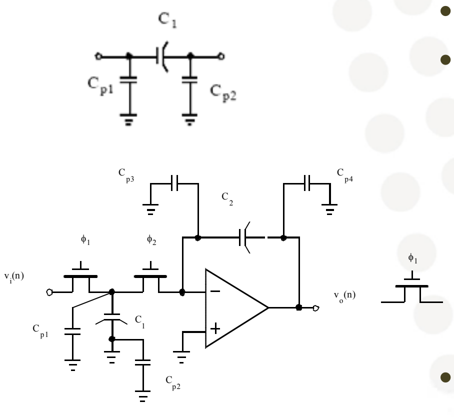
Parasitics reducing accuracy and performance



$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1}$$

- Parasitics added
- C_{p1} the one that is harmful, as accurate discrete-time frequency responses depends on precise matching of capacitors, (sometimes down to 0.1 percent)
- C_{p1} 1-5 % of C1 (page 396)
- Gain coefficient related to C_{p1} which is not well controlled and partly

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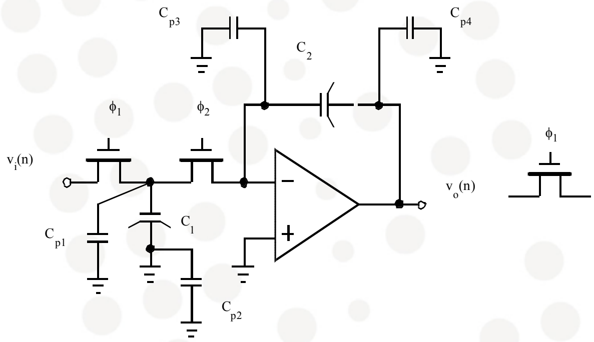
Effect of parasitic capacitors

$$H(z) = -\left(\frac{C_1 + C_{p1}}{C_2}\right)\frac{1}{z-1}$$



- The gain coefficient depends on the parasitic and possibly non-linear capacitance

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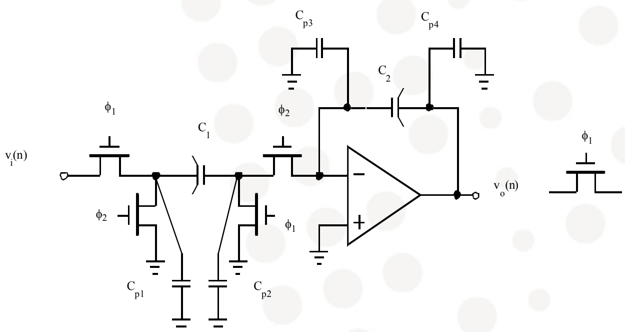
Parasitic-Insensitive Integrator



- The following parasitics does not influence:
  - Cp2 is either connected to virtual ground or physical ground
  - Cp3 is connected to virtual ground
  - Cp4 is driven by the output
  - Cp1 is charged between vi(n) and gnd.

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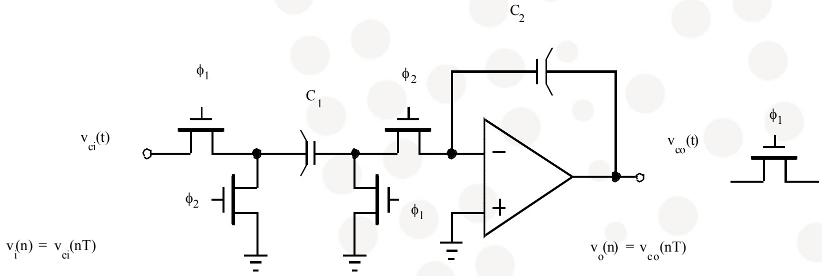
Parasitic-Insensitive Integrator



- Two additional switches removes sensitivity to parasitics:
  - Improved linearity
  - More well-defined and accurate transfer-functions

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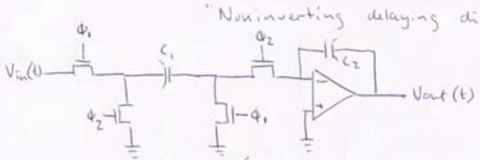
Transfer function not dependent on Cp1:

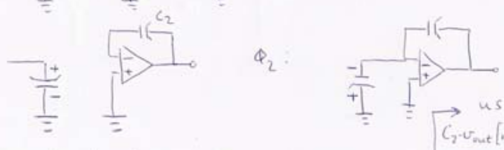
"Noninverting delaying discrete-time int." (J&M" p. 4.5)



$\boxed{Q = C \cdot V}$

Remember, from chapter 1: If $x(n) \Leftrightarrow X(z)$ then $x(n-k) \Leftrightarrow z^{-k} X(z)$

Φ_1 :



At time $t = (n-1)T$, in Φ_1, a "sample" of the input voltage is taken, and C_1 gets charged:

$$q_{c1}[(n-1)T] = C_1 \cdot v_{in}[(n-1)T]$$

At the same time, there is a charge on C_2:

$$q_{c2}[(n-1)T] = C_2 \cdot v_{out}[(n-1)T]$$

At time $t = nT$ the charge on C_1 is transmitted to C_2:

$$q_{c2}[nT] = q_{c2}[(n-1)T] + q_{c1}[(n-1)T]$$

using $Q = C \cdot V$:

$$C_2 \cdot v_{out}[nT] = C_2 \cdot v_{out}[(n-1)T] + C_1 v_{in}[(n-1)T]$$

$\Updownarrow$ z-transf. :

$$C_2 V_{out}(z) = C_2 V_{out}(z) \cdot z^{-1} + C_1 V_{in}(z) \cdot z^{-1}$$

$$\Updownarrow$$

$$C_2 V_{out}(z) - C_2 V_{out}(z) \cdot z^{-1} = C_1 V_{in}(z) \cdot z^{-1}$$

$$\Updownarrow$$

$$C_2 V_{out}(z)(1 - z^{-1}) = C_1 V_{in}(z) \cdot z^{-1}$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}}$$

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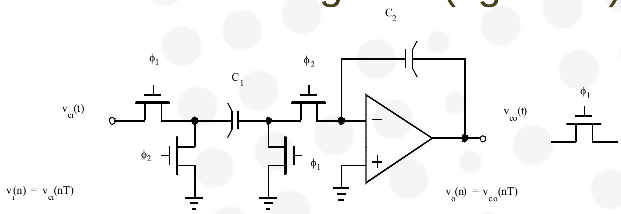
Parasitic-Insensitive Integrator (fig. 10.9)



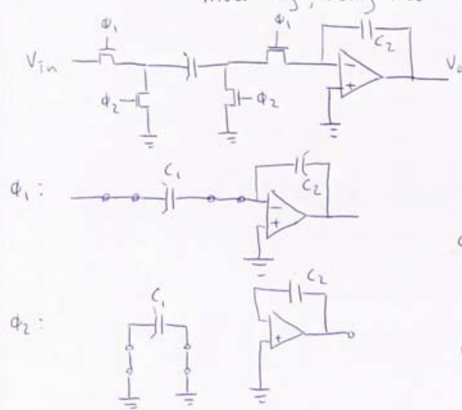
$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = \left(\frac{C_1}{C_2}\right)\frac{1}{z-1}$$

- Note that the integrator is now positive
- C_1 and C_2 no longer need to be much larger than parasitics
- A remaining limitation is the lateral stray capacitance between the lines leading to the electrodes of C_1 and C_2. This can be reduced by inserting a grounded line between the leads. In any case the minimum permissible C_1 and C_2 values are reduced by a factor 10 – 50 if the stray-insensitive configuration is used, hence reducing the area required by the capacitors is reduced by the same factor [GrTe86]. Price is proportional to area.
- While parasitics do not affect the discrete time difference equation (or H(z)), they may slow down settling time behaviour.

H(z) for inverting, delay-free integrator

Inverting, delay-free integrator (fig. 10.12 in "J&M")

$Q = C \cdot V$



Charge on C_2 at the end of ϕ_1 is equal to it's old value minus the charge needed to charge C_1 to $v_{in}(nT)$:

$$C_2 V_{out}(nT) = C_2 v_{out}[(n-1)T] - C_1 v_{in}[nT]$$

Dividing by C_2 and switching to discrete-time variables:

$$V_{out}(n) = V_{out}(n-1) - \frac{C_1}{C_2} v_{in}(n)$$

z-transf.:

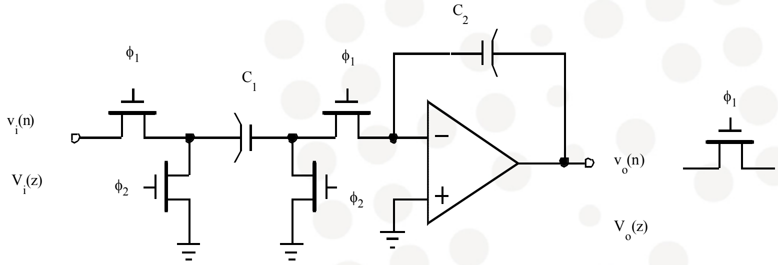
$$V_{out}(z) = V_{out}(z) \cdot z^{-1} - V_{in}(z) \cdot \frac{C_1}{C_2}$$

The charge on C_2 does not change when ϕ_2 turns on (and ϕ_1 is off).

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{1}{1-z^{-1}}$$

$V_{in}(nT)$ occurs in the difference equation, rather than $V_{in}[(n-1)T]$, since the charge on C_2 at the end of ϕ_1 is related to $V_{in}(nT)$ at the same time → "DELAY-FREE"

Inverting delay-free integrator (fig. 10.12)



- Equations similar to previous slide, but with clocking- and timing convention as in fig. 10.3:

$$C_2 v_{co}(nT - T/2) = C_2 v_{co}(nT - T)$$

$$C_2 v_{co}(nT) = C_2 v_{co}(nT - T/2) - C_1 v_{ci}(nT)$$

- H(z) having z^{-1} removed: $H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\left(\frac{C_1}{C_2}\right)\frac{z}{z-1}$

Next time, Tuesday the 23rd

- Rest of chapter 10. (10.3, 10.4, 10.5, 10.7)
- Chapter 11, Data Converter Fundamentals

Switched-Capacitor Circuits
(chapters 10.4, 10.5, 10.6, start of chapter 11 Data converter fundamentals)

Tuesday 23rd of February, 2010, 9:15-12:00

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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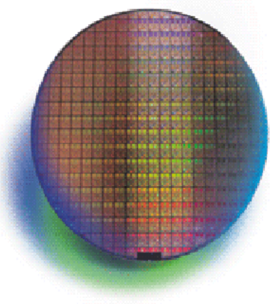
Last time – and today, Tuesday 23rd of February:

9.2 Laplace Transform of Discrete Time Signals
9.3 z-transform
9.4 downsampling and Upsampling
9.5 Discrete Time Filters
9.6 Sample-and-Hold Response

10.1 Switched Capacitor Circuits
10.2 Basic Operation and Analysis

Today:
10.3 First-order filters
10.4 Biquad filters (high-Q)
10.5 Charge injection
10.7 Correlated double sampling techn
11.1 Ideal D/A converter
11.2 Ideal A/D converter
11.3 quantization noise
11.4 signed codes



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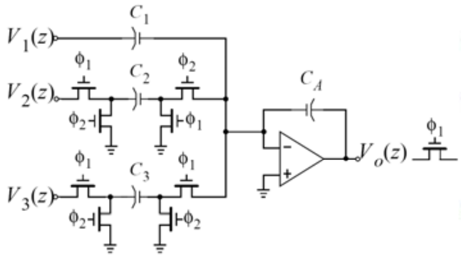
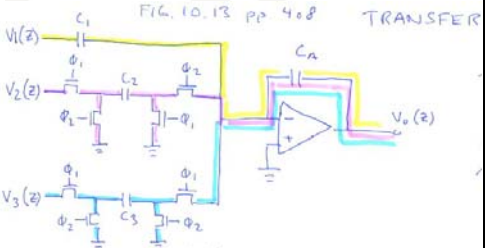
Signal-flow-graph analysis (p. 407)





- Applying charge equations is tedious for larger circuits. Using some rules and signal-flow-graph analysis simplifies analysis and design of SC-circuits.
- Superposition (Wikipedia)In a linear system, *the net response at a given place and time caused by two or more independent stimuli is the sum of the responses which would have been caused by each stimulus individually*.

Individual contributions:

$$\frac{V_o(z)}{V_1(z)} = -\frac{C_1}{C_A} \quad (10.28)$$ (See lecture notes from 16/2)

$$\frac{V_o(z)}{V_2(z)} = \frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}} \quad (10.29)$$ (Noninverting delaying integrator See eq. 10.26)

$$\frac{V_o(z)}{V_3(z)} = -\frac{C_3}{C_A}\frac{1}{1-z^{-1}} \quad (10.30)$$ (delay-free int., see eq. 10.25)

Getting the transfer function..

Multiplying each of the equations (10.28), (10.29), (10.30) by their respective input voltages, on each side:

$$V_o(z) = -\frac{C_1}{C_A} \cdot V_1(z)$$

$$V_o(z) = \frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}} \cdot V_2(z)$$

$$V_o(z) = -\frac{C_3}{C_A}\frac{1}{(1-z^{-1})} \cdot V_3(z)$$

Adding the contributions:

$$V_{out}(z) = -\frac{C_1}{C_A} \cdot V_1(z) + \frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}} V_2(z) + -\frac{C_3}{C_A}\frac{1}{(1-z^{-1})} \cdot V_3(z)$$

As powers of z:

$$V_{out}(z) = -\frac{C_1}{C_A} \cdot V_1(z) + \frac{C_2}{C_A}\frac{1}{z-1} V_2(z) - \frac{C_3}{C_A}\frac{z}{z-1} V_3(z) \quad (10.31)$$

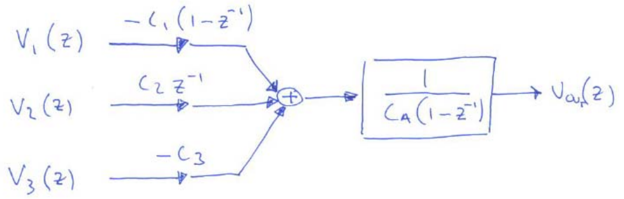
Signal Flow Graph (Fig. 10.13 in "J & M")

SIGNAL FLOW GRAPH IN FIG 10.13

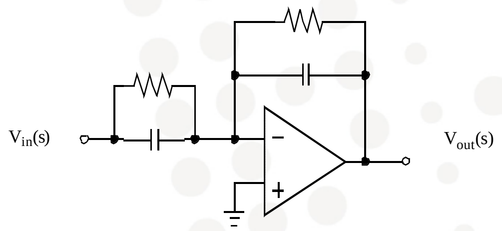
(10.30) $$V_{out}(z) = -\frac{C_1}{C_A}\cdot V_1(z) + \frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}}V_2(z) - \frac{C_3}{C_A}\frac{1}{1-z^{-1}}V_3(z)$$

$$= -\frac{C_1}{C_A}\frac{(1-z^{-1})}{(1-z^{-1})}\cdot V_1(z) + \frac{C_2}{C_A}\frac{z^{-1}}{1-z^{-1}}V_2(z) - \frac{C_3}{C_A}\frac{1}{1-z^{-1}}V_3(z)$$

See that $\frac{1}{C_A(1-z^{-1})}$ is a common factor



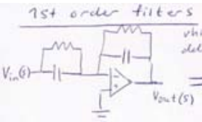
First-Order Filters



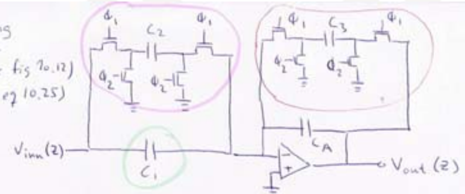
- Select a known Active-RC circuit
- Replace resistors by SC-equivalents
- Analyze using discrete-time methods

Making 1st order SC-filter from active RC equivalent

1st order filters



via inverting delay-free SC $\Rightarrow$ (See fig 10.12) (See eq 10.25)



Superposition

$$V_{out}(z) = -\frac{C_2}{C_A}\frac{1}{1-z^{-1}}\cdot V_{in}(z) - \frac{C_3}{C_A}\frac{1}{1-z^{-1}}\cdot V_{out}(z) - \frac{C_1}{C_A}V_{in}(z)$$

$$V_{out}(z)\cdot C_A(1-z^{-1}) = -C_2\cdot V_{in}(z) - C_3\cdot V_{out}(z) - C_1(1-z^{-1})\cdot V_{in}(z)$$

$$\Updownarrow$$

$$V_{out}(z)\cdot C_A(1-z^{-1}) + C_3 V_{out}(z) = -C_2\cdot V_{in}(z) - C_1(1-z^{-1})V_{in}(z)$$

$$\Updownarrow$$

$$V_{out}(z)\left[C_A(1-z^{-1}) + C_3\right] = -V_{in}(z)\left[C_2 + C_1(1-z^{-1})\right]$$

$$\Updownarrow$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{\left[C_2 + C_1(1-z^{-1})\right]}{\left[C_A(1-z^{-1}) + C_3\right]} = \frac{\frac{C_2}{C_A} + \frac{C_1}{C_A}(1-z^{-1})}{1-z^{-1}+\frac{C_3}{C_A}} = \frac{\frac{C_2}{C_A}z + \frac{C_1}{C_A}(z-1)}{z-1+\frac{C_3}{C_A}\cdot z} = \frac{\frac{C_2}{C_A}z + \frac{C_1}{C_A}z - \frac{C_1}{C_A}}{z+\frac{C_3}{C_A}z-1}$$

eq 10.33:

$$= \frac{\left(\frac{C_1+C_2}{C_A}\right)z - \frac{C_1}{C_A}}{\left(1+\frac{C_3}{C_A}\right)z - 1}$$

TET

POLES ?

Equating the denominator to zero, in $H(z)$:

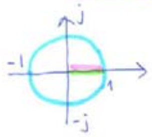
$$\left(1+\frac{C_3}{C_A}\right)z - 1 = 0$$

$$\Updownarrow$$

$$z_p = \frac{C_A}{C_A + C_3}$$

For positive capacitance values this pole is restricted to the real axis between zero and one

z-plane



In this case the circuit is always stable.

The case of $C_3 = 0$:

$$z_p = \frac{C_A}{C_A + C_3} = \frac{C_A}{C_A} = 1$$

ZEROS?

Numerator in $H(z) = 0$

$$\left(\frac{C_1+C_2}{C_A}\right)z - \frac{C_1}{C_A} = 0$$

$$\left(\frac{C_1+C_2}{C_A}\right)z = \frac{C_1}{C_A} \Leftrightarrow z = \frac{C_1}{C_1+C_2}$$

For positive capacitances the zero is located to the real axis between 0 and 1.

DC-gain $(z=1)$:

$$H(1) = -\frac{\left(\frac{C_1+C_2}{C_A}\right)z - \frac{C_1}{C_2}}{\left(1+\frac{C_3}{C_A}\right)z - 1} = -\frac{\frac{C_1}{C_A}+\frac{C_2}{C_A}-\frac{C_1}{C_A}}{1+\frac{C_3}{C_A}-1}$$

$$= -\frac{\frac{C_2}{C_A}}{\frac{C_3}{C_A}} = -\frac{C_2}{C_3}.$$

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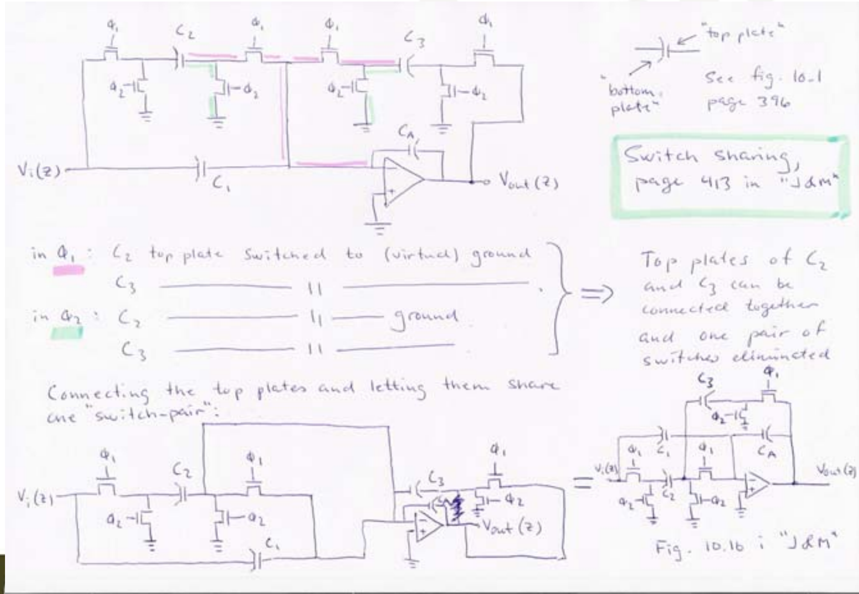
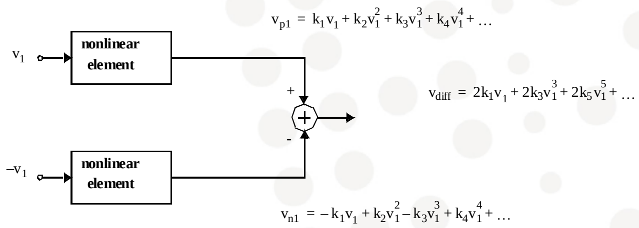
Switch sharing (p. 413)

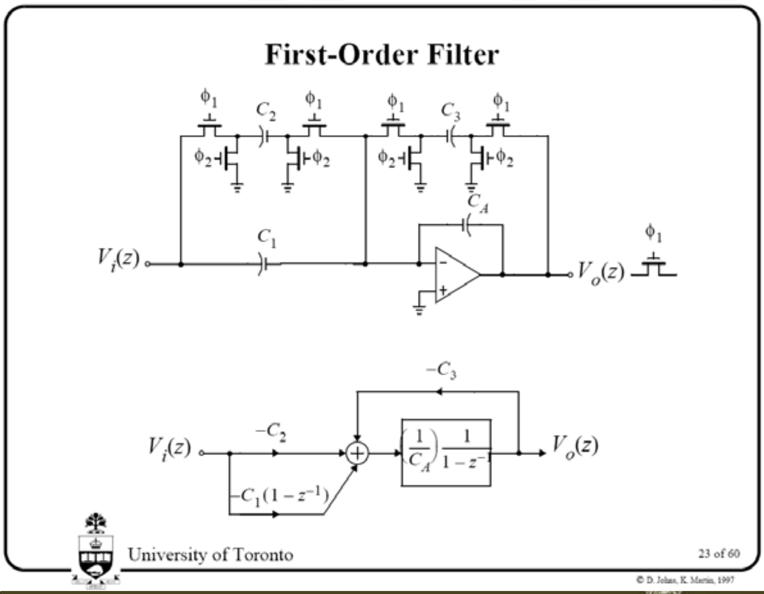


Fully Differential Filters (p. 414 (1/3))

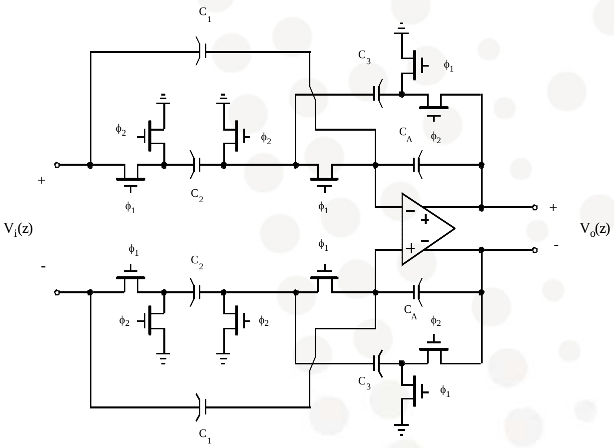


- The signal is represented by the difference of two voltages
- Most SC-designs are fully differential, typically operating around a dc common-mode voltage halfway between the supply voltages
- Reduced common-mode noise
- Cancellation of even-order harmonic distortion, if the nonlinearity is memoryless

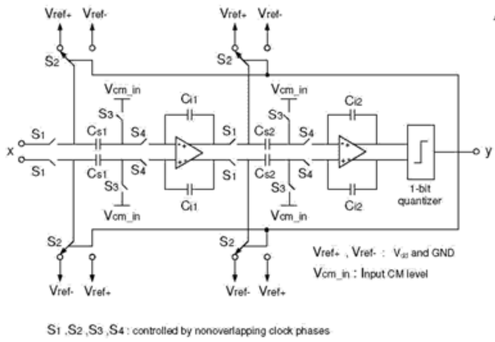
SFG based on superposition, similar as in fig 10.13.

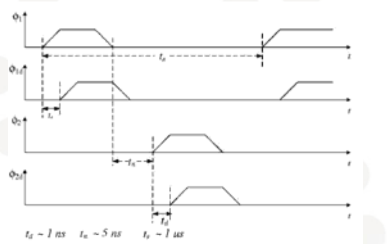


Differential implementation (fig. 10.18 p. 415)



Example: Fully differential SC-sigma-delta ADC published May 2007





A MICRO POWER SIGMA-DELTA A/D CONVERTER IN 0.35-μM CMOS FOR LOW FREQUENCY APPLICATIONS

Adnan Gundel[1,2], William N. Carr[1]

[1]New Jersey Institute of Technology, Newark, NJ 07102
[2]Telephonics Corporation, 815 Broad Hollow Road, Farmingdale, NY 11735

Figure 4. Nonoverlapping clock phases.

- Downloaded from IEEEXplore (http://ieeexplore.ieee.org/Xplore/dynhome.jsp)

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Properties of Fully Differential Filters, compared to single-ended solutions

- Requires two copies of a single-ended filter except from the Opamp which is shared
- Common-mode feedback circuitry is required
- The input- and output signal amplitude are doubled. The same dynamic range can be achieved with half-sized capacitors:
  - Area reduction and less power consumption
  - Reduced size of switches (less charge)
- More wires are required
- Improved performance with respect to noise and distortion

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Some Active RC 1st order filters (Sedra & Smith p. 779).
Filter in fig 10.14 in "Johns & Martin" lowermost.

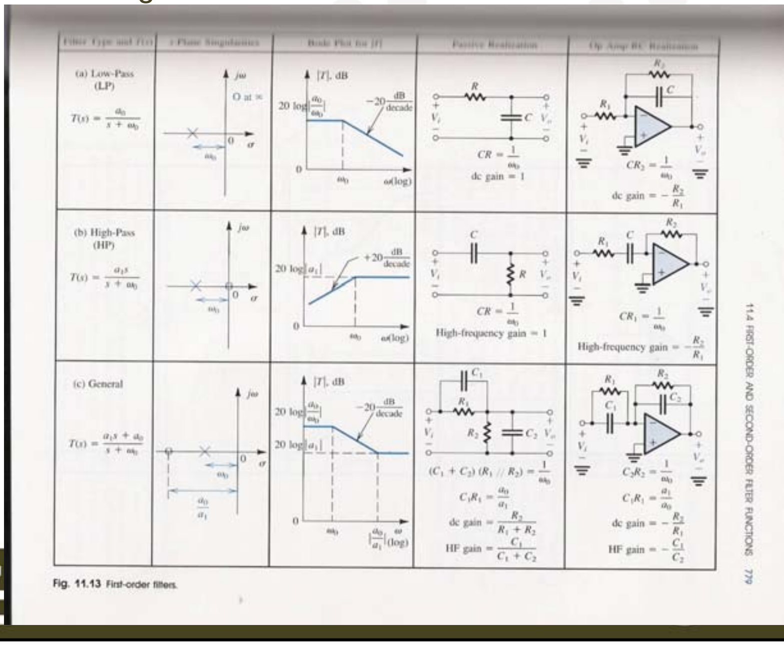

Fig. 11.13 First-order filters.

Additional litterature

- Adnan Gundel, William N. Carr: A micropower sigma-delta A/D converter in 0.35 um CMOS for low-frequency applications, Proceedings of IEEE Long Island Systems, Applications and Technology Conference, IEEE 2007
- [GrTe86]: Roubik Gregorian, Gabor C. Temes: Analog MOS Integrated Circuits for signal processing, Wiley, 1986.
- [Haah94]: Nils Haaheim: Analog CMOS, Universitetet i Trondheim, Norges Tekniske Høgskole, 1994.
- Adel S. Sedra, Kenneth C. Smith: Microelectronic Circuits, Saunders College Publ., 1989.
- Kenneth R. Laker, Willy M. C. Sansen: Design of analog integrated circuits and systems, McGraw-Hill, 1994.

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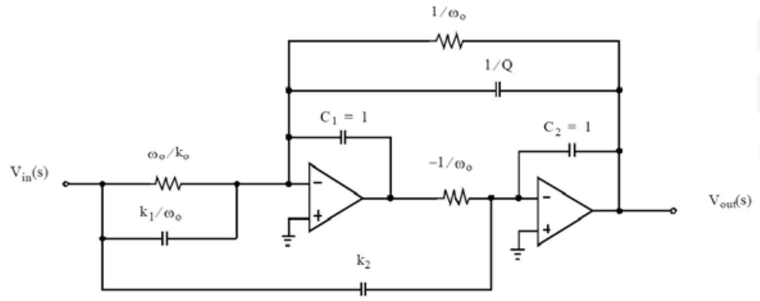
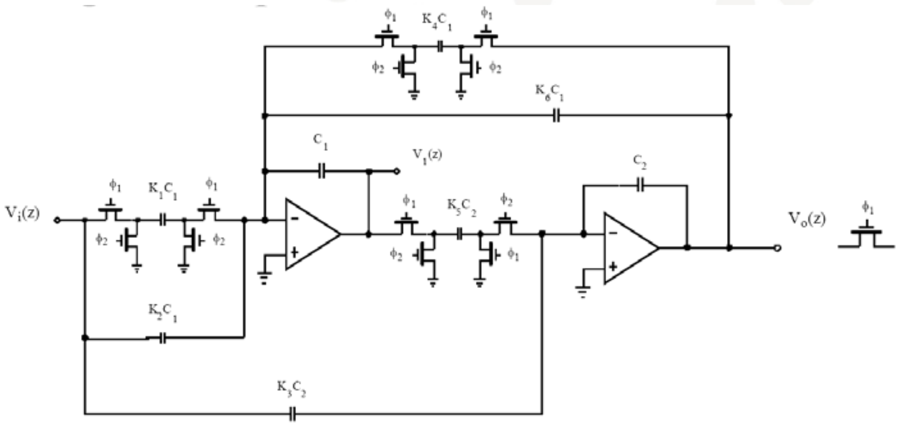
High-Q Biquad active RC-filter



- Another circuit is required for high Q-values and small capacitor spread
- Q-damping is obtained by adding a capacitor around both integrators instead of a resistive feedback around the last integrator

High-Q Switched-capacitor biquad filter (Fig. 10.25, p. 421) by changing the resistors with SC-equivalents



High-Q Biquad Filter

- General transfer function:

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_3 z^2 + (K_1K_5 + K_2K_5 - 2K_3)z + (K_3 - K_2K_5)}{z^2 + (K_4K_5 + K_5K_6 - 2)z + (1 - K_5K_6)}$$

- The function can be rewritten as:

$$H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$$

- The coefficients are then:

$$K_1K_5 = a_0 + a_1 + a_2$$
$$K_2K_5 = a_2 - a_0$$
$$K_3 = a_2$$
$$K_4K_5 = 1 + b_0 + b_1$$
$$K_5K_6 = 1 - b_0$$

- A signal-flow-graph approach is used to find the transfer function. There is some freedom in chossing the coefficients as there is one less equation than the number of coefficients. K4 = K5 = SQR (1+b0 + b1) defines the other ratios.

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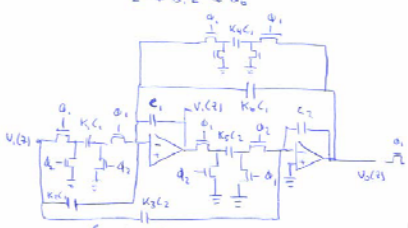
Ex 10.5 1) BP-filter, peak gain 5 near fs/10 amd Q of about 10

$$H(z) = -\frac{0.288(z-1)}{z^2 - 1.572z + 0.9429}$$

10.68: $H(z) = -\frac{a_2 z^2 + a_1 z + a_0}{z^2 + b_1 z + b_0}$

Find the largest to smallest capacitor ratio if this transfer function is realized using the high-Q biquad circuit. Let $C_1 = C_2$.



$C_1 = C_2 = 1$

(10.74): $K_4 = K_5 = \sqrt{1 + b_0 + b_1} = \sqrt{1 + 0.9429 - 1.572}$
$= \sqrt{0.3709} = 0.6090$

$K_5 \cdot K_6 = 1 - b_0 \Leftrightarrow K_6 = \frac{(1-b_0)}{K_5} = \frac{1 - 0.9429}{0.6090} = \frac{0.0571}{0.6090} = 0.0938$

(10.71) $K_3 = a_2 = 0$ (See 10.68)

(10.69): $K_1 K_5 = a_0 + a_1 + a_2$

$K_1 = (a_0 + a_1 + a_2)/K_5 = \frac{-0.288 + 0.288}{0.6090} = 0$

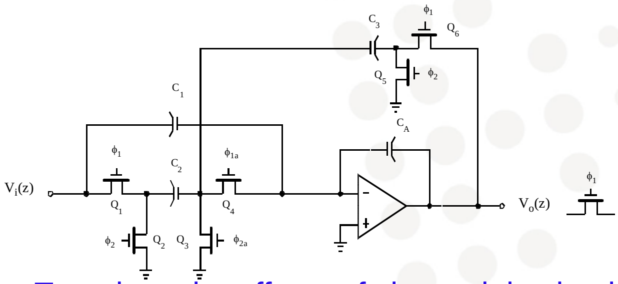
(10.70) $K_2 \cdot K_5 = a_2 - a_0 \Leftrightarrow K_2 = \frac{0 + 0.288}{0.6090} = 0.4729$

$K_1 \cdot C_1 = 0$
$K_2 \cdot C_1 = 0.4729 \cdot C_1$
$K_3 \cdot C_1 = 0$
$K_4 \cdot C_1 = 0.6090 \cdot C_1$
$K_5 \cdot C_2 = 0.6090 \cdot C_1$
$K_6 \cdot C_1 = 0.0938 \cdot C_1$

$\frac{C_1}{K_6 C_1} = \frac{1}{0.0938} = 10.66$

Max. capacitance spread is 10.66

Charge Injection (chapter 10.5)



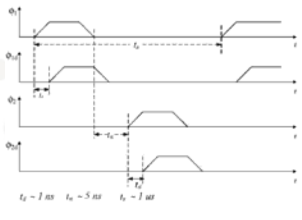
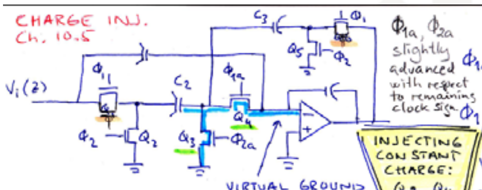


Figure 4. Nonoverlapping clock phases.

- To reduce the effects of charge injection in SC circuits, realize all switches connected to ground or virtual ground as n-channel switches only, and turn off the switches connected to ground or virtual ground first. Such an approach will minimize distortion and gain error as well as keeping DC offset low.
- In this case θ_{1a} and θ_{2a} are turned off first to prevent other switches affecting the output voltage of the circuit.

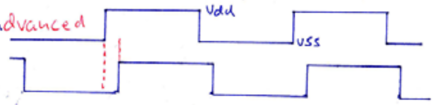
CHARGE INJ.
Ch. 10.5



Φ_{1a}, Φ_{2a} slightly advanced with respect to remaining clock sign. Φ_1

INJECTING CONSTANT CHARGE: Q_3, Q_4 Q_2, Q_5

$Q_{CH} = -WLC_{ox}(V_{GS} - V_t)$. (10.82)



Q_3 and Q_4 connect to ground or virtual ground, respectively, meaning that when they are turned on (ϕ_{2a} = Vdd or ϕ_{1a} = Vdd) they need only pass a signal near the ground node (VSS = 0V).

These two switches can be realized using single n-channel transistors. A 2nd important reason for this is that the charge injections due to Q_3 and Q_4 are not signal dependent (as will be seen)

Channel charge of an NMOS in triode, (chapter 7): $Q_{CH} = -WLC_{ox} \cdot V_{eff}$

When Q_3 and Q_4 are on, $V_{GS} = V_{DD}$, and since their source remain at 0 volts, their V_t's remain constant (in eq 10.82)

$\Rightarrow$: THE CHARGE INJECTED BY Q_3, Q_4 IS THE SAME FROM ONE CLOCK CYCLE TO THE NEXT, AND CAN BE CONSIDERED AS A DC OFFSET.

Unfortunately this is not the case for Q_1 and Q_6. Ex Q_1: $Q_{CH_1} = -W_1L_1C_{ox}(V_{DD} - V_i - V_{tn})$

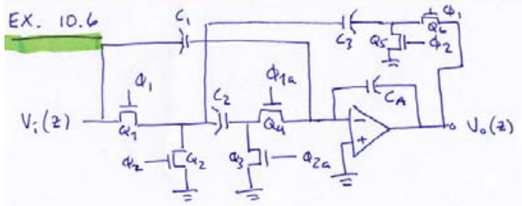
In this case one portion of the channel charge is linearly related to V_i. The V_{tn} changes in a nonlinear relationship (bulk effect). Q_{CH1} has a lin. and nonlin. relationship to V_i and would cause a gain error and distortion if Q_1 were turned off early.

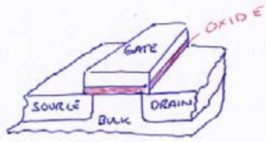
TO MINIMIZE DISTORTION, GAIN ERR. AND DC OFFS.:

TO REDUCE THE EFFECTS OF CHARGE-INJECTION IN SC-CIRCUITS, REALIZE ALL SWITCHES CONNECTED TO GROUND OR VIRTUAL GROUND AS n-CHANNEL SWITCHES, AND TURN OFF THE SWITCHES NEAR THE VIRTUAL GROUND OF THE OPAMPS FIRST.

Ex. 10.6 (1/2)

EX. 10.6





Assume an ideal opamp. Estimate the amount of dc offset at the output due to channel-charge injection when $C_1 = 0$ and $C_2 = C_A = 10\ C_3 = 10\ pF$. $V_{tn} = 0.8V$, $W = 30\,\mu m$, $L = 0.8\,\mu m$. $V_{dd} = \pm 2{,}5V$ $C_{ox} = 1.9 \cdot 10^{-3}\ pF/(\mu m)^2$

Q_3 and Q_4 are advanced, and contribute with channel charge.

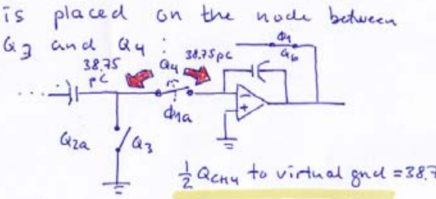
$$\underline{Q_{CH3}} = \underline{Q_{CH4}} = (-30 \cdot 10^{-6})(0.8 \cdot 10^{-6})\, 1.9 \cdot 10^{-3} \cdot \frac{10^{-12}}{(10^{-6})^2}(2.5-0.8)\,C$$

$$= -30 \cdot 0.8 \cdot 0.0019 \cdot 1.7\ pC = \underline{0.07752\ pC}$$

The dc feedback will keep the virtual input of the opamp at 0 volts. All feedback current is charge transferred through C_3.

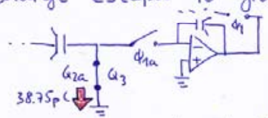
Ex. 10.6 (2/2)

When ϕ_{1a} turns off, half the charge, Q_{CH4}, goes to virtual ground, while half of Q_{CH4} is placed on the node between Q_3 and Q_4:



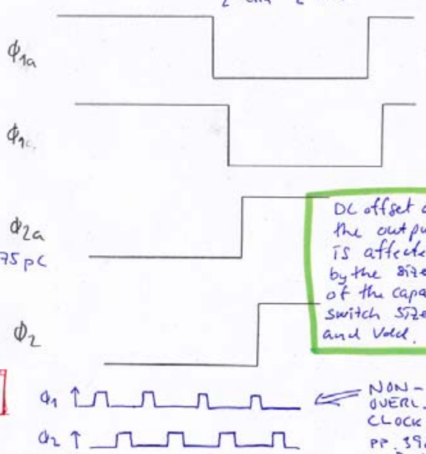
$\frac{1}{2} Q_{CH4}$ to virtual gnd $= 38.75\ pC$

When ϕ_{2a} goes high, the 2nd charge escapes to ground:



$\boxed{Q = CV}$

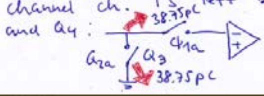
$\frac{1}{2} Q_{CH4} + \frac{1}{2} Q_{CH3} = 77.5 \cdot 10^{-3}\ pC$



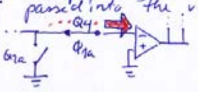
DC offset on the output is affected by the sizes of the capacitors, switch sizes and Vdd.

NON-OVERL. CLOCKS, PP. 398 IN J & M.

When Q_{2a} goes low, half of it's channel ch. is left between Q_3 and Q_4:



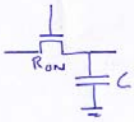
At "last" when ϕ_{1a} goes high again, the previously mentioned charge package is passed into the virtual ground:



$\frac{1}{2} Q_{CH3}$ to virtual gnd $= 38.75\ pC$

$$V_{out} = \frac{Q_{C3}}{-C_3} \qquad \frac{Q_{C3}}{C_3} = \frac{77.5 \cdot 10^{-3}\ pC}{1\ pF} = 77.5\ mV$$

CHARGE INJECTION AND HIGHER FREQUENCIES



$Q = CV$

$V = \frac{Q}{C}$

The smaller the R_{on} and smaller the C, the higher the frequency of switching (possible)

$$H(s) = \frac{1}{1+\tau s} \quad \wedge \; \tau = RC$$

To decrease R_{ON} the size of the switch increases, and thus the charge injection.

Will derive a simple formula that gives the upper bound on the frequency of operation of an SC circ. for a max. voltage change due to charge inj.: (ignore overlap capacitance)

MOST SC CIRC. HAVE 2 SERIES SWITCHES PER CAPACITOR. AS A RULE OF THUMB, FOR GOOD SETTLING, THE SAMPLING CLOCK HALF PERIOD MUST BE GREATER THAN 5 TIME CONST.

$$\frac{T}{2} > 5 R_{ON} \cdot C \iff f_{clk} < \frac{1}{10 R_{ON} C} \quad (10.89)$$

$$f_{clk} = \frac{1}{T}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox} \cdot \frac{W}{L} \cdot V_{eff}} \quad (1.108)$$

Using (10.83) the charge change due to the channel charge caused by turning an n-channel switch off is approximated by

$$|\Delta V| = \frac{1}{2} Q_{CH} \cdot \frac{1}{C} = \frac{W L C_{ox} V_{eff}}{2C}$$

For a specified $|\Delta V|_{max}$

$$C = \frac{W L C_{ox} V_{eff}}{2|\Delta V|_{max}}$$

Substituting in (10.89):

$$f_{clk} < \frac{1}{10 \cdot \frac{1}{\mu_n \cancel{C_{ox}} \frac{W}{L} \cancel{V_{eff}}} \cdot \frac{\cancel{W} L \cancel{C_{ox}} \cancel{V_{eff}}}{2|\Delta V|_{max}}}$$

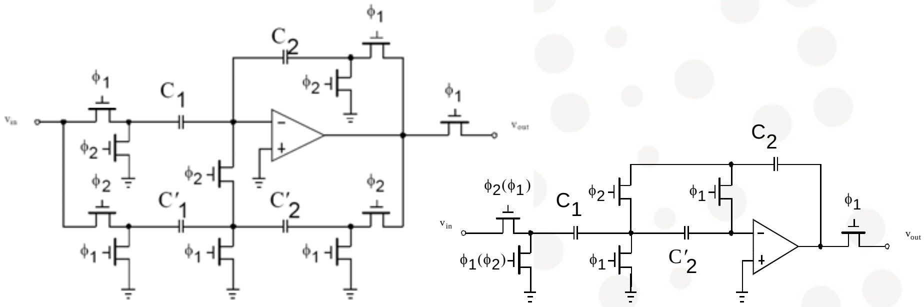
$$f_{clk} < \frac{\mu_n |\Delta V|_{max}}{5 L^2}$$

⇒: UPPER FREQ. LIMIT INVERSELY PROPORTIONAL TO L^2. IT IGNORES OVERLAP CAP. AND IS SOMEWHAT OPTIMISTIC

Correlated Double Sampling ("CDS")

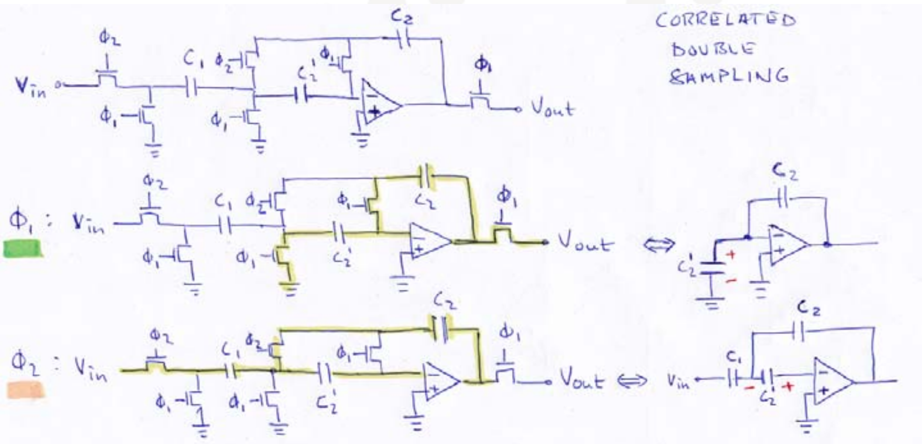
- Used to realize highly accurate gain amplifiers, sample-and-hold circuits and integrators to reduce errors due to offset voltages, 1/f noise and finite opamp gain.
- Method: During a calibration phase the input voltage of an opamp is sampled and stored (accross a C) and later subtracted from the signal in the operational phase (when the output is being sampled), by appropriate switching of the capacitors.
- A detailed description is beyond the scope of the text in "J & M". The interested reader may check : C. G. Themes, C. Enz: "Circuit techniques for reducing the effects of opamp imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Nov. 1996.

SC amplifier (left) and SC integrator with CDS (right)



- For the amplifier: During θ2 the error is sampled and stored across C1 and C2
- The stored error is then subtracted during θ1
- For the integrator: During θ1 the error is sampled and stored across C'2
- The stored error is then subtracted during θ2

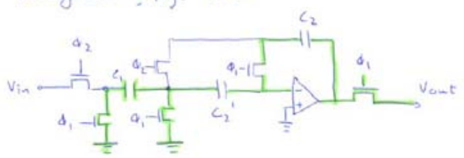
CORRELATED DOUBLE SAMPLING



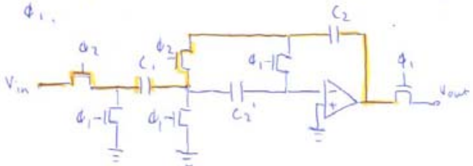
The opamp input error voltage is sampled during ϕ_1. Next, during ϕ_2', C_2' is connected in series with the opamp's inverting input and greatly minimizes the effects of these errors (by a factor of the inverse of the opamp's gain over what would otherwise occur at frequencies substantially less than the sampling frequency).

CORRELATED DOUBLE SAMPLING (CDS)

Integrator, fig. 10.35



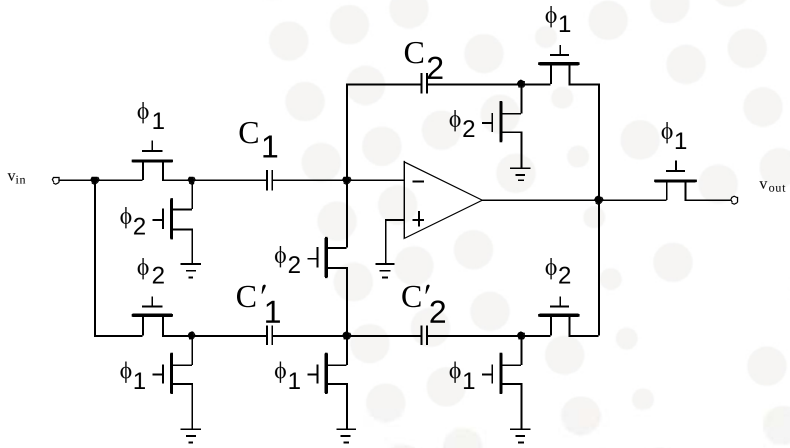
An additional capacitor, C_2' samples the opamp input error voltage during ϕ_1.



During ϕ_2, C_2' is connected in series with the opamp's inverting input and greatly minimizes the effects of these errors

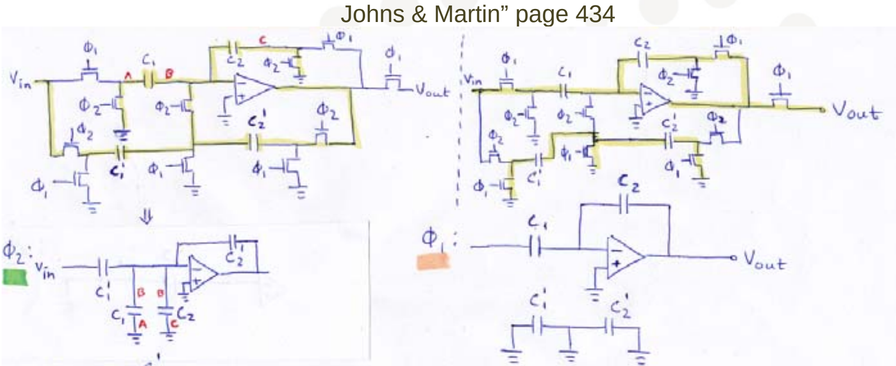
- Reducing errors by a factor of the inverse of the opamp's gain over what would otherwise occur at frequencies substantially less than the sampling frequency
- When CDS is used, the opamps should be designed to minimize thermal noise rather than 1/f noise.
- When used in SC-filters only a couple among the stages typically need CDS
- Very useful in over-sampling A/D converters

SC-integrator with CDS ("J & M" page 434)



- During Phi1 the error is sampled and stored accross C2

”Johns & Martin” page 434



$V_{out} \cong -\frac{C_1'}{C_2'} \cdot V_{in}$

Errors due to finite-offset voltage, 1/f noise and gain are included. At the same time the finite opamp input voltage caused by these errors is sampled and stored accross C_1 and C_2.

Next, during ϕ_1, this input error voltage is subtracted from the signal (applied to the opamp input) at that time. Assuming that the input voltage and the opamp input error voltages did not change appreciably from ϕ_1 to ϕ_2, errors due to them will be significantly reduced.

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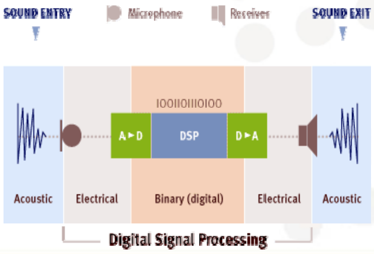
Data Converter Fundamentals (chapter 11)



Main data converter types:

- Nyquist-rate converters:
  - Each value has a one-to-one correspondencewith a single input
  - The sample-rate must be at least equal to twice the signal frequency (Typically somewhat higher)
- Oversampled converters:
  - The sample-rate is much higher than the signal frequency, typically 20 – 512 times.
  - The extra samples are used to increase the SNR
  - Often combined with noise shaping

Flash ADC from 1926 (Analog Digital Conversion handbook, Analog Devices)

The first documented flash converter was part of Paul M. Rainey's electro-mechanical PCM facsimile system described in a relatively ignored patent filed in 1921 (Reference 5—see further discussions in Chapter 1 of this book). In the ADC, a current proportional to the intensity of light drives a galvanometer which in turn moves another beam of light which activates one of 32 individual photocells, depending upon the amount of galvanometer deflection (see Figure 3.49). Each individual photocell output activates part of a relay network which generates the 5-bit binary code.

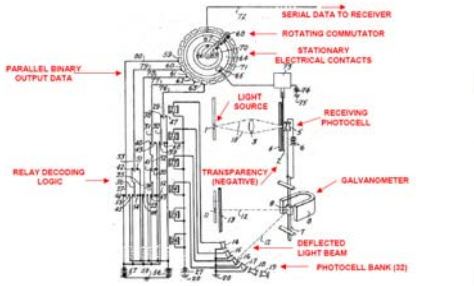


Figure 3.49: *A 5-Bit Flash ADC Proposed by Paul Rainey Adapted from Paul M. Rainey, "Facsimile Telegraph System," U.S. Patent 1,608,527, Filed July 20, 1921, Issued November 30, 1926*

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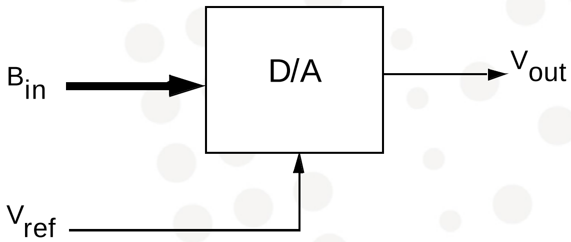
11.1 Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

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Example 11.1 : 8-bit D/A converter

An ideal D/A converter has

$$V_{ref} = 5\text{ V}$$

Find Vout when

$$B_{in} = 10110100$$

$$B_{in} = 2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} = 0{,}703125$$

$$V_{out} = V_{ref}B_{in} = 3{,}516\text{ V}$$

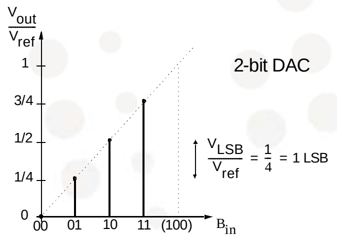
Find

V_{LSB}

$$V_{LSB} = 5/256 = 19{,}5\text{ mV}$$

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

$$1\text{ LSB} = \frac{1}{2^N}$$



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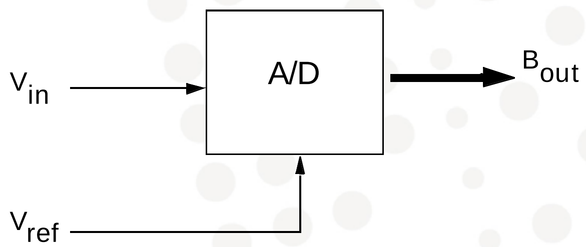
11.2 Ideal A/D converter (Fig. 11.3)



$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm V_x$$

where

$$-\frac{1}{2}V_{LSB} \le V_x < \frac{1}{2}V_{LSB}$$

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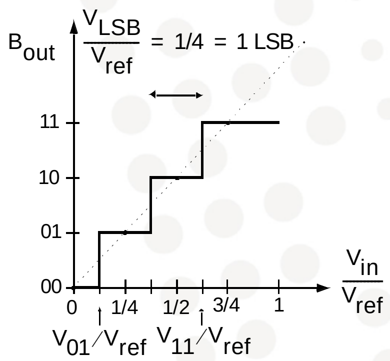
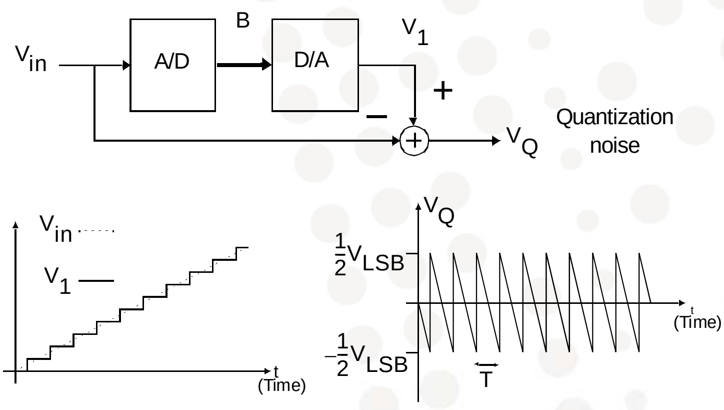
Ideal transfer curve for a 2-bit A/D converter (Fig. 11.4)



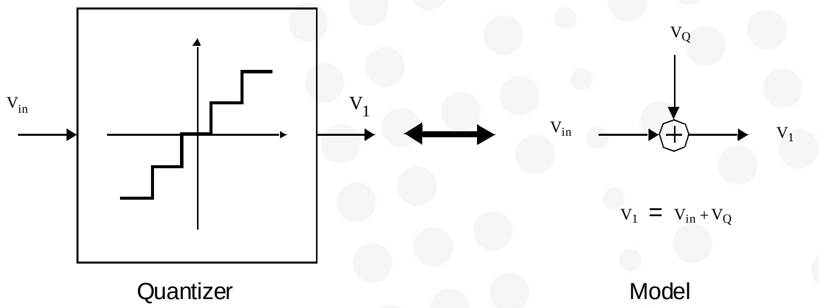
- A range of input values produce the same output value (QA range of input values produce the same output value (Quantization error)
- Different from the D/A case

11.3 Quantization noise



$$V_Q = V_1 - V_{in}$$

Quantization noise model



•TThe model is exact as long as Vq is properly defined

•Vq is most often assumed to be white and uniformely distributed between +/- Vlsb/2

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Quantization noise

•The rms-value of the quantization noise can be shown to be:

$$V_{Q(rms)} = \frac{V_{LSB}}{\sqrt{12}}$$

•Total noise power is independent of sampling frequency

•In the case of a sinusoidal input signal with p-p amplitude of $V_{ref}/2$

$$SNR = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/(2\sqrt{2})}{V_{LSB}/(\sqrt{12})}\right)$$

$$SNR = 6{,}02N + 1{,}76\ \mathrm{dB}$$

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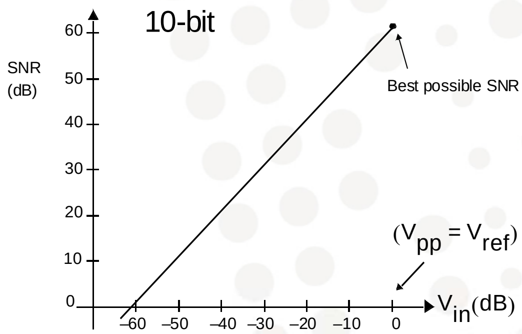
Quantization noise



•Signal-to Noise ratio is highest for maximum input signal amplitude

11.4 Signed codes

Table 11.1 Some 4-bit signed digital representations

Number	Normalized number	Sign magnitude	1's complement	Offset binary	2's complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	0010
+1	+1/8	0001	0001	1001	0001
+0	+0	0000	0000	1000	0000
(–0)	(–0)	(1000)	(1111)		
–1	–1/8	1001	1110	0111	1111
–2	–2/8	1010	1101	0110	1110
–3	–3/8	1011	1100	0101	1101
–4	–4/8	1100	1011	0100	1100
–5	–5/8	1101	1010	0011	1011
–6	–6/8	1110	1001	0010	1010
–7	–7/8	1111	1000	0001	1001
–8	–8/8			0000	1000

- Unipolar / bipolar
- Common signed digital repr.: sign magnitude, 1's complement, 2's compl.
- Sign. M.: 5:0101, -5:1101, two repr. Of 0, 2^N-1 numb.
- 1's compl.: Neg. Numbers are complement of all bits for equiv. Pos. Number: 5:0101, -5:1010
- Offset bin: 0000 to the most neg., and then counting up..
  +: closely related to unipolar through simple offset

2’s complement

A3a2a1a0	Sign magnitude	2s complement
0111	+7	+7
0110	+6	+6
0101	+5	+5
0100	+4	+4
0011	+3	+3
0010	+2	+2
0001	+1	+1
0000	+0	+0
1000	-0	-8
1001	-1	-7
1010	-2	-6
1011	-3	-5
1100	-4	-4
1101	-5	-3
1110	-6	-2
1111	-7	-1

- 5_{10} : 0101 = $2^2 + 2^0$
- \- 5_{10} : (0101)’ +1 = 1010 + 1 = 1011

- Addition of positive and negative numbers is straightforward, using addition, and requires little hardware
- 2’s complement is most popular representation for signed numbers when arithmetic operations have to be performed

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7_{10}-6_{10} via addition using two’s complement of -6

- 0000 0000 0000 0000 0000 0000 0000 0000 00111_2 = 7_{10}
- 0000 0000 0000 0000 0000 0000 0000 0000 00110_2 = 6_{10}
- *Subtraction uses addition: The appropriate operand is negated before being added*
- *Negating a two’s complement number: Simply invert every 0 and 1 and add one to the result.* Example:
- 0000 0000 0000 0000 0000 0000 0000 0000 0110_2 becomes
- 1111 1111 1111 1111 1111 1111 1111 1111 1001_2

\+ 1_2

= 1111 1111 1111 1111 1111 1111 1111 1111 1010_2

0000 0000 0000 0000 0000 0000 0000 0000 0111_2 = 7_{10}

\+ 1111 1111 1111 1111 1111 1111 1111 1111 1010_2 = -6_{10}

= 0000 0000 0000 0000 0000 0000 0000 0000 0001_2 = 1_{10}

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11.5 performance limitations

- Resolution
- Offset and gain error
- Accuracy
- Integral nonlinearity (INL) error
- Differential nonlinearity (DNL) error
- Monotonicity
- Missing codes
- A/D conversion time and sampling rate
- D/A settling time and sampling rate
- Sampling time uncertainty
- Dynamic range
- NB!! Different meanings and definitions of performance parameters sometimes exist. → Be sure what's meant in a particular specification or scientific paper.. There are also more than those mentioned here.

Resolution

- Resolution usually refers to the number of bits in the input (D/A) or output (ADC) word, and is often different from the accuracy.
- Analog-Digital Conversion Handbook, Analog Devices, 3rd Edition, 1986: *An n-bit binary converter should be able to provide 2n distinct and different analog output values corresponding to the set of n binary words. A converter that satisfies this criterion is said to have a resolution of n bits.*

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

TABLE I
KEY DATA FOR THE ADC

Nominal sampling rate	110MS/s
Technology	0.18μm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{P-P}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

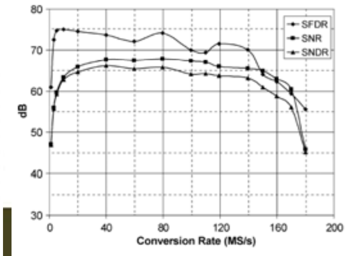

Fig. 8. SFDR, SNR, and SNDR versus conversion rate. The input frequency and signal swing is 10 MHz and $2V_{P-P}$, respectively.

Next Tuesday (2/3-10):

- Chapter 12 Nyquist DACs

Du er her: UiO > Studier > Emner > Matematikk og naturvitenskap > Informatikk > INF4420 > V10 >

Undervisningsplan (INF4420 - Vår 2010)

Dato	Undervises av	Sted	Tema	Kommentarer / ressurser
26.01.2010	Snorre Aunet ("SA")	Lille Auditorium, Ifi	introduksjon til INF4420	Slides, Slides, two per page .
02.02.2010	SA, Amir Hasanbegovic ("AH")	Lille Auditorium, Ifi.	From chapter 8 i "Johns & Martin". + SW intro (Cadence)	Slides, Slides, two per page , Other relevant material .
09.02.2010	SA	Lille Aud.	from chapters 8 and 9 in "Johns & Martin".	Slides, Slides, two per page .
16.02.2010	SA	Lille Aud.	9.2-9.6, 10.1-10.2	Slides Slides, two per page
23.02.2010	SA	Lille Aud.	Chapter 10.3, --> , beg. of chapter 11.	
02.03.2010	SA	Lille Aud.	chapter 12; Nyquist-rate DACs	
09.03.2010	SA	Lille Aud.	chapter 13; Nyquist-rate ADCs I	
16.03.2010	SA	Lille Aud.	chapter 13; Nyquist-rate ADCs II	
23.03.2010	SA	Lille Aud.	Chapter 14; Oversampling Converters	
30.03.2010				No teaching in week 13.
06.04.2010				No teaching in week 14, due to Easter holidays.
13.04.2010	SA	Lille Aud.	chapter 16; PLLs	
20.04.2010	SA, AH	Lille Aud.	"project meeting"	
27.04.2010	SA	Lille. Aud.	To be defined.	In case..
10.05.2010	AH	Lille Aud.	Selected problems relevant for the exam.	
11.05.2010	SA, AH	Lille Aud.	presentation of the project work.	

Redaksjon: Redaksjon for informasjon om studietilbudet ved UiO
Dokument opprettet: 26.12.2009, endret: 17.02.2010

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Additional litterature:

1506 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

ANALOG-DIGITAL CONVERSION

Walt Kester

Editor

ANALOG DEVICES

High speed data converters fully integrated in CMOS

by

Leif Hanssen

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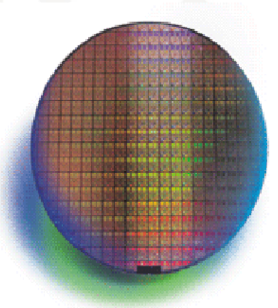
Last time – and today, Tuesday 2nd of March:

Last time:

10.3 First-order filters
10.4 Biquad filters (high-Q)
10.5 Charge injection
10.7 Correlated double sampling techniques
11.1 Ideal D/A converter
11.2 Ideal A/D converter
11.3 quantization noise
11.4 signed codes

Today:

11.5 Performance Limitations
12.1 Decoder-based converters
12.2 Binary-scaled converters
12.3 Thermometer-code converters
12.4 Hybrid converters
10:55 : 5 minute survey by "Micro"



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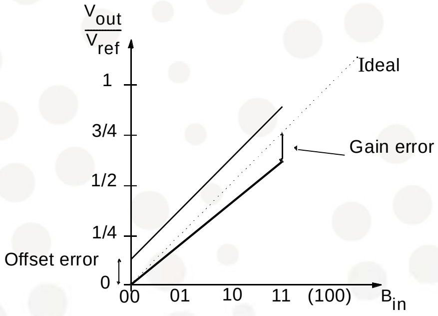
Offset and gain error

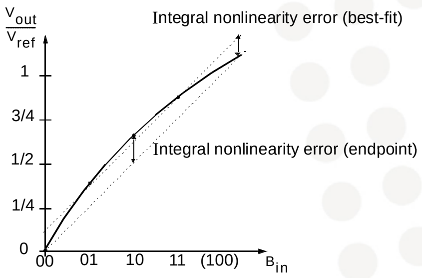
- In a D/A converter ("DAC") the *offset error* is defined to be the output that occurs for the input code that should provide zero output. For an A/D converter ("ADC") the offset error is the deviation of V0…01 from ½ LSB.
- The gain error is the the difference at the full scale value between ideal and actual curves when the offset has been reduced to zero. For a DAC it is given in units of LSBs.



ADC: given by

$$E_{gain(A/D)} = \left(\frac{V_{1\ldots1}}{V_{LSB}} - \frac{V_{0\ldots01}}{V_{LSB}}\right) - (2^N - 2) \quad (11.25)$$

Integral nonlinearity error (INL)



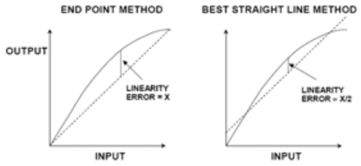
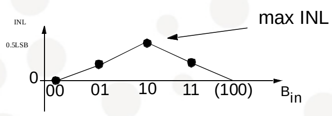
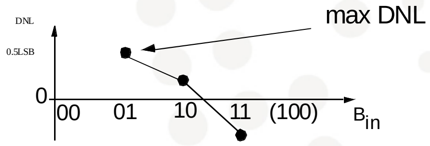


Figure 2.18: Method of Measuring Integral Linearity Errors (Same Converter on Both Graphs)



- After both offset and gain errors have been removed, the integral nonlinearity (INL) error is defined to be the deviation from a straight line. Possible straight lines: endpoints of the converters transfer respons, best-fit straight line such that the difference (or mean squared error) is minimized.

Differential nonlinearity error (DNL)

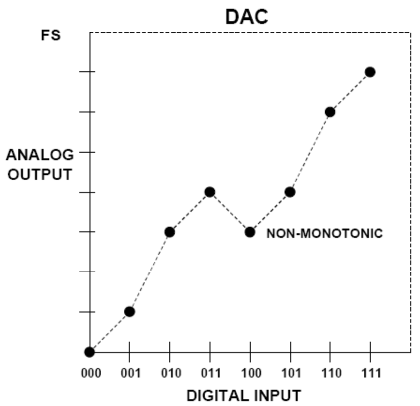


step size between 00 and 01 is 1.5 LSB
step size between 10 and 11 is 0.7 LSB

•Ideally, each analog step size is equal to 1 LSB. DNL is variation in step size from V_{LSB} (after removal of gain and offset errors). Ideally DNL is 0 for all digital values. DNL is in "J & M" defined for each digital word, whereas other sometimes refer to DNL as the maximum magnitude of DNL values.

Monotonicity in DACs

- A monotonic DAC is one in which the output always increases as the input increases (slope of the transfer response is of only one sign.)
- If the maximum DNL error is less than 1 LSB, the DAC is guaranteed to be monotonic.
- A converter is guaranteed to be monotonic if maximum DNL is < 1 LSB (or if INL is less than ½ LSB).
- 3-bit nonmonotonic example in the figure is from Analog-Digital conversion handbook by Analog Devices



D/A (DAC) settling time and sampling rate

- In a DAC the settling time is defined as the time it takes for the converter to settle within some specified amount of the final value (usually 0.5 LSB).
- The sampling rate is the rate at which samples can be continously converted and is typically the inverse of the settling time.
- Different combinations of input vectors give different settling times. Picture from "High-speed data converters fully integrated in CMOS", dissertation for the dr. scient. degree by Leif Hanssen, Ifi, UiO, 1990.

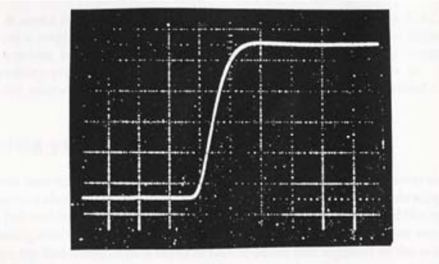


Fig 3.9 Risetime 6 bit DAC, input 0 to 128. (Xdivision = 50ns)

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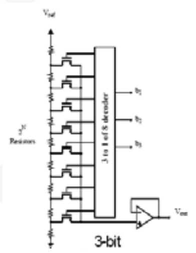
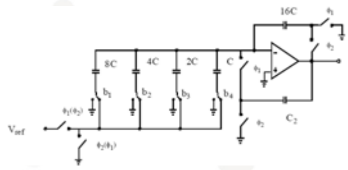
Nyquist Rate D/A Converters

- 12.1 Decoder-based converters
  - resistor string conv.
  - folded resistor string conv.
  - multiple R-string converters
- 12.2 Binary-Scaled converters
  - binary-weighted resistor converters
  - reduced resistance-ratio ladders
  - R-2R-based converters
  - charge-redistribution switched-capacitor conv.
  - current-mode conv.
- 12.3 Thermometer-code converters
  - thermometer-code current-mode D/A converters
  - single-supply positive-output converters
  - dynamically matched current sources
- 12.4 Hybrid converters
  - resistor-capacitor hybrid converters
  - segmented converters





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Some systems exploiting data converters, "Allen & Holberg"

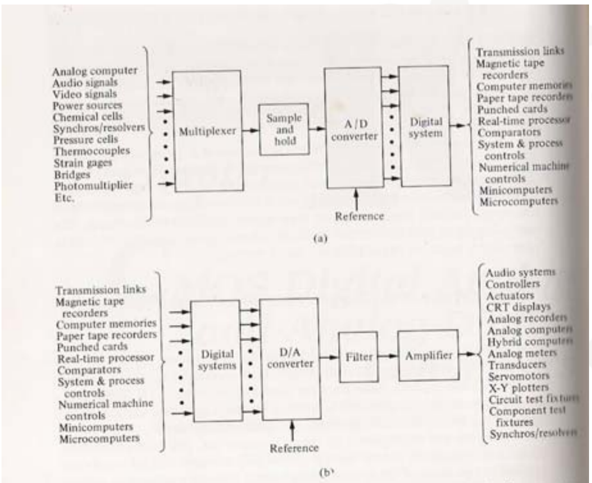
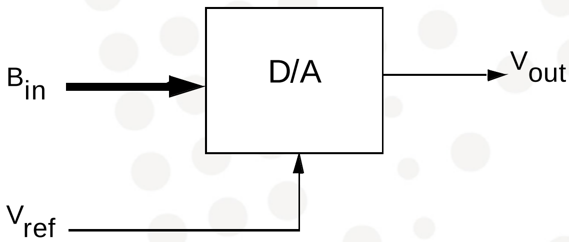


Figure 10.1-1 (a) A/D converters and (b) D/A converters in signal processing systems.

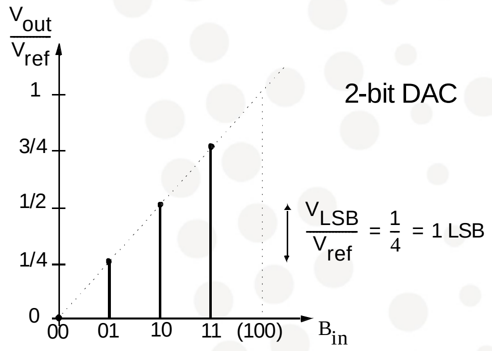
Ideal D/A converter



$$B_{in} = b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}$$

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

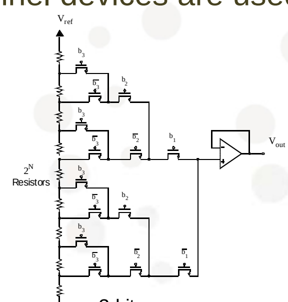
Ideal D/A converter



$$V_{LSB} \equiv \frac{V_{ref}}{2^N} \qquad 1\text{ LSB} = \frac{1}{2^N}$$

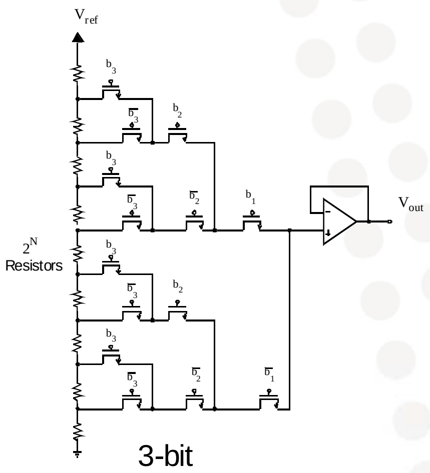
12.1 Decoder-Based Converters

- Creates 2^N reference signals and passes the appropriate signal to the output, depending on the digital input word.
- The switching network produces one, and only one, low impedance path between the resistor string and the input of the buffer
- Relatively compact switches if n-channel devices are used instead of transmission gates.



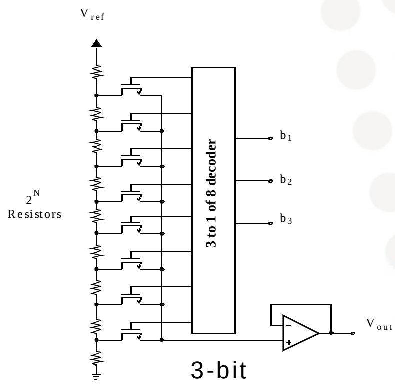
3-bit

Resistor String Converters (12.1)



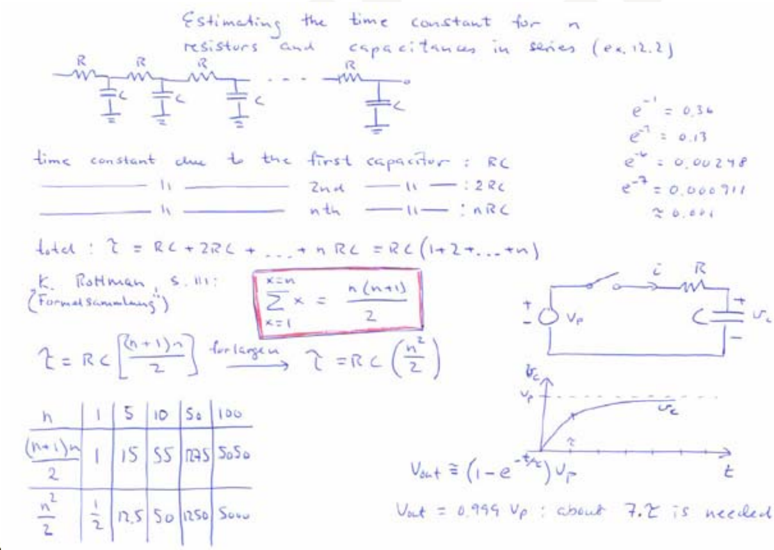
- Only one path between resistor string and D/A-output
- Guaranteed monotonicity, provided that the voltage follower does not have too large offset
- Compact design when using only n-transistors (no contacts)
- Polysilicon resistors may give resolution up to 10 bit
- Delay through switch network is the major speed limitation of the circuit
- 2^N resistors are required (when only one resistor string is included)

Resistor String Converters (12.1)

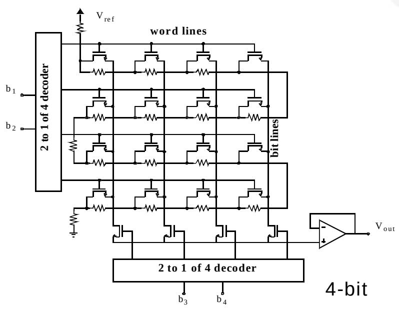


- High-speed implementation (when compared to the previous one), due to maximum of one switch in series →
- Less resistance through switches
- The switches are controlled by digital logic
- More area for the decoder compared to the previous DAC
- Larger capacitance on the buffer input, due to the 2^N transistors connected to it
- Pipelining may be applied for "moderate speed"
- 2^N resistors are required

Estimating the time constant for n resistors and capacitors in series (ex. 12.2)

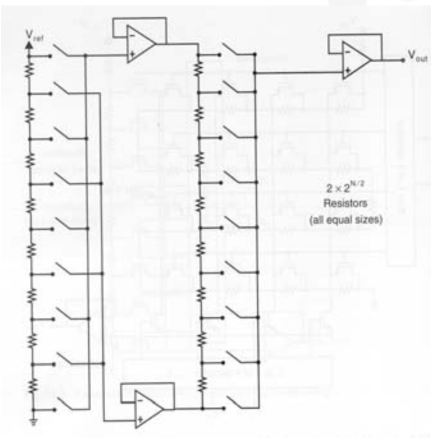


Folded Resistor-String Converters 12.1



- Reduzing size of digital circuitry and capacitive loading
- 2^N resistors are required
- b1b2 : Most significant bits in the 4 bit case (selects one single word line.)
- Structure similar to what can be found in digital memories.
- OBS! NMOS switches here
- Number of transistor junctions connected to the output line is now 2 SQRT (2^N), instead of 2^N
- 4 bit case: 8 instead of 16
- 8 bit case: 32 instead of 256
- 10 bit case: 64 instead of 1024
- When a word line goes high, alle the bit lines must be pulled to new levels, limiting speed (no increase equal to the ratio ([2 SQRT (2^N)] / 2^N)

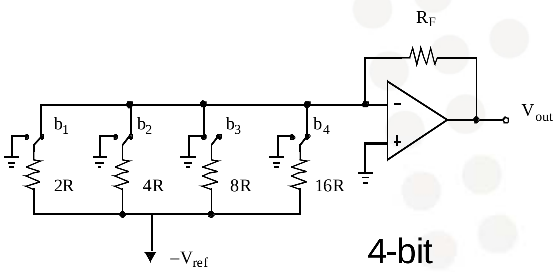
Multiple R-String Converters (12.1)



- A second tapped resistor string is connected between buffers whose inputs are two adjacent nodes of the first resistor string, as shown.
- In this 6-bit case the 3 MSBs determine the two adjacent nodes. The 2nd ("fine") string linearly interpolates between the two adjacent voltages from the first ("coarse") resistor string
- Additional logic needed to handle polarity switching, related to which intermediate buffer has the highest voltage on the input
- Guaranteed monotonicity assuming matched opamps and voltage insensitive offset voltages
- $2 \times 2^{N/2}$ resistors are required
- Relaxed matching requirements for the 2nd resistor string.
- Ex.: 10 bit, 4 bits for the 1st string, matched to 0.1 %. Requirements for 2nd string? $2^4 \times 0.1$ % = 1.6 %

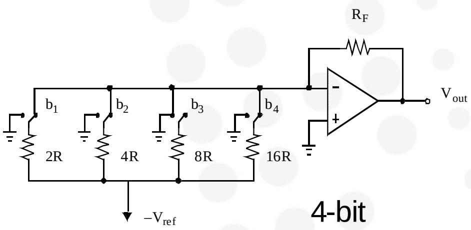
12.2 Binary-Scaled Converters

- Combining a set of signals that are related in a binary fashion
- Typically currents (resistors or plain current) or binary weighted arrays of charges
- Example: 4-bit binary-weighted resistor DAC:



4-bit

Binary-Weighted Resistor Converters (12.2)



4-bit

$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R} - \dots\right)$$

- Few switches and resistors
- Large resistor and current ratios (2^N)
- Monotonicity not guaranteed
- Prone to glitches for high-speed operation

Glitches –from Analog Digital Conversion Handbook

Glitch Impulse Area

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both (see Figure 2.94). This uncontrolled movement of the DAC output during a transition is known as a *glitch*. It can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC operating more quickly than others and producing temporary spurious outputs.

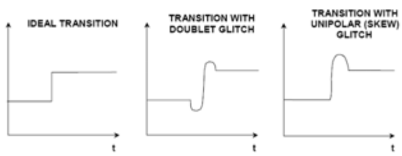


Figure 2.94: *DAC Transitions (Showing Glitch)*

Capacitive coupling frequently produces roughly equal positive and negative spikes (sometimes called a *doublet* glitch) which more or less cancel in the longer term. The glitch produced by switch timing differences is generally unipolar, much larger and of greater concern.

- Glitches waste energy and make noise

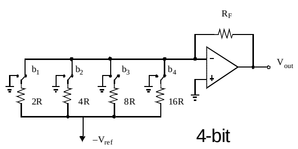
Glitches waste energy and produce noise

- Glitches can be seen as unwanted transitions on the output, instead of a monotonous move from one output value to the next
- Mainly the result of different delays occuring when switching different signals

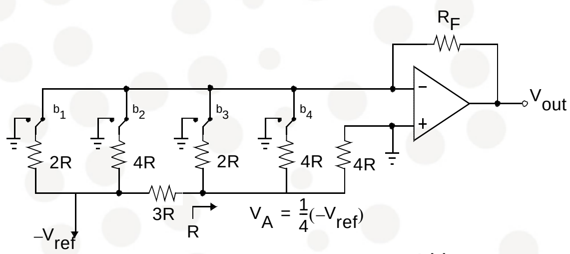
decimal	Binary b1b2b3	Thermometer code d1d2d3d4d5d6d7
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

- Potential cures:
- Exact matching in time (difficult)
- Reducing the bandwidth by placing C accross Rf in a circuit similar to the one in fig. 12.13
- Add S/H to the output
- Modify some or all of the digital word from binary to thermometer code (most popular)

Reduced-Resistance-Ratio Ladders (12.2)



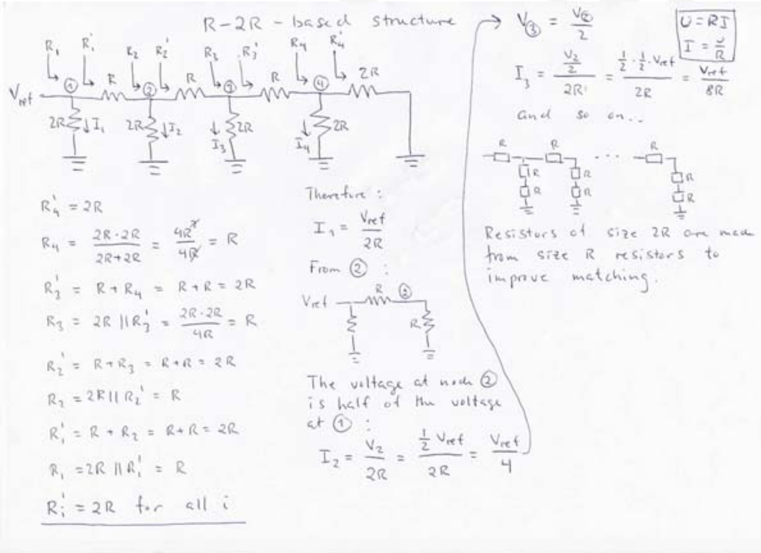
4-bit



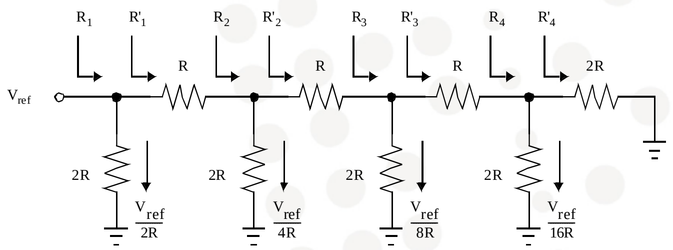
4-bit

- Reducing the large resistor ratios (compared to Fig. 12.7, left) in a binary weighted array by introducing a series resistor (right).
- Same relationship to the digital binary signals as in the previous case, but with one-fourth the resistance ratio
  (4/2 - not 16/2)
  Somewhat similar to the R-2R ladder structure..

R-2R ladder



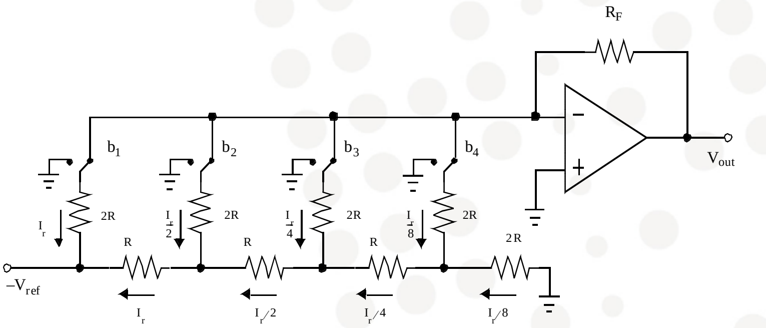
R-2R-Based Converters (12.2)



- Only two resistor values
- Improved matching
- → smaller size and better accuracy

$$R'_4 = 2R$$
$$R_4 = 2R \| 2R = R$$
$$R'_3 = R + R_4 = 2R$$
$$R_3 = 2R \| R'_3 = R$$

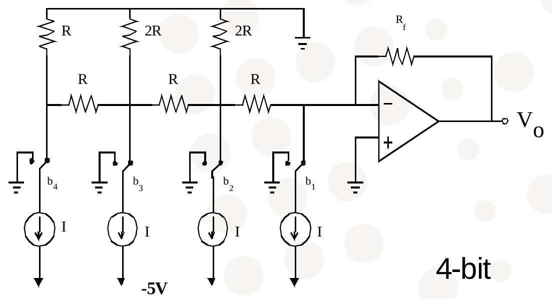
4-bit R-2R Resistor Ladder (12.2)



- The current is scaled by controlling the switches
- Important to scale the switches accordingly
    - Ensuring equal voltage drop across the switches
- Suited for fast operation
    - V_{out} is the only changing voltage

R-2R Resistor Ladder with equal current through all switches

(12.2)



4-bit

- Not necessary to scale switch sizes (Equal current)
- Slower due to changing node voltages

Binary weighted current mode DAC (12.2)(fig. 12.13)

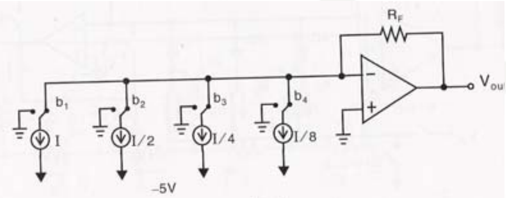
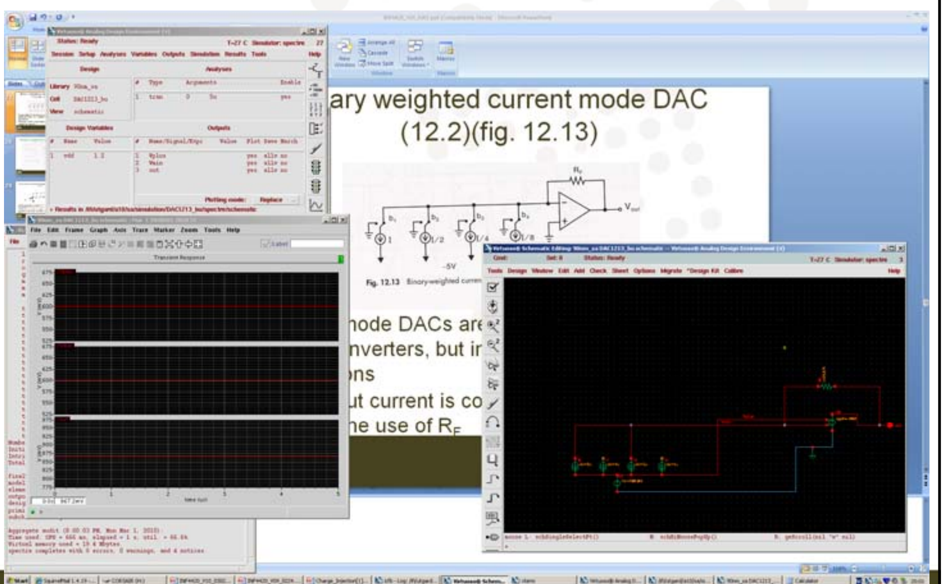


Fig. 12.13 Binary-weighted current-mode D/A converter.

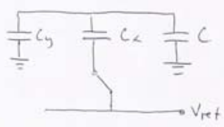
- Current-mode DACs are very similar to resistor-based converters, but intended for higher speed applications
- The output current is converted to a voltage through the use of R_F



Parallel charge sharing DAC principle

PARALLEL CHARGE SCALING DAC

DAC operation based on capacitive voltage division

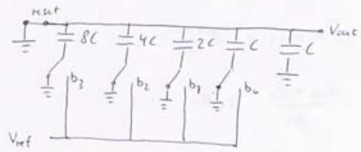


$$V_{out} = \frac{C_x}{C_x + C_y + C} V_{ref}$$

→ Make C_x & C_y function of incoming DAC digital word

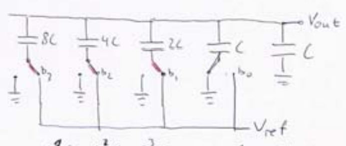
Example: 4-bit DAC, charge scaling

Reset phase:



Charge-phase:

input-code 1110:



$$V_{out} = \frac{2^1 \cdot C + 2^2 \cdot C + 2^3 \cdot C}{2^4 C} V_{ref} = \frac{(2+4+8) \cdot C}{16 C} \cdot V_{ref}$$

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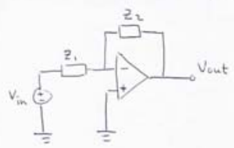
Capacitance ratios defining voltage gain

SWITCHED CAPACITOR GAIN STAGES

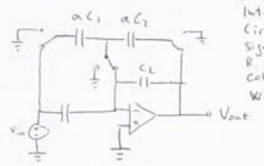


One of the most common functions in analog signal processing is voltage amplification, as shown left (most often used way..)

The input-output relation:

$$\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1}$$

If $Z_2 = k \cdot Z_1$, where k is a constant, a (fixed) gain is achieved.



"Analog MOS Integrated Circuits for Signal processing" R. Gregorian, Gabor C. Temes, Wiley 1986, page 413

SC voltage amplifier

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}$$

$H(z)$ is a frequency independent constant

By switching in different C, the voltage gain may change, depending on dig. input

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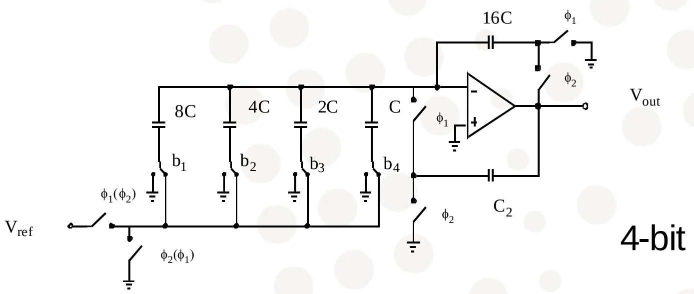
Charge-Redistribution Switched Capacitor Converter (12.2) (fig. 12.12)



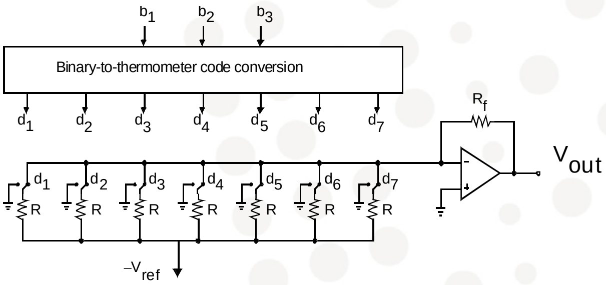
- By replacing the input capacitor of an SC gain amplifier by a programmable capacitor array (PCA) a charge based converter is obtained
- Employs correlated double sampling (CDS) – insensitive to 1/f noise, input-offset voltage and finite amplifier gain.
- An additional sign bit may be realized by interchanging the clock phases
- Carefully generated clock waveforms and a deglitching capacitor are required
- Digital codes must change only when the input-side of the capacitors are connected to ground

Thermometer-Code Converters (Chapter 12.3)- number of 1s represents the decimal value

- + compared to binary counterpart:
- Lower DNL errors
- Reduced glitching noise
- Guaranteed monotonicity
- - compared to binary counterp.:
- Need $2^N - 1$ digital inputs to represent 2^N input values

decimal	Binary b1b2b3	Thermometer code d1d2d3d4d5d6d7
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

Thermometer Based 3-bit DAC (12.3)



- Equal resistor sizes
- Equal switch sizes
- 2^N resistors required

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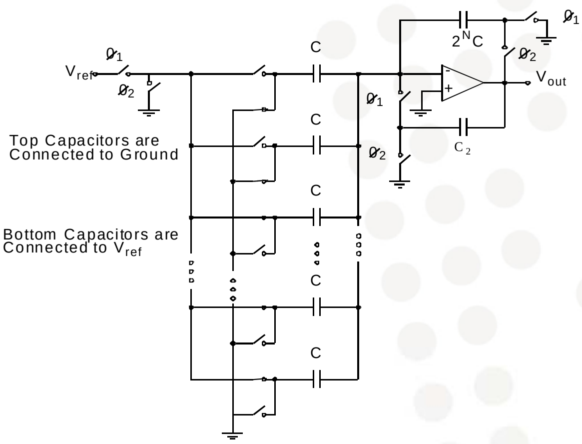
Thermometer-Code Charge-Redistribution DAC (12.3) (Fig. 12.16)



- 2^N capacitors required

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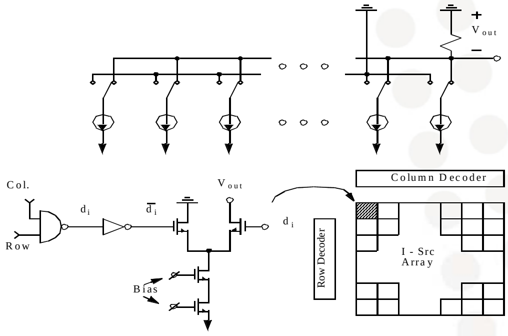
Thermometer-code Current-Mode D/A-Converter (12.3)



- Thermometer-code decoder in both row and column, for inherent monotonicity and good DNL
- Current is switched to the output when both row and column lines for a cell are high
- Cascode current source used for improved current matching
- Suited for high speed, with output fed directly into a resistor (50 or 75 Ohms), instead of an output opamp.
- The delay to all switches must be equal (suppress glitching)
- Important that the edges of d_i and d_i' are synchronized

Thermometer-code Current-Mode DAC - example

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-21, NO. 6, DECEMBER 1986

An 80-MHz 8-bit CMOS D/A Converter

TAKAHIRO MIKI, YASUYUKI NAKAMURA, MASAO NAKAYA, SOTOJU ASAI, YOICHI AKASAKA, AND YASUTAKA HORIBA

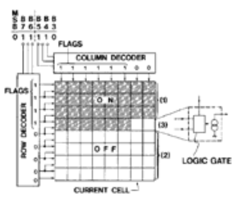


Fig. 2. Two-step decoding.

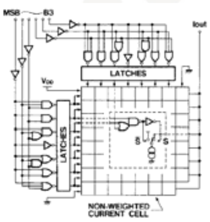


Fig. 3. High-speed decoding circuit.

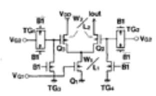


Fig. 4. Circuit diagram of the LSB current source.

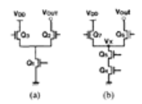


Fig. 5. Configuration of current source. (a) Single-transistor configuration. (b) Cascode configuration.

- Cascode current sources
- Latches connected to decoding
- One gate in the differential pair may be put to a dc level, to improve speed.

TABLE I
CHARACTERISTICS OF THE DAC

Resolution	8 bit
Settling Time	12.5 ns
Rise/Fall Time	5.5 ns
Integral Linearity Error (DC)	0.38 LSB (Typ.)
Differential Linearity Error (DC)	0.22 LSB (Typ.)
Glitch Energy	100 ps·V
Power Consumption	145 mW
Chip Size	1.85 mm x 2.05 mm

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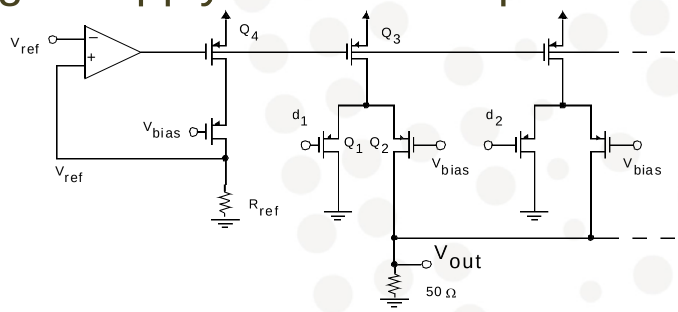
Single-Supply Positive-Output Converters



- For fast single-supply positive-output
- ***One side of each current-steering pair connected to V_{bias}, rather than the inversion of the bit signal***, to maintain current matching. When the current is steered to the output through Q2, the drain-source voltage across the current source, Q3, remains mostly constant if V_{out} stays close to zero, such that Q2 remains in the active region.
- Thus, Q2 and Q3 effectively form a cascode current source when driving current to the output.
- Does not need d_i and $d_{i'}$; reduces complexity and removes the need for precisely timed edges to avoid glitches.

Dynamically Matched Current Sources (12.3)

- for high resolution

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 23, NO. 6, DECEMBER 1988

A Low-Power Stereo 16-bit CMOS D/A Converter for Digital Audio

HANS J. SCHOUWENAARS, SENIOR MEMBER, IEEE, D. WOUTER J. GROENEVELD, AND HENK A. H. TERMEER

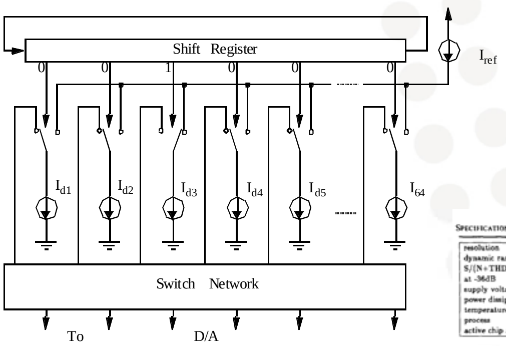


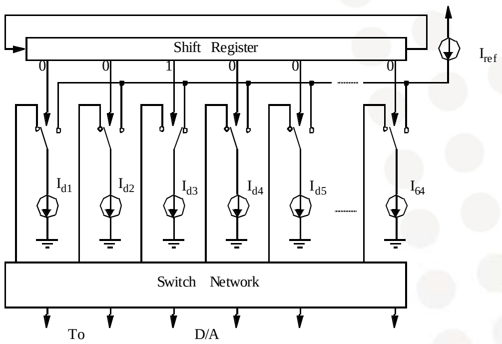
TABLE II
SPECIFICATIONS OF THE D/A CONVERTER

resolution	16 bit
dynamic range	95 dB
S/(N+THD) at 0dB	79 dB
at -36dB	59 dB
supply voltage range	2.5 to 5 V
power dissipation	15 mW at 5 V
temperature range	-20 to 85° C
process	2μm CMOS
active chip area	5 mm²

- Current sources are periodically being regulated to ideally the same value (matched) during normal operation, to ensure proper resolution.
- A "once and for all" matching of each current source is not enough due to mechanisms including temperature drift and gate leakage.

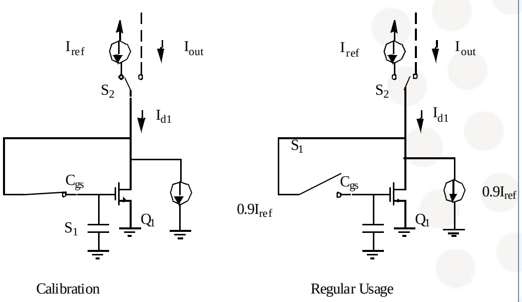
Dynamically Matched Current Sources

(12.3)



- 6 MSB realized using a thermometer code. (binary array for the remaining bits)
- All currents are matched against $I_{ref,}$ one after one, to get the same precise value on all Idi.
- One extra current source is included to provide continous operation, even when one of the sources is being calibrated.

Dynamic matched current sources – method for calibration



- I_{di} is connected to I_{ref} during calibration. This places whatever voltage is necessary across the parasitic C_{gs} so that I_{di} equals I_{ref} . When S_i is opened Idi remains nearly equal to I_{ref}.
- Major limitation in matching the 64 current sources is due to differences in clock feedthrough and charge injection of the switches S_i. → have relatively large C_{gs} and V_{gs} (large V_{gs} so that a certain voltage difference will cause a smaller current deviation.)
- Using $0.9I_{ref}$ in parallell makes Q_1 need only to source a current near 0.1 I_{ref}. With such an arrangement a large low-transconductance device can be used (ex.: W/L=1/8)

12.4 Hybrid Converters

- Combination of different techniques, like for example decoder based, binary scaled, and thermometer-code converters
- Hybrid converters combine the advantages of different approaches for better performance
- Example: Thermometer code used for MSBs, while using a binary-scaled technique for the lower LSBs to reduce glitching. Using binary scaled for the LSBs, where glitching requirements are reduced, may save valuable chip area.

Resistor-Capacitor Hybrid Converters (12.4)

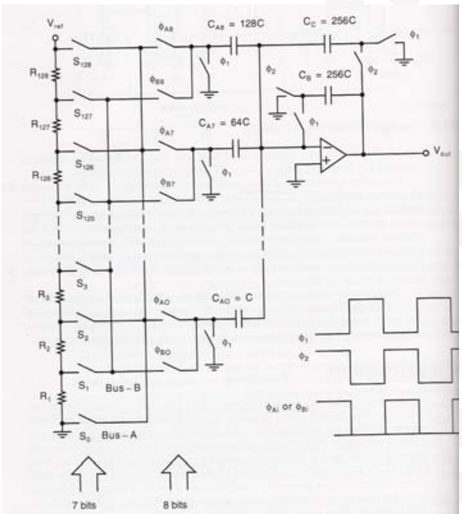


Fig. 12.21 One example of a 15-bit resistor-capacitor hybrid D/A converter.

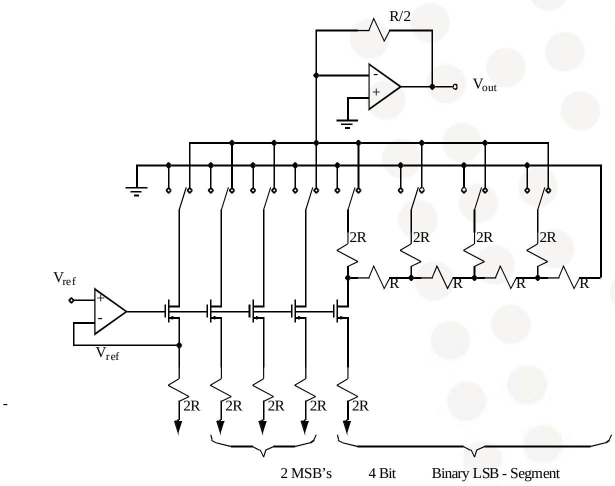
- Top 7 MSBs determine which pair of voltages across a single resistor is passed on to the 8-bit capacitor array.
- A 7-bit resistor-sting DAC is combined with an 8-bit SC binary-weighted DAC for a 15-bit converter
- 15-bit monotonicity, without trimming

High-Resolution Low-Power CMOS D/A Converter

JOHN W. YANG AND KENNETH W. MARTIN, SENIOR MEMBER, IEEE

Abstract —A very low-power, high-resolution, medium-speed D/A converter is described. The converter was realized using a standard analog CMOS technology. It achieved 15-bit monotonicity and less than 0.07-percent overall linearity at a clock frequency of 100 kHz, without requiring any trimming or calibration. The measured SNR was 85 dB, the power dissipation was less than 10 mW, and the distortion for a sinusoidal output was less than 0.04 percent. The D/A converter is intended for battery-powered speech and music synthesis applications where high dynamic range, low power, and low cost are all important.

Segmented Converters (12.4)



- Combination of thermometer- and binary
- 2 MSB's are thermometer (reduces glitches)
- 4 LSB's are binary
- High bits switched to the output, low bits to ground

A few published DACs

Publication year	SFDR @Nyquist [dB]	ENOB @ Nyquist	Nyquist update rate, [Ms/s]	Power consumpt. [mW]	Area [mm²]	Supply voltage [V]	Technology [nm]	other	Reference
2009	>60dB	9.7	1000	188			65	Current steering	Lin et al., ISSCC '09
2008	80	12.9	11	119	0.8	1.8	180	"current steering"	Radulov, APPCAS '08
2007	59	9.5	200 @3.3 V	56	2.25	3.3	180	"current steering"	Mercer, JSCC, Aug.'07
2004	40	6	250	23	0.14	1.8	180	"binary weighted"	Deveugele, JSCC, July '04
2001	61	9.84	1000	110	0.35	3.0	350	"current steering"	Van den Bosch, JSCC, Mar.'01
1988	95	15.45	0.044	15	5	2.5-5	2000		Schouwenaars, JSCC, Dec. '88

Next Tuesday (9/3-08):

- Chapter 13 Nyquist Analog-to-Digital Converters

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Additional litterature

- Phillip E. Allen, Douglas R. Holberg: CMOS Analog Circuit Design, Holt Rinehart Winston, 1987.
- R. Gregorian, G. Temes: Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986
- Leif Hanssen: High Speed Data Converters Fully Integrated in CMOS, dissertation for the dr. scient. Degree, University Of Oslo, 1990.
- A/D , D/A Conversion Handbook, Analog Devices.
- Lecture Notes, University of California, Berkeley, EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/

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Nyquist Rate Analog-to-Digital Converters

Tuesday 9th of March, 2009, 9:15 – 11:00

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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Last time – and today, Tuesday 9th of March:

Last time:
12.1 Decoder-Based Converters
12.2 Binary-Scaled Converters
12.3 Thermometer-Code Converters
12.4 Hybrid Converters

Today – from the following chapters:
13.1 Integrating Converters
13.2 Successive-Approx. Converters
13.3 Algorithmic (or cyclic) A/D Converters
13.4 Flash (or parallel) converters
13.5 Two-Step A/D converters
13.6 Interpolating A/D Converters (16/3-10)
13.7 Folding A/D Converters (16/3-10)
13.8 Pipelined A/D Converters
13.9 Time-Interleaved A/D Converters

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Different A/D Converter Architectures

Low-to-Medium Speed High Accuracy	Medium Speed Medium Accuracy	High Speed Low-to-Medium Accuracy
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-Step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

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Different ADCs depending on needs

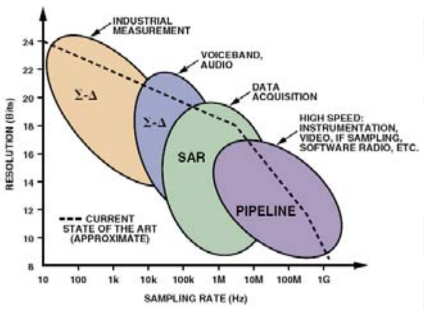

Figure 1. ADC architectures, applications, resolution, and sampling rates.

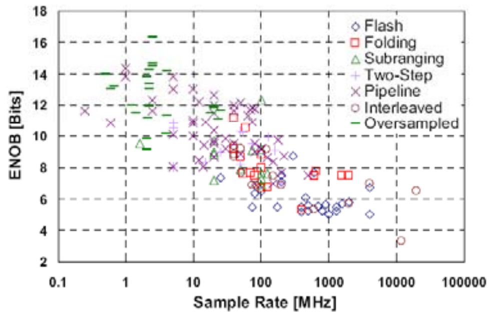

Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

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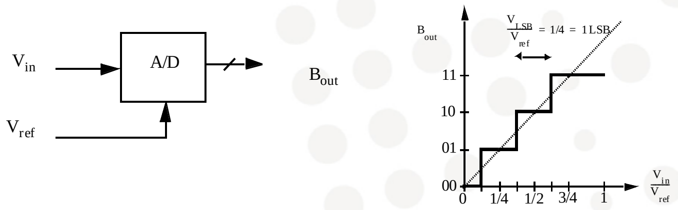
A/D-conversion – Basic Principle



$$V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}) = V_{in} \pm x$$

$$\text{where } \left(-\frac{1}{2}V_{LSB} < x < \frac{1}{2}V_{LSB}\right)$$

- The analog input value is mapped to discrete digital output value
  - Quantization error is introduced

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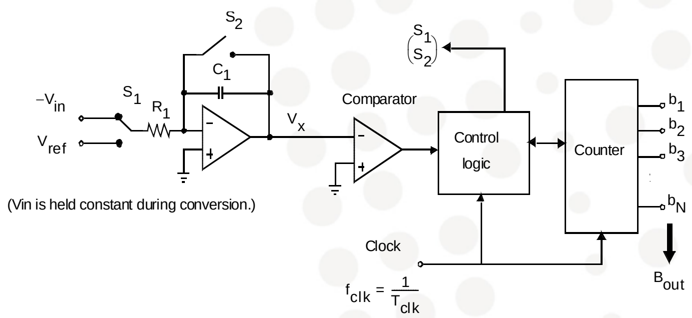
Integrating Converters (13.1)



- $V_x(t) = V_{in}\, t / RC$ (V_x ramp derivative depending on V_{in})
- High linearity and low offset/gain error
- Small amount of circuitry
- Low conversion speed
  - $2^{N+1} * 1/T_{clk}$ (Worst case)

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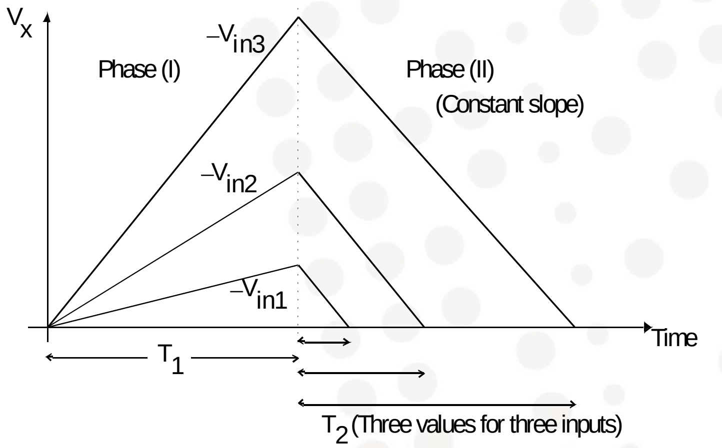
Integrating Converters



- The digital output is given by the count at the end of T_2
- The digital output value is independent of the time-constant RC

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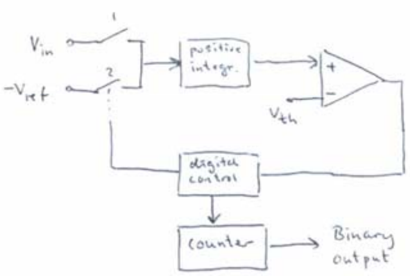
Dual slope ADC

POSITIVE INTEGRATOR USED IN DUAL-SLOPE ADCS

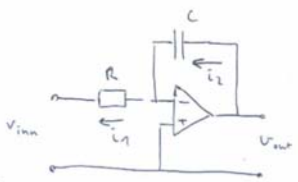


$$v_{out} = \frac{1}{RC}\int_0^t v_{inn}\,dt$$

$$= \frac{V_{in}}{RC}\,t$$

Example: 16-bit two-slope ADC with $V_{in} = 3V$, $V_{xmax} = 4V$ and $T_1 = 20ms$. RC - constant? Clock fr?

$$f_{clk} = \frac{1}{T_{clk}} = \frac{2^{16}}{20ms} \approx \underline{3.28\ MHz}$$



$$i_1 = i_2$$

$$\frac{v_{inn}}{R} = C\frac{dv_{out}}{dt}$$

$$\Updownarrow$$

$$\frac{dv_{out}}{dt} = \frac{v_{inn}}{RC}$$

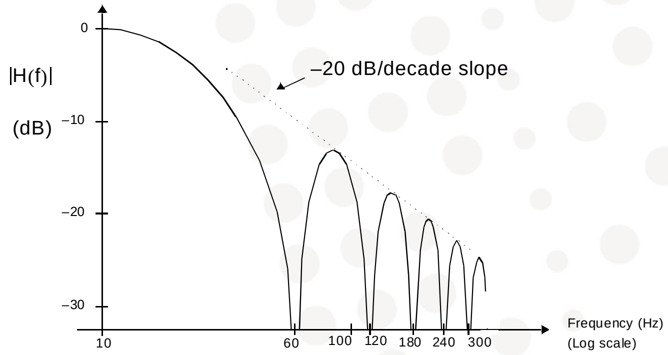
equation (17.15):

$$V_x = \frac{V_{in}T_1}{RC} \Leftrightarrow 4V = \frac{3V\ 20ms}{RC}$$

$$\Updownarrow$$

$$\underline{RC = 15ms}$$

Integrating Converters – careful choice of T1 can attenuate frequency components superimposed on the input signal



- In the above case, 60 Hz and harmonics are attenuated when T1 is an integer multiple of 1/60 Hz.
- Sinc-response with rejection of frequencies multiples of $1/T_1$

Successive approx ADC algorithm (13.2)

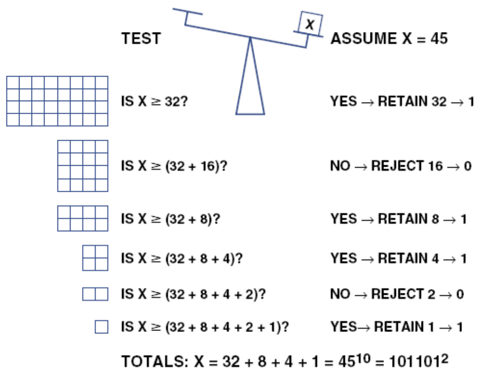


Figure 4. Successive-approximation ADC algorithm using balance scale and binary weights.

Which ADC Architecture Is Right for Your Application?

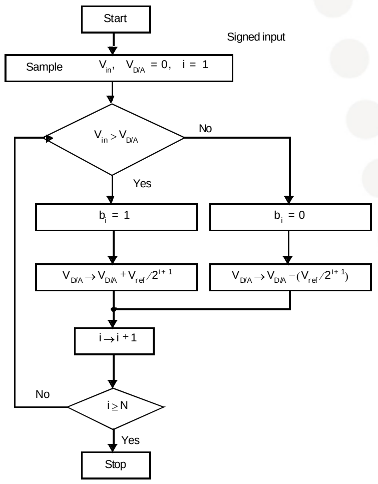
By Walt Kester [walt.kester@analog.com]

- If we have weights of 1 kg, 2 kg, 4 kg, 8 kg, 16 kg, 32 kg and will find the weight of an unknown X assumed to be 45 kg.
- 101101_2

=1*32+0*16+1*8+1*4+0*2+1*1

= 45_{10}

Successive-Approximation Converters



- Uses binary-search algorithm
- Accuracy of 2^N requires N steps
- The digital signal accuracy is within +/- 0.5 V_{ref}
- Medium speed
- Medium resolution
- Relatively moderate complexity

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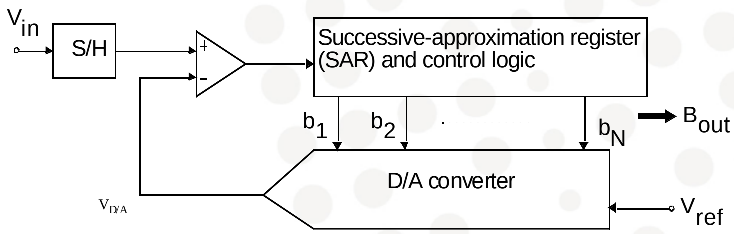
DAC-Based Successive Approximation



- $V_{D/A}$ is adjusted until the value is within 1LSB of V_{in}
- Starts with MSB and continues until LSB is found
- Requires DAC, S/H, Comparator and digital logic
- The DAC is typically limiting the resolution

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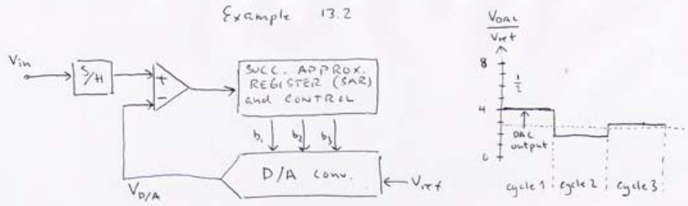
Succ. Approx ADC, example 13.2

Example 13.2



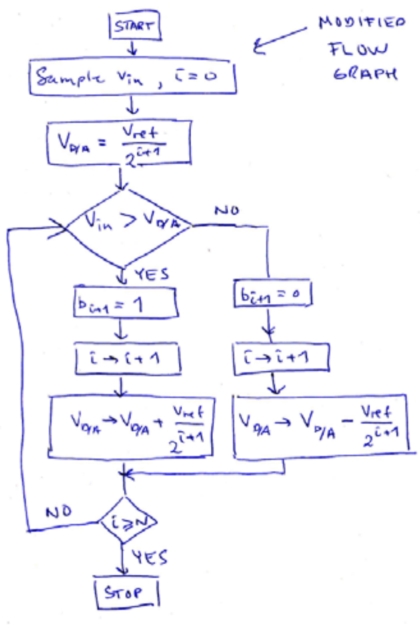
$V_{ref} = 8V$
$V_{in} = 2.831\,V$
3-bit conversion

cycle 1: $B_{out} = 100$, so that $V_{D/A} = 4.0\,V$. Since $V_{in} < V_{D/A}$, $b_1 \to 0$

cycle 2: $B_{out} = 010$, so that $V_{D/A} = 2.0\,V$. Since $V_{in} > V_{D/A}$, $b_2 \to 1$

cycle 3: $B_{out} = 011$, — " " — $3.0\,V$. Since $V_{in} < V_{D/A}$, $b_3 \to 0$

$\underline{010}$



Ex. 13.2

$V_{ref} = 8V$, $V_{in} = 2.831\,V$

$V_{D/A} = \frac{V_{ref}}{2^{i+1}} = \frac{8V}{2^1} = 4V$

$V_{in} > V_{D/A} \Leftrightarrow 2.831\,V > 4V\,? \to$ NO!

$b_{i+1} = b_{0+1} = b_1 = 0$

$i \to i+1 = 0+1 = 1$

$V_{D/A} \to 4V - \frac{8}{2^2}V = 4V - 2V = 2V$

$i = 1 \geq 3\,? \to$ NO

$V_{in} > V_{D/A} \Leftrightarrow 2.831\,V > 2V\,? \to$ YES!

$b_{i+1} = b_{1+1} = 1$; $b_2 = 1$

$i \to i+1 = 1+1 = 2$

$V_{D/A} \to V_{D/A} + \frac{V_{ref}}{2^{i+1}} = 2V + \frac{8}{2^{2+1}}V = 2V + 1V = 3V$

$i = 2$, $2 \geq 3\,?$ NO!

$V_{in} > V_{D/A} \Leftrightarrow 2.831\,V > 3V\,?$ — NO!

$b_3 = 0$

$i \to 2+1$

$V_{D/A}$ update, $3 \geq 3 \Rightarrow$ STOP

Charge-Redistribution A/D-Converter (unipolar)

- Instead of using a separate DAC and setting it equal to the input voltage (within 1 LSB) as for the DAC based converter from figure 13.5, one can use the error signal equaling the difference between the input signal, V_{in}, and the DAC output, $V_{D/A}$

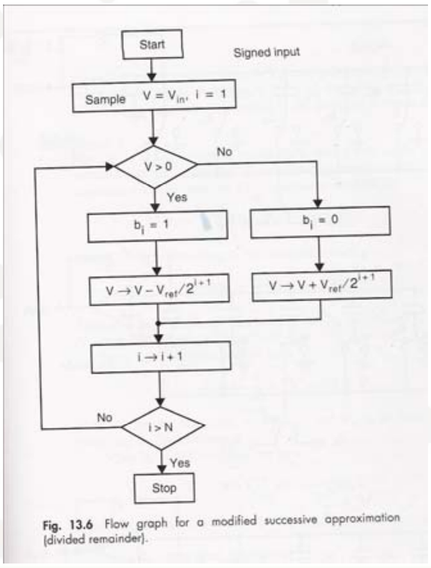


Fig. 13.6 Flow graph for a modified successive approximation (divided remainder).

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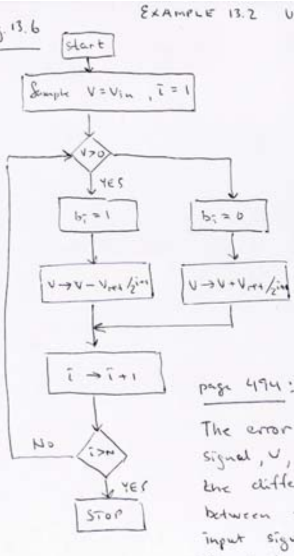
Numbers from 13.2 setting an error signal V equal to $V_{in} - V_{D/A}$ – modified succ. approx as in fig. 13.6

EXAMPLE 13.2 USING MODIFIED SUCC. APPROX (DIVIDED REMINDER)

Fig. 13.6



page 494:

The error signal, V, equals the difference between the input signal, V_{in}, and the D/A output

Error signal, $V = V_{in} - V_{DAC}$

$V = +2.831V - 4V = -1.169V$

$-1.169 > 0$? NO , $b_1 = 0$

$V \to -1.169V + 2V = 0.831V$

$i = i + 1 = 2$

$i = 2 > 3$? NO

$0.831V > 0$?

YES

$b_2 = 1$

$V \to (0.831 - 8/8)V = -0.169V$

$i = 2 + 1 = 3$

$i > 3$?

NO

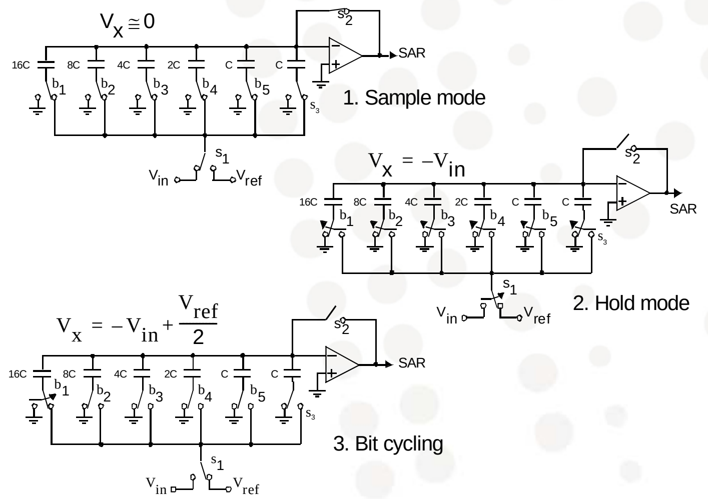
$-0.169V > 0$?

NO $\to b_3 = 0$

$b_1 b_2 b_3 = 010$

(like in ex. 13.2)

Unipolar Charge-Redistribution A/D-Converter



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Charge-Redistribution A/D-Converter

- Sample mode:
  - All capacitors charged to Vin while the comparator is reset to its threshold voltage through S_2. The capacitor array is performing S/H operation.
- Hold mode:
  - The comparator is taken out of reset by opening S_2, then all capacitors are switched to ground. V_x is now equal to $-V_{in}$. Finally S_1 is switched so that V_{ref} can be applied to the capacitors during bit-cycling.
- Bit-cycling:
  - The largest capacitor is switched to V_{ref}. V_x goes to $-V_{in} + V_{ref}/2$. If V_x is negative, then V_{in} is greater than $V_{ref}/2$ and the MSB capacitor is left connected to V_{ref}. Otherwise the MSB capacitor is disconnected and the same procedure is repeated N times

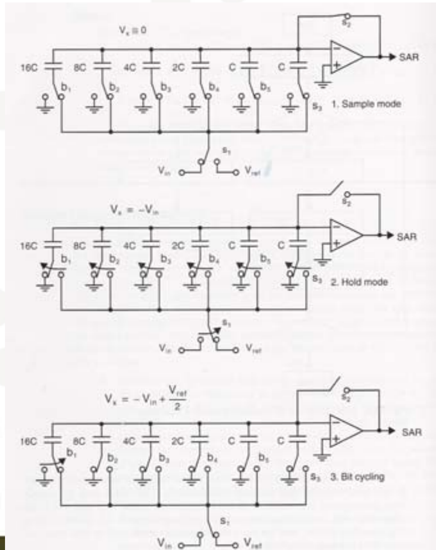

Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

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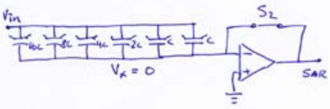
EX. 13.3 pp. 497

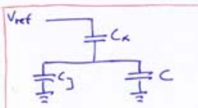
Find intermediate node voltages at V_x during the operation of the 5-bit charge-redistribution converter shown in fig. 13.7. Assume $8C$ as a parasitic cap. at V_x

$V_{ref} = 5V$, $V_{in} = 1.23V$

SAMPLE MODE :



Top-plates to V_-, to minimize parasitic capacitance at node V_x.

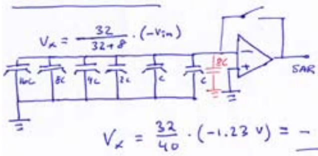


$$V_{out} = \frac{C_x}{C_x + C_y + C} \cdot V_{ref}$$

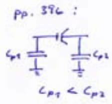
C_x and C_y functions of digital word/switching

HOLD MODE :

$$V_x = \frac{32}{32+8} \cdot (-V_{in})$$



pp. 396 :



$C_{p1} < C_{p2}$

1) Sample mode
2) Hold mode
3) Bit - cycling

$$V_x = \frac{32}{40} \cdot (-1.23\,V) = \underline{-0.984\,V}$$

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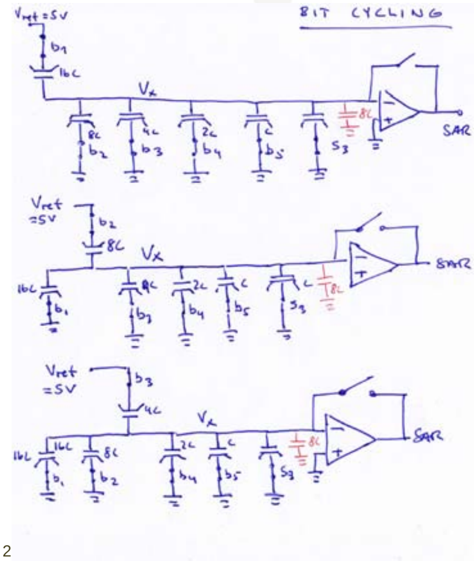
BIT CYCLING



- b_1 is switched, controlling the 16C capacitor:

$$V_x = -0.984V + \frac{16}{(32+8)} \cdot 5V$$
$$= -0.984\,V + 2V = 1.016V$$

$V_x > 0 \Rightarrow \underline{b_1 = 0}$

- $$V_x = -0.984V + \frac{8}{(32+8)} \cdot 5V$$

$V_x = -0.984V + 1V = 0.016\,V$

When b_2 is switched $V_x > 0$, so $b_2 = 0$ and V_x is set back to -0.984 V by switching b_2 back to gnd.

- b_3 is switched :

$V_x = -0.984\,V + \frac{4.5}{40} V = -0.484V$

V_x is now $< 0 \Rightarrow b_3 = 1$ and b_3 left connected to V_{ref}.

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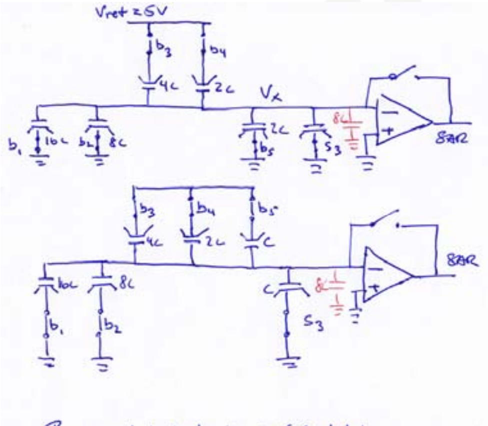


• b_4 is switched:

$V_x = -0.984V + \frac{6}{40} \cdot 5\,V =$

$-0.984V + 0.75V = -0.234V$

$V_{x_4} < 0 \Rightarrow \underline{b_4 = 1}$

• b_5 is switched:

$V_{x_5} = -0.234V + \frac{1}{40} \cdot 5V = -0.109V$

$V_{x5} < 0 \Rightarrow \underline{b_5 = 1}$

May also be expressed from the drawing and the orig.

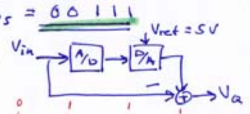
$\underbrace{\text{Sampled}}$ volt.:

$\frac{32}{32+8}(-V_{in}) + \frac{7}{32+8} \cdot 5V =$

$-0.984V + 0.875V = -0.109V$

$\underline{B_{out}} = b_1 b_2 b_3 b_4 b_5 = \underline{0\,0\,1\,1\,1}$

$\frac{5V}{2^5} = \frac{5V}{32} = 0.15625\,V$



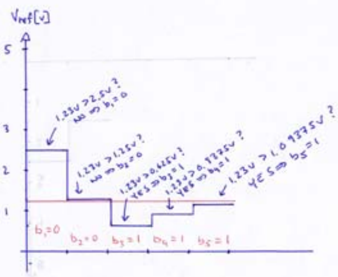
DAC: $V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 \cdot 2^{-3} + b_4 \cdot 2^{-4} + b_5 \cdot 2^{-5})$

$= 5 * (0.125V + 0.0625V + 0.03125V) = 5V(0.21875) = 1.09375\,V$

$V_a = 1.09375V - 1.23V = -0.13625$

Succc. Approx. Approach flow graph

EX. 13.3 VIEWED IN ANOTHER WAY, AND WITHOUT PARASITICS.



$V_{in} = 1.23\ V$

$V_{ref} = 5V$

5V : 2 = 2.5V

2.5V : 2 = 1.25V

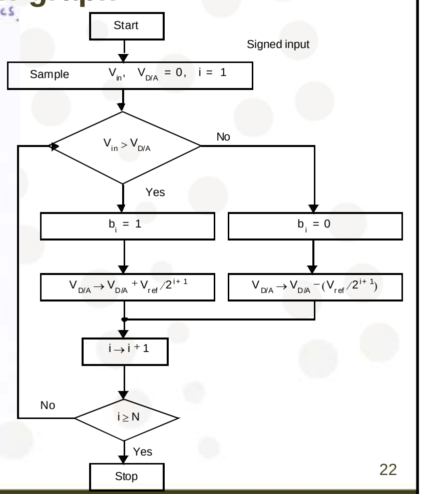
1.25V : 2 = 0.625V

1.25V : 4 = 0.3125V

5V : 32 = 0.15625V

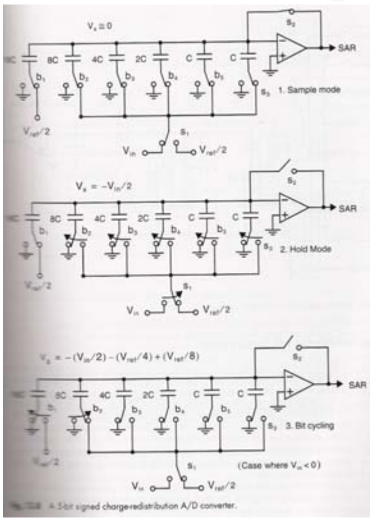
$(0.625 + 0.3125)V = 0.9375V$

$(0.625 + 0.3125 + 0.15625)V = 1.09375V$



Signed Charge redistribution A/D

(Fig. 13.8)



- Resembling the unipolar version (Fig. 13.7)
- Assming V_{in} is between +/- $V_{ref}/2$
- Disadvantage: V_{in} attenuated by a factor 2, making noise more of a problem for high resolution ADCs
- Any error in the MSB capacitor causes both offset and a sign-dependent gain error, leading to INL errors

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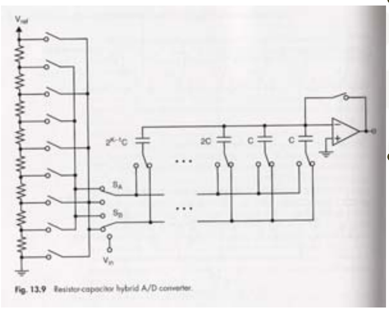
Resistor-Capacitor Hybrid (figure 13.9 in "J & M")



- First all capacitors are charged to V_{in} before the comparator is being reset.
- Next a succ. approx. conversion is performed to find the two adjacent resistor nodes having voltages larger and smaller than V_{in}
- One bus will be connected to one node while the other is connected to the other node. All of the capacitors are connected to the bus having the lower voltage.
- Then a successive approximation using the capacitor-array network is done, starting with the largest capacitor…

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Speed estimate for charge-redistribution converters

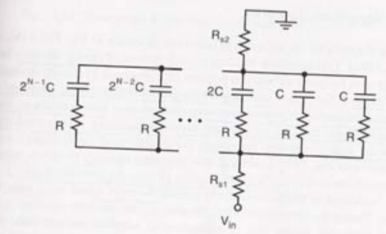

Fig. 13.12 Simplified model of a capacitor array during the sampling time.

- RC time constants often limit speed
- Individual time constant due to the 2C cap.: $(R_{s1}+R+R_{s2})2C$
- (R ; bit line)
- $Tau_{eq}=(R_{s1}+R+R_{s2})2^NC$, for the circuit in fig. 13.12
- For better tha 0.5 LSB accuracy: $e^{-T/Tau_{eq}} < 1/(2^N+1)$, T = charging time
- $T > Tau_{eq}\,(N+1)\ln 2$

  $= 0.69(N+1)Tau_{eq}$

- 30 % higher than from Spice simulations (”J & M”)

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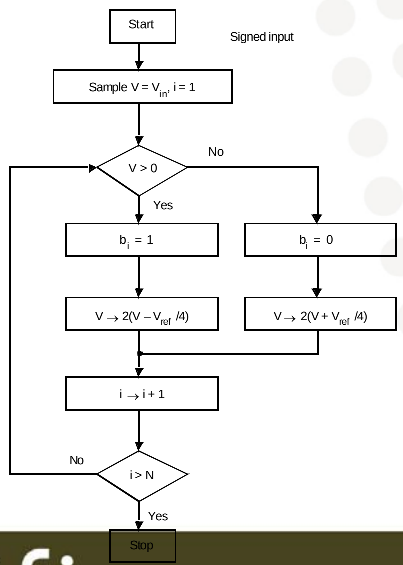
Algorithmic (or Cyclic) A/D Converter (13.3)



- Similar to the Successive approximation converter
- Constant V_{ref}
- Doubles the error each cycle, instead of halving the reference voltage in each cycle, like succ. approx. conv.
- Requires an accurate multiply-by-2 amplifier
- Accuracy can be improved by operating in four cycles (instead of two)
- compact

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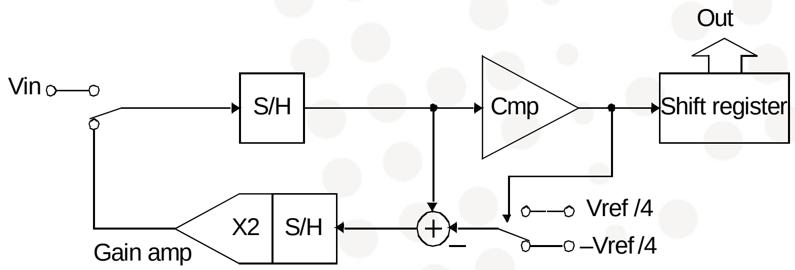
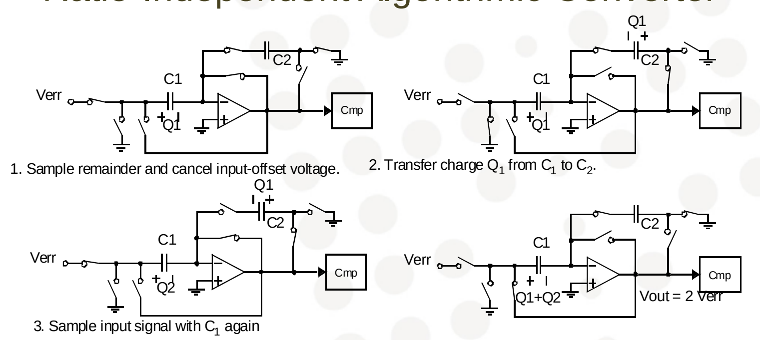
Ratio-Independent Algorithmic Converter



- Simple circuitry
- Due to the cyclic operation the circuitry are reused in time
- Fully differential circuits normally used

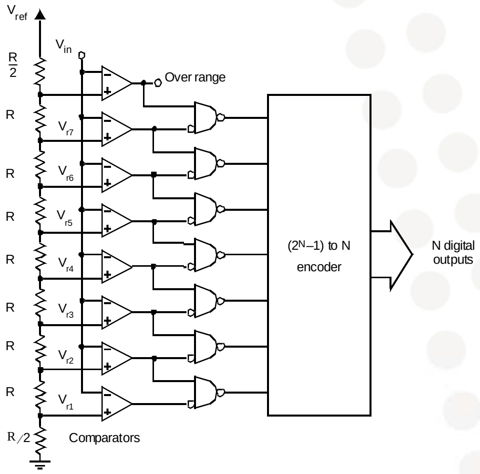
Ratio-Independent Algorithmic Converter



1. Sample remainder and cancel input-offset voltage.
2. Transfer charge Q_1 from C_1 to C_2.
3. Sample input signal with C_1 again after storing charge Q_1 on C_2.
4. Combine Q_1 and Q_2 on C_1, and connect C_1 to output.

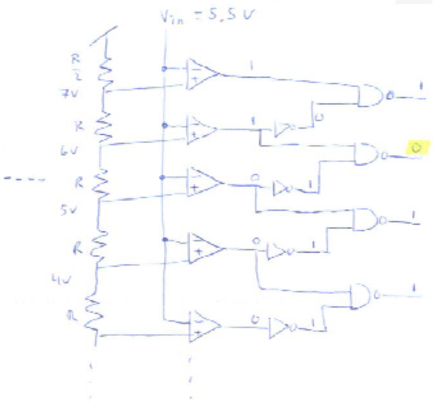
- The basic idea is to sample the input signal twice using the same capacitor. During the 2nd sampling the charge from the 1st capacitor is stored on a 2nd capacitor whose size is unimportant. After the 2nd sampling both charges are recombined into the 1st capacitor which is then connected between the opamp input and output.
- Does not rely on capacitor matching, is insensitive to amplifier offset.

Flash (Parallel) Converters (13.4)



- High speed – among the fastest
- 2^N comparators in parallel, each connected to different nodes – area consuming
- High power consumption
- Thermometer-code output fed into decoder
- Nands used for simpler decoding and error detection (bubble error)
- Differential comparator required to ensure sufficient PSSR
- Top and bottom resistors chosen to create the 0.5 LSB offset in an A/D converter

Flash converter



One NAND-gate will have a 0 output

All other NAND-gate outputs will be 1.

This also allows for error checking by checking for more than one 0 output.

(See fig 13.16 page 508)

Any comparator connected to a resistor string node where V_{ri} is larger than V_{in} will have a 1 output.

Clocked CMOS comparator

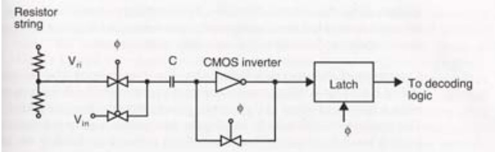


Fig. 13.17 A clocked CMOS comparator.

- When the clock ("phi") is high, the inverter is set to its bistable point, Vin = Vout (= Vdd/2). The other (left) side of C is charged to V_{ri}.
- When the clock ("phi") goes low, the inverter switches, depending on the voltage difference between V_{ri} and V_{in}. ($V_{ri} > V_{in}$; 1 output, $V_{ri} < V_{in}$; 0 output from inv.)
- Differential inverters helps poor PSRR with this simple comparator solution.

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Issues in Designing Flash A/D Converters

- **Input Capacitive Loading:** The large number of comparators connected to Vin results in a large capacitive load on at the input node which increases power and reduces speed
- **Comparator Latch-to-Track Delay:** The internal delay in the comparator when going from latch to track mode
- **Signal and/or Clock Delay:** Differences in signal/clock delay between the comparators may cause errors. Example: A250-MHz, 1-V peak input-sinusoid converted with 8-bit resolution requires a precision of 5ps. Can be reduced by matching the delays and capacitive loads on the signal/clock.
- **Substrate and Power-Supply Noise:** For a 8-bit converter with Vref=2V only 7.8mV of noise injection is required to introduce an error of 1LSB. The problem can be reduced by proper layout (Shielding, Differential clocks, Separate power supplies, and symmetrical layout)
- **Bubble Error Removal:** Comparator metastability may introduce wrong thermometer code (a single 1 or 0 in between opposite values)
- **Flashback:** Caused by latched comparators. When the comparator is switched from track to latch mode a charge glitch is introduced at the input. The problem is reduced by using a preamplifier and input impedance matching

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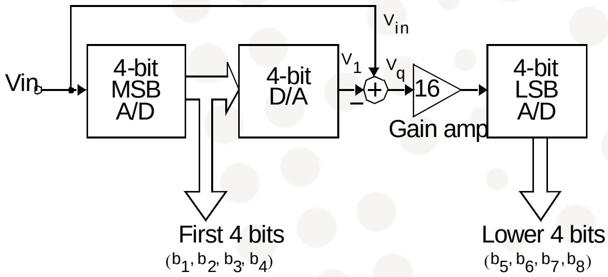
Two-Step (Subranging) A/D Converters (13.5)



- Popular choice for high-speed medium accuracy converters (8-10 b)
- Less area and power consumption than a Flash ADC
- The MSB's are converted during the first step. In the next step the remaining error is converted into the LSB's
- Speed is limited by the Gain Amplifier
- Requires N-bit accuracy for all components (May be relaxed by using Digital Error Correction)

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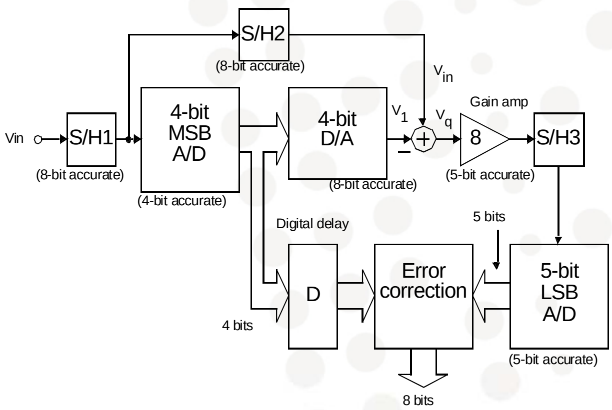
Digital Error Correction for two-step A/D



- The accuracy requirements on the input ADC is relaxed due to the error corr.. 4-bit for MSb converter

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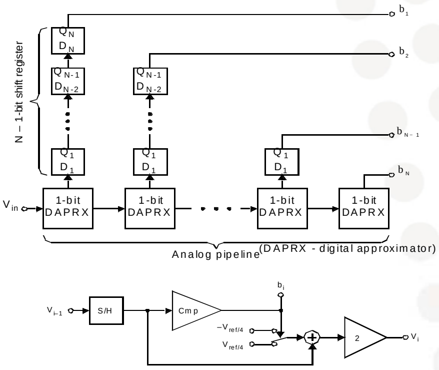
Pipelined ADCs (13.5) Once the first stage has completed it's work it immediately starts working on the next sample



- Small area

The pipelined ADC has its origins in the *subranging* architecture, first used in the 1950s. A block diagram of a simple 6-bit, two-stage subranging ADC is shown in Figure 11.

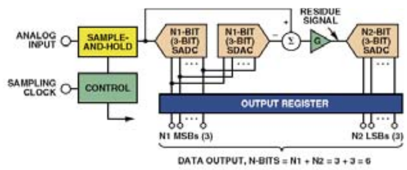
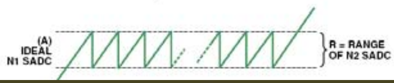


Figure 11. 6-bit, two-stage subranging ADC.

The output of the SHA is digitized by the first-stage 3-bit sub-ADC (SADC)—usually a flash converter. The coarse 3-bit MSB conversion is converted back to an analog signal using a 3-bit sub-DAC (SDAC). Then the SDAC output is subtracted from the SHA output, the difference is amplified, and this "residue signal" is digitized by a second-stage 3-bit SADC to generate the three LSBs of the total 6-bit output word.



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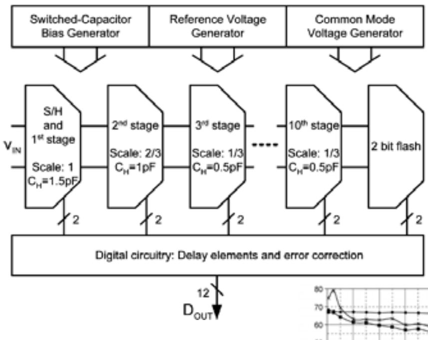
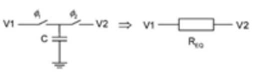
Pipelined ADC -example

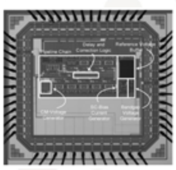
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor







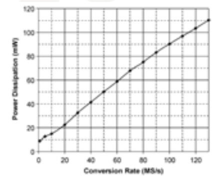


Fig. 7. Power dissipation versus conversion rate. The input frequency and signal swing is 10 MHz and 2V_{P-P}, respectively.

Nominal sampling rate	110MS/s
Technology	0.18µm digital CMOS
Nominal supply voltage	1.8V
Resolution	12bit
Full scale analog input	$2V_{P-P}$
Area	$0.86mm^2$
Power consumption	97mW
DNL	±1.2 LSB
INL	-1.5/+1 LSB
SNR (f_{in}=10MHz)	67.1 dB
SNDR (f_{in}=10MHz)	64.2 dB
SFDR (f_{in}=10MHz)	69.4 dB
ENOB (f_{in}=10MHz)	10.4 bit

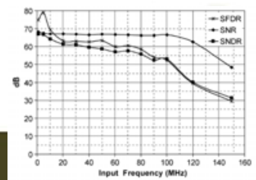


Fig. 9. SFDR, SNR, and SNDR versus input frequency. The conversion rate and signal swing are 110 MS/s and 2V_{P-P}, respectively.

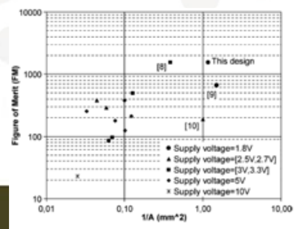
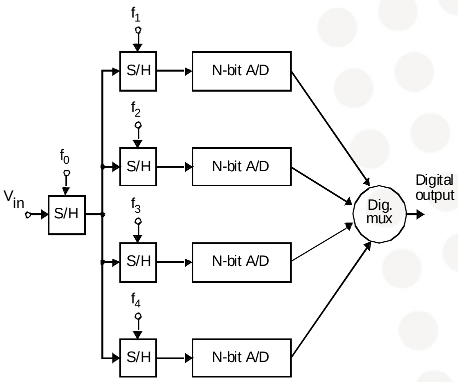


Fig. 12. Figure of Merit (FM) versus 1/A for 12-bit ADCs. f_{CR} is given in MS/s, A is given in mm² and P_{TOT} is given in mW.

Time-Interleaved A/D-converter (13.9)



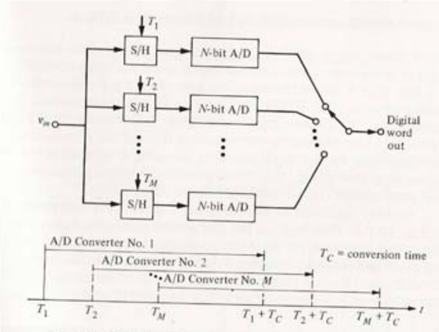


Figure 10.7-2 A time-interweaved A/D converter array.

- Very high speed (figure to the right from "Allen & Holberg")
- f_0 is four timer higher than $f_1 - f_4$, which in addition is slightly delayed
- Only the S/H and the MUX must run on the highest frequency
- Tones are introduced at multiples of f_0/N

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Time-Interleaved – best compromise between complexity and sampling rate – may be used for different architectures [Elbjornsson '05]

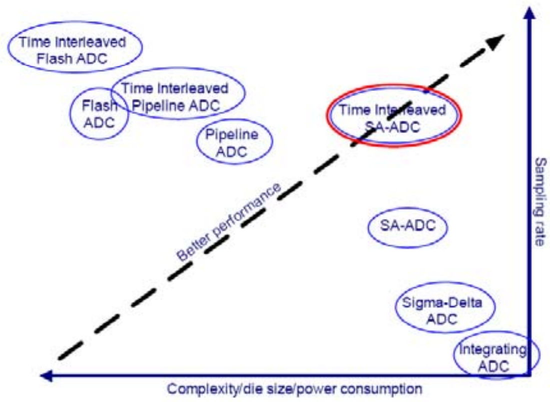

Figure 7 Comparison between ADC architectures. The time interleaved successive approximation ADC gives the best compromise between complexity and sampling rate.

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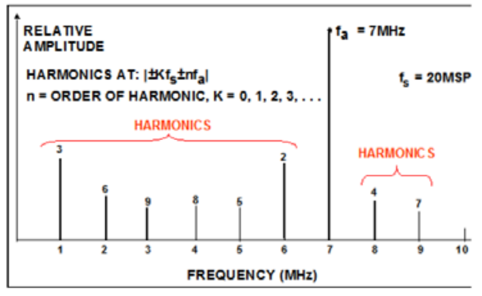
Dynamic range

- Dynamic range is defined as the power of the maximum input signal range divided by the total power of the quantization noise and distortion
- Often referred to as Signal-to-Noise-and-Distortion range
- S/(N+D)
- SINAD



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Analog and digital supply voltages are reduced as technology scales

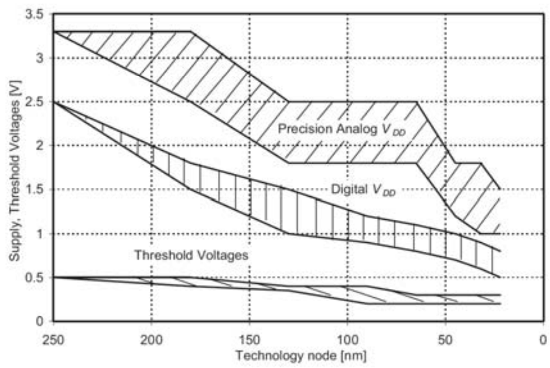

Fig. 1. Scaling of supply and threshold voltages.

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [2]
[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

Some ADC trends:

- Limited dynamic range at low supply voltages remains the utmost challenge for high-resolution Nyquist converters.
- Oversampling converters will dominate this arena in the future
- Linearity correction with digital correction is becoming prevalent

22. mai 2010 40

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Nyquist ADCs at ISSCC; FOM, Effective Number of Bits

$$\mathrm{FOM} = \frac{P}{2^{2\mathrm{ENOB}} f_s}.$$

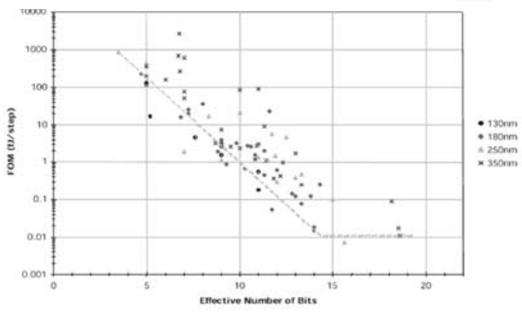

Fig. 22. *FOM as a function of effective number of bits and technology.*

Analog Circuit Design in Nanoscale CMOS Technologies

Classic analog designs are being replaced by digital methods, using nanoscale digital devices, for calibrating circuits, overcoming device mismatches, and reducing bias and temperature dependence.

By Lanny L. Lewyn, *Life Senior Member IEEE*, Trond Ytterdal, *Senior Member IEEE*, Carsten Wulff, *Member IEEE*, and Kenneth Martin, *Fellow IEEE*

- FOM: Figure of Merit
- High-resolution conv.: FOM minimum at about 10^{-17}J/step
- 6-bit ADCs : FOM about 4 orders of magnitude worse than 14 bit converters, suggesting that there is much to be gained by designing more effecient 6-bit ADCs
- Better ENOB reported for 350 nm than 250 nm, 180 nm and 130 nm
- Data from ISSCC up to 2005.

Nyquist ADCs at ISSCC; FOM, Sampling rate

$$\mathrm{FOM} = \frac{P}{2^{2\mathrm{ENOB}} f_s}.$$

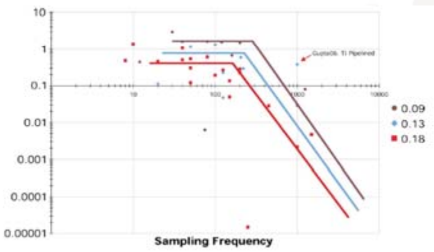

Fig. 23. *FOM cliff for Nyquist ADCs in ISSCC 2000-2007.*

Vol. 97, No. 10, October 2009 | Proceedings of the IEEE

- Maximum Sampling frequency (Usually faster is better) and FOM.
- ISSCC 2000-2007 (90 nm, 130 nm, 180 nm technologies)
- Small improvement in sampling frequency in going to finer technologies, mainly due to reduced capacitance.

Analog Circuit Design in Nanoscale CMOS Technologies

Classic analog designs are being replaced by digital methods, using nanoscale digital devices, for calibrating circuits, overcoming device mismatches, and reducing bias and temperature dependence.

By Lanny L. Lewyn, *Life Senior Member IEEE*, Trond Ytterdal, *Senior Member IEEE*, Carsten Wulff, *Member IEEE*, and Kenneth Martin, *Fellow IEEE*

Publication year	SFDR @Nyquist [dB]	ENOB @ Nyquist	Nyquist update rate, [Ms/s]	Power consumpt. [mW]	Area [mm²]	Supply voltage [V]	Technology [nm]	other	Reference
2006	55	8.5	1000	250	3.5	1.2	130	Time interleaved	Gupta et al IEEE JSSC '06
2007		4	2500	24	0.057	1.2	130	"Pipelined flash"	Wang et al, IEEE Trans. Instr. Meas.
2007		5	500	6	0.9	1.2	65	Time interleaved succ. approx	Ginsburg et al IEEE JSSC '07
2007		8	100	30	2.04	1.0	180	Switched opamp pipelined	Wu et al, IEEE JSSC '07
2008		10	30	22	0.7	1.8	180	pipelined	Li et al, IEEE JSSC '08
2009	81	13		0.073		0.7	180	Delta-sigma	Chae, JSSCC Feb.09
2009	27.5	4.3	1750	2.2	0.02	1.0	90	"folding flash"	Verbruggen, JSSCC, Mar. '09
2009	10		1.2	12.2	0.354	3.3	350	Continous time sigma delta	TCAS-II, Jan. '09

Sampling-time uncertainty

•Variation in output voltage caused by variations in the time of sampling

Consider the following input signal: $V_{in} = \frac{V_{ref}}{2}\sin(2\pi f_{in} t)$

If the variation in sampling time is Δt, following equation must be satisfied to keep ΔV less than 1LSB

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

Additional litterature

- Phillip E. Allen, Douglas Holberg: CMOS Analog Circuit Design, Holt Rinehart Winston, 1987.
- Jonas Elbornsson: White paper on parallel successive approximation ADC, Mathcore Engineering AB, 2005.
- R. Gregorian, G. Temes: Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986
- D. M.Gingrich Lecture Notes, University of Alberta, Canada http://www.piclist.com/images/ca/ualberta/phys/www/http/~gingrich/phys395/notes/phys395.html
- Walt Kester: Which ADC is right for your application?
- Y. Chiu, B. Nicolic, P. R. Gray: Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS, Proceedings of Custom Integrated Circuits Conference, 2005.
- Lecture Notes, University of California, Berkeley,
  EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/
- Lanny L. Lewyn, Trond Ytterdal, Carsten Wulff, Kenneth Martin: "Analog Circuit Design in Nanoscale CMOS Technologies", Proceedings of the IEEE, October 2009.
- James L. McCreary, Paul R. Gray: "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – part 1", IEEE Journal of Solid-State circuits, December 1975.

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 7, JULY 2005

A Cost-Efficient High-Speed 12-bit Pipeline ADC in 0.18-μm Digital CMOS

Terje Nortvedt Andersen, Bjørnar Hernes, *Member, IEEE*, Atle Briskemyr, Frode Telstø, Johnny Bjørnsen, *Member, IEEE*, Thomas E. Bonnerud, and Øystein Moldsvor

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Next Tuesday (10/3-08):

Rest of chapter 13.

- Chapter 14 Oversampling Converters

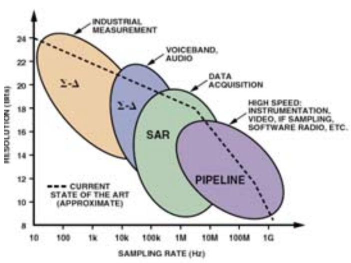


Figure 1. ADC architectures, applications, resolution, and sampling rates.

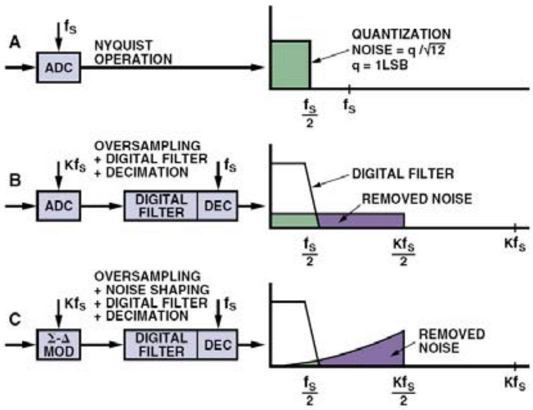
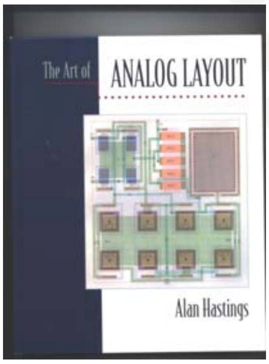


Figure 6. Noise-spectrum effects of the fundamental concepts used in Σ-Δ: oversampling, digital filtering, noise shaping, and decimation.

Analog Layout - mismatch



- *"…The ratio between two similar components on the same integrated circuit can be controlled to better than +/- 1 %, and in many cases, to better than +/- 0.1 %. Devices specifically constructed to obtain a known, constant ratio are called matched devices."*
- "Matching – the Achilles Heel of Analog" (Chris Diorio)

Some companies located in Norway, doing (or that have done) full custom data converter designs:

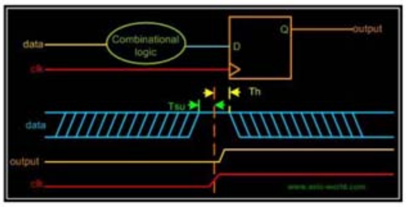
- Analog Concepts (Trondheim)
- Arctic Silicon Devices (Trondheim)
- Atmel Norway (Trondheim)
- Energy Micro (Oslo)
- GE Vingmed Ultrasound (Horten)
- Nordic Semiconductors (Trondheim, Oslo)
- Novelda (Oslo)
- Micrel (Oslo)
- Sintef (Trondheim, Oslo)
- Texas Instruments (Oslo)

NORDIC SEMICONDUCTOR
ATMEL Everywhere You Are
MICREL Innovation Through Technology
ENERGY micro
TEXAS INSTRUMENTS

Metastability in FFs (http://www.asic-world.com/tidbits/metastablity.html) To avoid M. in comparators: Make gain high, increase current levels.

What is metastability?

Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'. This whole process is known as metastability. In the figure below Tsu is the setup time and Th is the hold time. Whenever the input signal D does not meet the Tsu and Th of the given D flip-flop, metastability occurs.



When a flip-flop is in metastable state, its output oscillate between '0' and '1' as shown in the figure below (here the flip-flop output settles down to '0') . How long it takes to settle down, depends on the technology of the flip-flop.

The approximate equation which describes the output voltage, $V_O(t)$ is given by:

$$V_O(t) = \Delta V_{IN} A e^{t/\tau}, \quad \text{Eq. 1}$$

where ΔV_{IN} = the differential input voltage at the time of latching, A = the gain of the preamp at the time of latching, τ = regeneration time constant of the latch, and t = the time that has elapsed after the comparator output is latched (see References 2 and 3).

For small differential input voltages, the output takes longer to reach a valid logic level. If the output data is read when it lies between the "valid logic 1" and the "valid logic 0" region, the data can be in error. If the differential input voltage is exactly zero, and the comparator is perfectly balanced at the time of latching, the time required to reach a valid logic level can be quite long (theoretically infinite). However, comparator hysteresis and input noise makes this condition highly unlikely. The effects of invalid logic levels out of the comparator are different depending upon how the comparator is used in the actual ADC.

From a design standpoint, comparator metastability can be minimized by making the gain (A) high, minimizing the regeneration time constant (τ) by increasing the gain-bandwidth of the latch, and allowing sufficient time (t), for the output of the comparator to settle to a valid logic level. It is not the purpose of this discussion to analyze the complex tradeoffs between speed,

Interpolating ADCs, Folding ADCs and Oversampling Converters

Tuesday 16th of March, 2009, 9:15 – 11:00

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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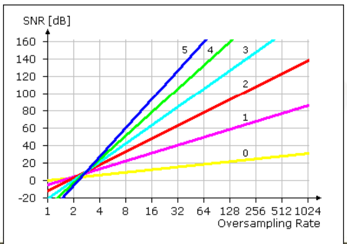
Last time – and today, Tuesday 16th of March:

Last time:
13.1 Integrating Converters
13.2 Successive-Approx. Converters
13.3 Algorithmic (or cyclic) A/D Converters
13.4 Flash (or parallel) converters
13.5 Two-Step A/D converters
13.8 Pipelined A/D Converters
13.9 Time-Interleaved A/D Converters

Today – from the following chapters:
13.6 Interpolating A/D Converters
13.7 Folding A/D Converters
14.1 Oversampled converters



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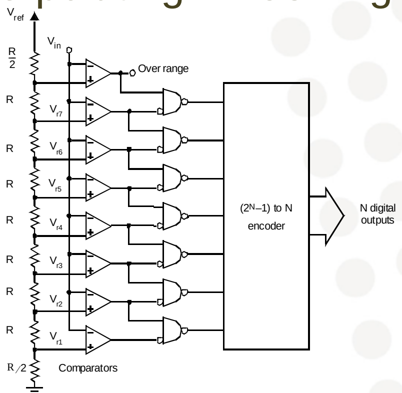
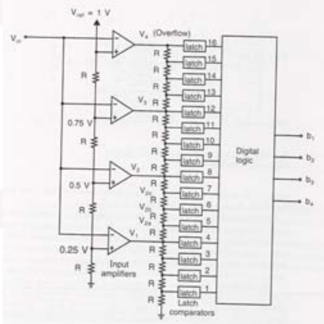
Interpolating ADCs. Rightmost interpol.=4 (1/4)





- Reduced complexity compared to Flash ADCs → reduced input capacitance and slightly reduced power.
- In the mathematical subfield of numerical analysis, **interpolation** is a method of constructing new data points within the range of a discrete set of known data points.

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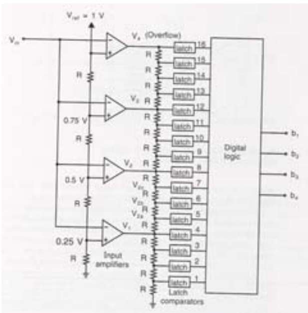
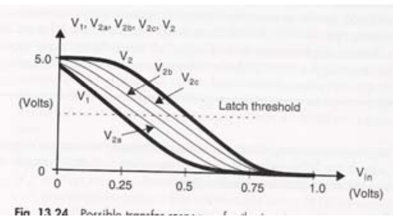
Interpolating ADCs (2/4)





- Uses input amplifiers behaving as linear amplifiers near their threshold voltages, allowed to saturate for moderately large input signals
- Thus ”noncritical” latches need only determine the sign of the amplifier outputs

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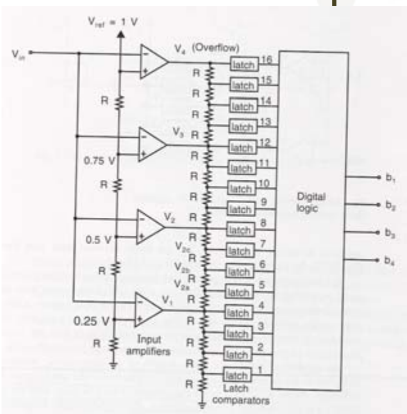
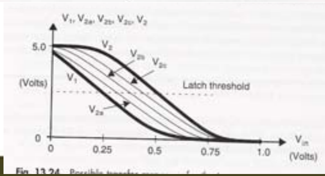
Interpolating ADCs (3/4)





- Amplifier outputs V_1 and V_2 as well as their interpolated values are shown lowermost (fig. 13.24)
- The reference points created from interpolated values (for example V_{2a}, V_{2b}, V_{2c}) have latches potentially triggering in order, for increasing (or decreasing) input.
- For good linearity the interpolated signals need only cross the latch threshold at the correct points

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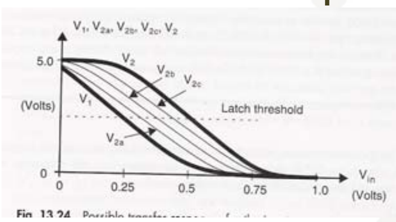
Interpolating ADCs (4/4)



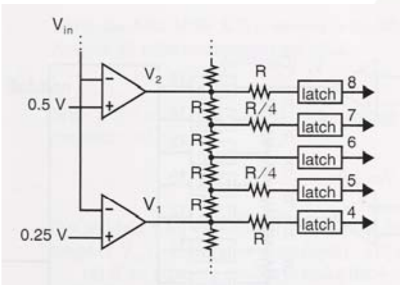


Fig. 13.25 Adding series resistors to equalize delay times to the latch comparators.

- To achieve good linearity V_1 and V_2 need to be linear between their own thresholds. In figure 13.24 this linear region corresponds to $0.25 < V_{in} < 0.5$ (horizontally)
- For fast operation the delays to each of the latches must be made to equal each other as much as possible. In fig. 13.25 this is done using resistors.

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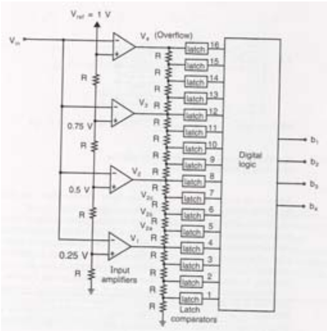
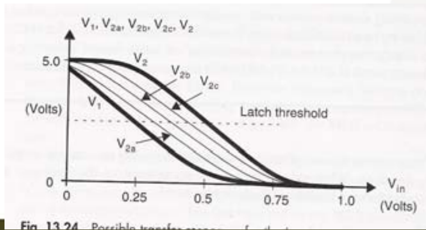
Example, based on Fig. 13.23 (1/2)

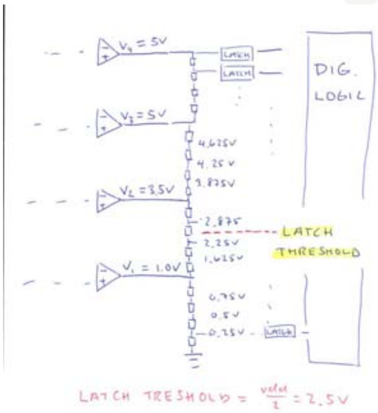


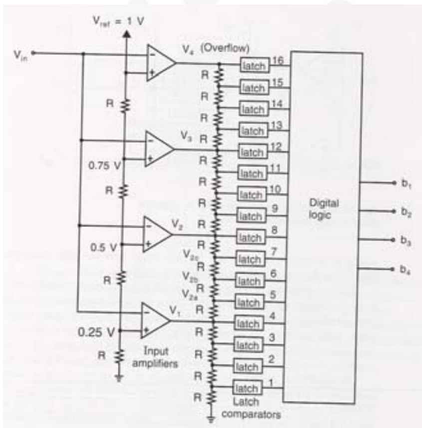


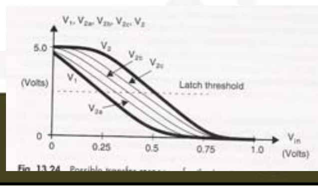
- Vin = 0.4 V, gain of -10, logic levels of 0 and 5 volts. →

- V4 = 5 V
- V3 = 5 V
- V2 = 3.5 V
- V1 = 1.0 V

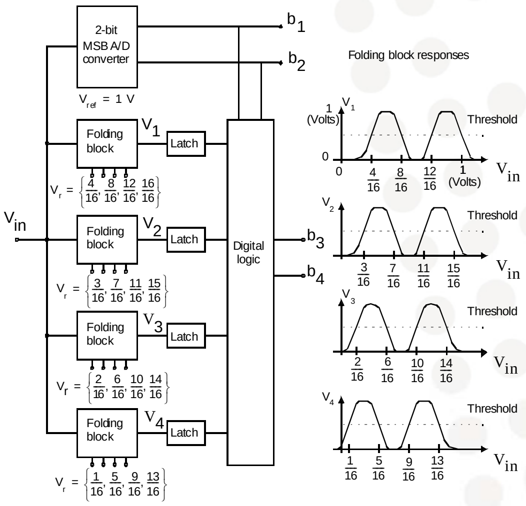
Example – interpolating ADC (2/2)







Folding A/D Converters (13.7)



- The number of latches is reduced compared to the interpolating ADC, and even more from FLASH
- The figure shows a 4 bit converter with folding rate of 4
- A group of LSBs are found separately from a group of MSBs.
- The MSB converter determines whether the input signal, V_{in}, is in one of four voltage regions (between 0 and ¼, ¼ and ½ , ½ and ¾ , or ¾ and 1)
- V_1 to V_4 produce a thermometer code for each of the four MSB regions

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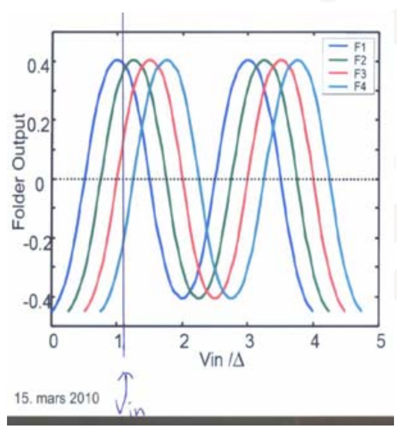
Similar to folding block responses on previous slide..



- Bipolar folder outputs
- Ex: Input 1.05:
- F1 > threshold=0 -> ”1”
- F2 > threshold=0 -> ”1”
- F3 > threshold=0 -> ”1”
- F4 < threshold=0 -> ”0”
- Thermometer code produced for each of the four MSB regions (between 0 and ¼, ¼ and ½ , ½ and ¾ , or ¾ and 1 for previous slide)
- (in certain respects related to interpolation in Fig 13.24)

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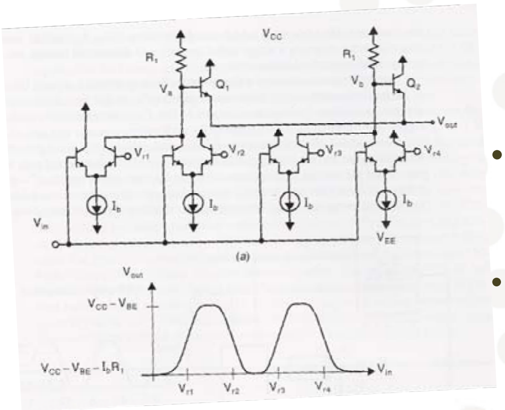
Folding block with a folding rate of four



- Input-output response for the cross-coupled differential pair is shown lowermost
- Vout is low if, and only if, both V_a and V_b are low, otherwise high
- The output from a folding block is at a much higher frequency than the input signal, limiting the practical folding rate.
- Differential solutions in practice

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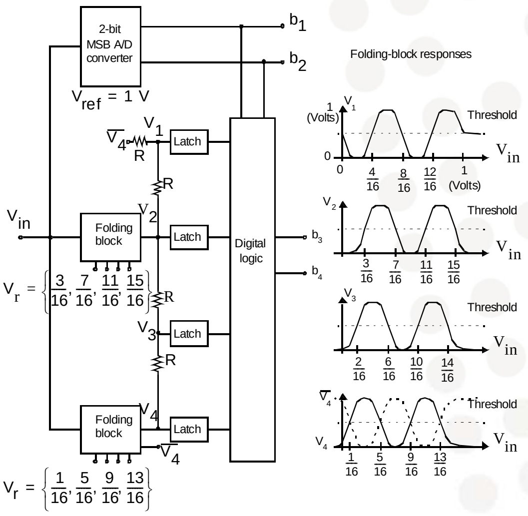
Folding and Interpolating ADC



- By introducing interpolation, the number of folding blocks is reduced
- Input capacitance is reduced (if both folding and interpolating is combined)
- Folding-rate of four and interpolate-by-two
- (Literature references on page 523)

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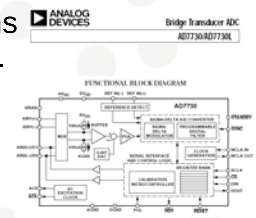
Interpolating and folding and interpolating ADCs

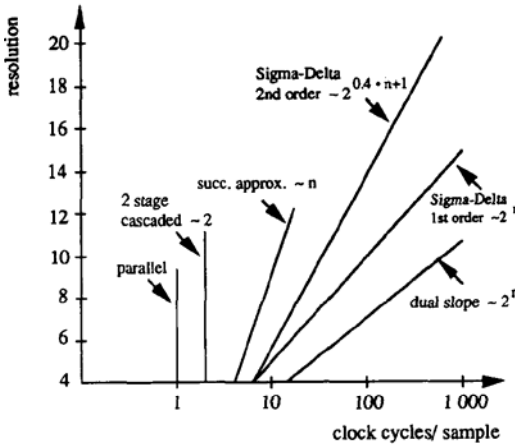
Resolution	Sampling rate	ENOB	Power dissip.	Supply voltage	architecture	reference
8 bit	100 MHz	6.5 bit@5V, 7.1 bit@8V	1.2W@5V	5 or 8 V	interpolating	Steyaert , Roovers, Craninckx, CICC 1993
5 bit	5 GHz	4 bit at 5GHz	113 mW@1V	1 V	interpolating	Wang, Liu, VLSI-DAT '2007
6 bit	200 MHz	5.35 bit	35 mW@3.3V	3.3V	folding and interpolating	Yin, Wang, Liu, ICSICT, 2008
6 bit	200 MHz	5.5 bit	78.8 mW@2.5V	2.5V	folding and interpolating	Silva, Fernandes, ISCAS, 2003

Oversampling converters (chapter 14 in "J & M")

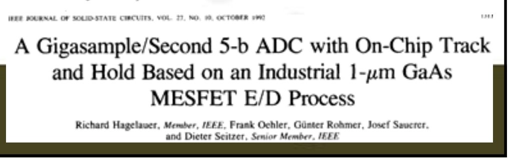
- For high resolution, low-to-medium-speed applications like for example digital audio
- Relaxes requirements placed on analog circuitry, including matching tolerances and amplifier gains
- Simplify requirements placed on the analog anti-aliasing filters for A/D converters and smoothing filters for D/A converters.
- Sample-and-Hold is usually not required on the input
- Extra bits of resolution can be extracted from converters that samples much faster than the Nyquist-rate. Extra resolution can be obtained with lower oversampling rates by exploiting noise shaping



Resolution and clock cycles per sample



. Dependence of achievable resolution and required clock cycles per sample for various ADC systems.

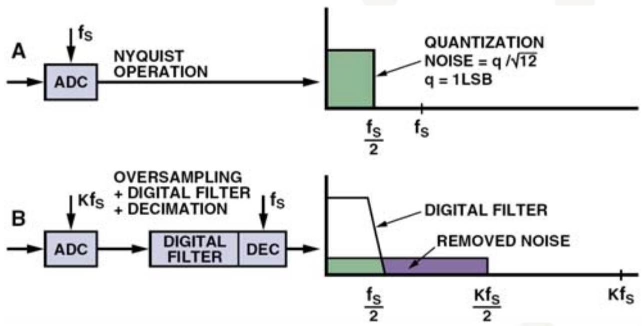


IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 27, NO. 10, OCTOBER 1992

A Gigasample/Second 5-b ADC with On-Chip Track and Hold Based on an Industrial 1-μm GaAs MESFET E/D Process

Richard Hagelauer, *Member, IEEE*, Frank Oehler, Günter Rohmer, Josef Sauerer, and Dieter Seitzer, *Senior Member, IEEE*

Nyquist Sampling and Oversampling



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

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Oversampled converters; High resolution and relatively low speed

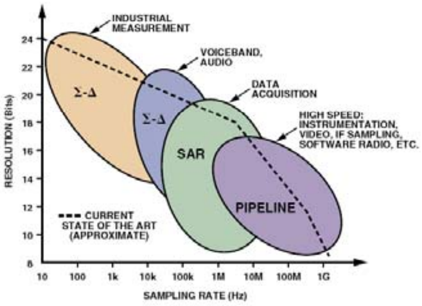

Figure 1. ADC architectures, applications, resolution, and sampling rates.

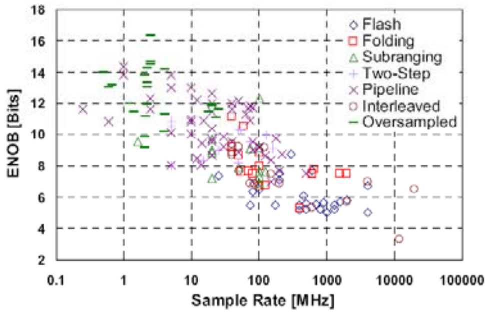

Fig. 2. ADC sample rate vs. ENOB from 1987 to 2005.

Which ADC Architecture Is Right for Your Application?

By Walt Kester [walt.kester@analog.com]

IEEE 2005 CUSTOM INTEGRATED CIRCUITS CONFERENCE

Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS

Y. Chiu [1], B. Nikolić [2], and P. R. Gray [1]

[1] Electrical and Computer Engineering, University of Illinois at Urbana-Champaign
[2] Electrical Engineering and Computer Sciences, University of California at Berkeley

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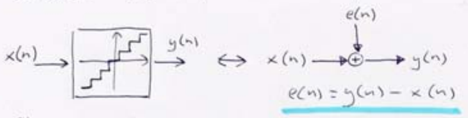
QUANTIZATION NOISE (p. 532–533 in "J & M")

The quantization noise is the difference between the input and output values.



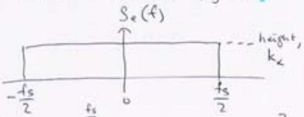
$e(n) = y(n) - x(n)$

This model is exact under the assumption that the quantization error is strongly related to the input signal ("J & M" p. 532). The model becomes approximate when assumptions are made about the statistical properties of $e(n)$, such as $e(n)$ being an independent white-noise signal. This model leads to a simpler understanding of ΣΔ and with some exceptions is usually reasonably accurate.

- If $x(n)$ is very active, $e(n)$ can be approximated as an independent random number uniformly distributed between $\pm\frac{\Delta}{2}$, where Δ equals the difference between two adjacent quantization levels.

Thus, the quantization noise power equals $\frac{\Delta^2}{12}$ (Sec. 11.3) and is independent of the sampling frequency, f_s

The spectral density of $e(n)$, $S_e(f)$ is white (constant over freq.) and all its power within $\pm f_s/2$, as shown in the figure:



$$\int_{-f_s/2}^{f_s/2} S_e^2(f)\,df = \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} k_x^2\,df = (k_x)^2 f_s = \frac{\Delta^2}{12}$$

$$\Updownarrow$$

$$k_x = \frac{\Delta}{\sqrt{12}}\sqrt{\frac{1}{f_s}}$$

The spectral density height is calculated by noting that the total noise power is $\Delta^2/12$ and with a two-sided def. of power equals the area under $S_e(f)$ within $+/- f_s/2$

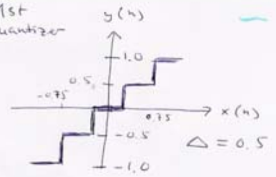
14.1 Output and quantization errors for two quantizers

$x(n) = \{0.01, 0.31, -0.11, 0.80, 0.52, -0.70\}$

Quantizer 1:

$y_1(n) = \{0.0, 0.5, 0, 1.0, 0.5, -0.5\}$

1st quantizer



$\Delta = 0.5$

Quantizer 2:

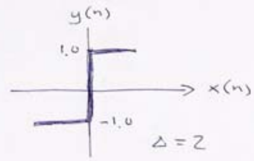
$y_2(n) = \{1.0, 1.0, -1.0, 1.0, 1.0, -1.0\}$

$e(n) = y(n) - x(n)$

$e_1(n) = \{-0.01, 0.19, -0.11, -0.30, -0.02, 0.20\}$

$e_2(n) = \{0.99, 0.69, -0.89, 0.20, 0.48, -0.30\}$

Quantizer II:



$\Delta = 2$

Expected power and power density height?

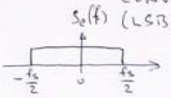
$e(n)$ is approximated as an independent random number uniformly distributed between $\pm\frac{\Delta}{2}$, where Δ equals the difference between two adjacent quantization levels.

$$\boxed{P_e = \frac{\Delta^2}{12}}$$

quant 1: $\frac{\Delta^2}{12}[W] = \frac{(0.5)^2}{12}[W] = 0.0208\bar{3}\ [W]$

quant 2: $\frac{\Delta^2}{12}[W] = \frac{2^2}{12}[W] = 0.3\bar{3}\ [W]$

"OVERSAMPLING IS BASED ON THE ASSUMPTION THAT AN ADC'S TOTAL QUANTIZATION NOISE POWER (VARIANCE) IS THE SQUARED VALUE OF THE CONVERTER'S LEAST SIGNIFICANT BIT (LSB) VOLTAGE DIVIDED BY 12" [LYONS'05]



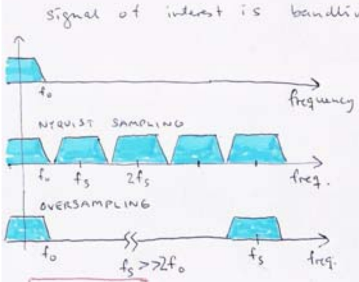
$S_{e_I}^2(f) = \frac{0.0208\bar{3}}{2\pi}\left[\frac{W}{rad/sample}\right] = 0.00331 \frac{W}{rad/sample}$

$S_{e_{II}}^2(f) = \frac{0.333}{2\pi}\left[\frac{W}{rad/sample}\right] = 0.053 \frac{W}{rad/sample}$

OVERSAMPLING ADVANTAGE p. 535

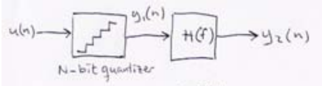
PEAK

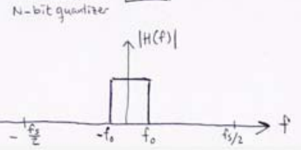
Signal of interest is bandlimited to f_o



$$\boxed{OSR \equiv \frac{f_s}{2f_o}}$$

After quantization, $y_1(n)$ is filtered by $H(f)$ to create $y_2(n)$ that eliminates quantization noise (together with any other signals) greater than f_o.





If the input is sinusoidal, its maximum peak value without clipping is $2^N(\Delta/2)$

For this wave the signal power, P_s, has a power equal to $P_s = \left(\frac{\Delta 2^N}{2}\frac{1}{\sqrt{2}}\right)^2 = \frac{\Delta^2 2^{2N}}{8}$

The power of the input signal within $y_2(n)$ remains the same as before since we assumed the signal's frequency content is below f_o.

HOWEVER, THE QUANTIZATION NOISE POWER IS REDUCED TO

$$P_e = \int_{-f_s/2}^{f_s/2} S_e^2(f)\,|H(f)|^2\,df = \int_{-f_o}^{f_o} k_x^2\,df$$

$$= \frac{2f_o}{f_s}\cdot\frac{\Delta^2}{12} = \frac{\Delta^2}{12}\left[\frac{1}{OSR}\right]$$

THEREFORE, DOUBLING OSR DECREASES THE QUANTIZATION NOISE POWER BY ONE-HALF, OR EQUIVALENTLY, 3 dB (or equiv. 0.5 bits)

$$SNR_{MAX} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR)$$

$$= \underbrace{6.02N + 1.76}_{\text{due to N-bit quantizer}} + \underbrace{10\log(OSR)}_{\text{due to oversampling}}\ [dB]$$

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) \quad \wedge \quad P_s = \frac{\Delta^2 2^{2N}}{8} \quad \wedge \quad P_e = \frac{\Delta^2}{12}\frac{1}{OSR}$$

$$\Downarrow$$

$$SNR_{max} = 10 \log\left[\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}\cdot\frac{1}{OSR}}\right] = 10 \log\left[\frac{\frac{\Delta^2 \cdot 2^{2N}}{2\cdot 2\cdot 2}}{\frac{\Delta^2}{2\cdot 2\cdot 3}\frac{1}{OSR}}\right] = 10 \log \frac{3}{2} 2^{2N} \cdot OSR$$

$$= 10 \log \frac{3}{2}\cdot 2^{2N} + 10 \log OSR$$

$$= 10 \log \frac{3}{2} + 10 \log 2^{2N} + 10 \log OSR$$

$$= 10 \log 2^{2N} + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2N \cdot \log 2 + 1.76 + 10 \log OSR$$

$$= 10 \cdot 2 \cdot N \cdot 0.301 + 1.76 + 10 \log OSR$$

$$= 6.02N + 1.76 + 10 \log(OSR) \quad [dB]$$

$\boxed{\log_b(c^p) = p\log_b(c) \qquad \log(xy) = \log x + \log y}$

(14.13) pp. 536 i J&M.

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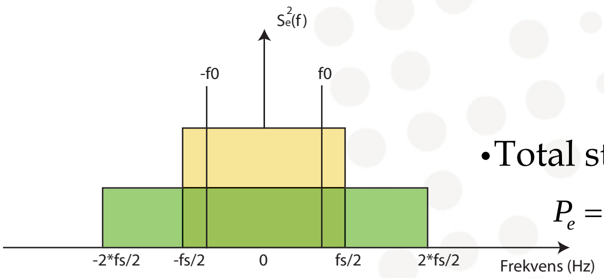
Oversampling (without noise shaping)



- Total støy er gitt av:

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\,df = \frac{\Delta^2}{12}\cdot\frac{1}{OSR}$$

- Doubling of the sampling frequency increases the dynamic range by 3 dB = 0.5 bit.
- To get a high SNR a very high fs is needed → high power consumption.
- Oversampling usually combined with noise shaping and higher order modulators, for higher increase in dynamic range per octave ("OSR")

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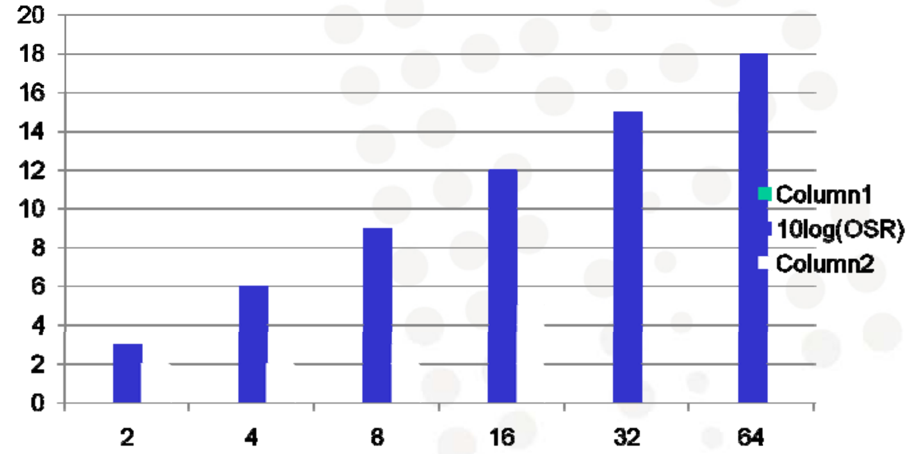
SNRmax = 6.02N+1.76+10log(OSR) [dB]

SNR improvement 0.5 bits / octave



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Ex. 14.3

EXAMPLE 14.3

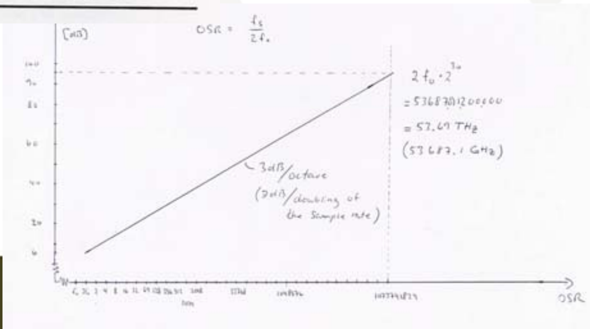
Given that a 1-bit A/D converter has a 6-dB SNR, what sample rate is required using oversampling (no noise shaping) to obtain a 96-dB SNR (i.e., 16 bits) if $f_0 = 25$ kHz ? (Note that the input into the A/D converter has to be very active for the white-noise quantization model to be valid—a difficult arrangement when using a 1-bit quantizer with oversampling without noise shaping).

Solution

Oversampling (without noise shaping) gives 3 dB/octave where 1 octave implies doubling the sampling rate. We require 90 dB divided by 3 dB/octave, or 30 octaves. Thus, the required sampling rate, f_s, is

$$f_s = 2^{30} \times 2f_0 \cong 54{,}000 \text{ GHz !}$$

This example shows why noise shaping is needed to improve the SNR faster than 3 dB/octave, since 54,000 GHz is highly impractical.



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Advantages of 1-bit A/D converters (p.537 in "J&M")

- Oversampling improves signal-to-noise ratio, but not linearity
- Ex.: 12-bit converter with oversampling needs component accuracy to match better than 16-bit accuracy if a 16-bit linear converter is desired

- Advantage of 1-bit D/A is that it is inherently linear. Two points define a straight line, so no laser trimming or calibration is required
- Many audio converters presently use 1-bit converters for realizing 16- to 18-bit linear converters (with noise shaping).

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Problems with some 1-bit converters ((?))

Why 1-Bit Sigma-Delta Conversion is Unsuitable for High-Quality Applications

by

Stanley P. Lipshitz and John Vanderkooy
Audio Research Group, University of Waterloo
Waterloo, Ontario N2L 3G1, Canada

ABSTRACT
Single-stage, 1-bit sigma-delta converters are in principle imperfectible. We prove this fact. The reason, simply stated, is that, when properly dithered, they are in constant overload. Prevention of overload allows only partial dithering to be performed. The consequence is that distortion, limit cycles, instability, and noise modulation can never be totally avoided. We demonstrate these effects, and using coherent averaging techniques, are able to display the consequent profusion of nonlinear artefacts which are usually hidden in the noise floor. Recording, editing, storage, or conversion systems using single-stage, 1-bit sigma-delta modulators, are thus inimical to audio of the highest quality. In contrast, multi-bit sigma-delta converters, which output linear PCM code, are in principle infinitely perfectible. (Here, multi-bit refers to at least two bits in the converter.) They can be properly dithered so as to guarantee the absence of all distortion, limit cycles, and noise modulation. The audio industry is misguided if it adopts 1-bit sigma-delta conversion as the basis for any high-quality processing, archiving, or distribution format to replace multi-bit, linear PCM.

Audio Engineering Society
Convention Paper 5395
Presented at the 110th Convention
2001 May 12–15 Amsterdam, The Netherlands

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Oversampling with noise shaping (14.2)

- Oversampling combined with noise shaping can give much more dramatic improvement in dynamic range each time the sampling frequency is doubled.
- The sigma delta modulator converts the analog signal into a noise-shaped low-resolution digital signal.
- The decimator converts to a high resolution digital signal

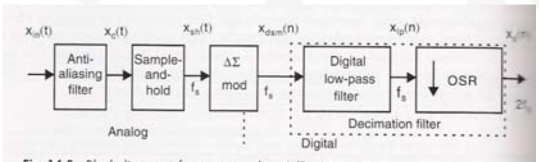
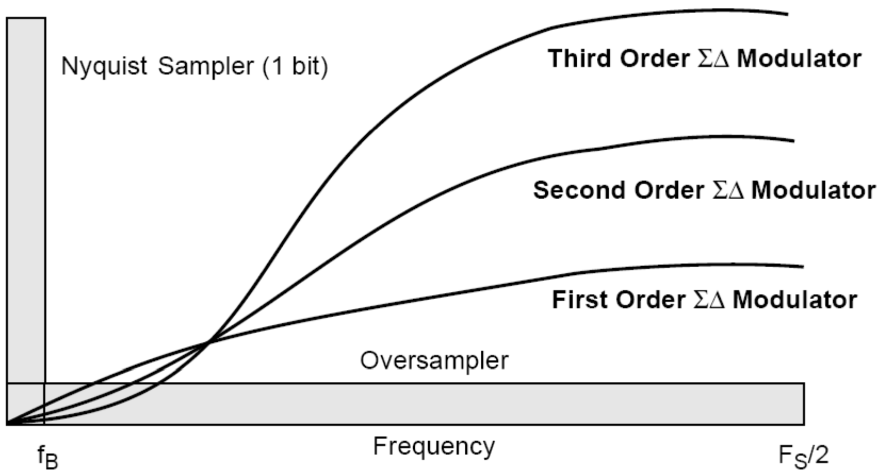


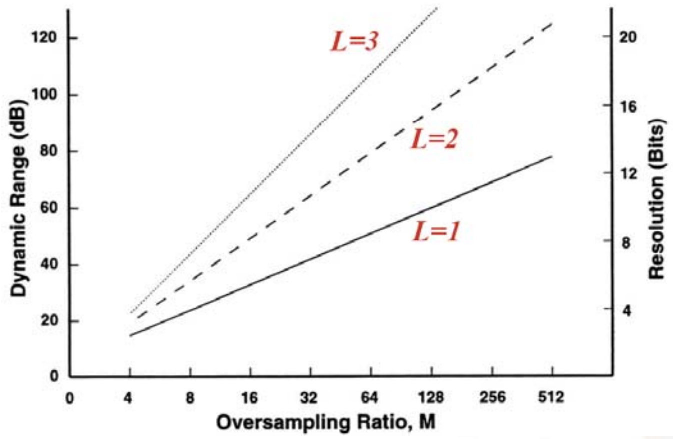
Fig. 14.5 Block diagram of an oversampling A/D converter.

Multi-order sigma delta noise shapers (Sangil Park, Motorola)



Note: Higher order Noise Shaper has less baseband noise

OSR, modulator order and Dynamic Range



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order

Oversampling and noise shaping

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Ex. 14.5

- Given that a 1-bit A/D converter has a 6 dB SNR, which sample rate is required to obtain a 96-dB SNR (or 16 bits) if f_0 = 25 kHz for straight oversampling as well as first-and second-order noise shaping?
- Oversampling with no noise shaping: From ex. 14.3 we know that straight oversampling requires a sampling rate of 54 THz.
- (6.02N+1.76+10 log (OSR) = 96 <-> 6 + 10 log OSR = 96) <-> 10 log OSR = 90

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Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 5.17 + 30\log(OSR) \quad (14.26)$$

We see here that doubling the OSR gives an SNR improvement for a first-order modulator of 9 dB or, equivalently, a gain of 1.5 bits/octave. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

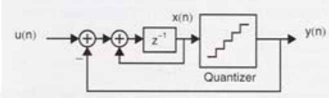

Fig. 14.7 A first-order noise-shaped interpolative modulator.

- Oversampling with 1st order noise shaping:
- 6 - 5.17 + 30 log(OSR) = 96 OSR = f_s / 2f_0
- 30log (OSR) = 96 – 6 + 5.17 = 95.17

  A doubling of the OSR gives an SNR improvement of 9 dB / octave for a 1st order modulator;

  95.17 / 9 = 10.57 $2^{10.56}$ x 2*25 kHz = 75.48 MHz

OR: log(OSR)=95.17/30 = 3.17 → OSR = 1509.6

1509.6 * (2*25kHz) = 75.48 MHz

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Ex. 14.5

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50\log(OSR) \quad (14.3$$

We see here that doubling the OSR improves the SNR for a second-order modulator by 15 dB or, equivalently, a gain of 2.5 bits/octave.
The realization of the second-order modulator using switched-capacitor techniques is straightforward and is left as an exercise for the interested reader.

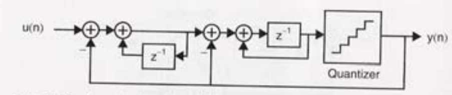

Fig. 14.10 Second-order ΔΣ modulator.

- Oversampling with 2nd order noise shaping:
- 6 – 12.9 + 50 log(OSR) = 96 OSR = fs / 2f_0
- 50 log (OSR) = 96 – 6 + 12.9 = 102.9

  A doubling of the OSR gives an SNR improvement of 15 dB / octave for a 2nd order modulator;

  102.9 / 15 = 6.86 $2^{6.86}$ x 2*25 kHz = 5.81 MHz

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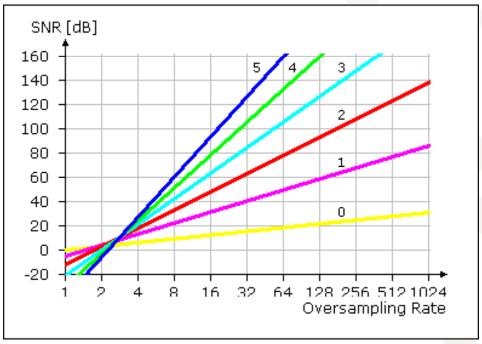
Ex. 14.5 ”point”:



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- 6 db Quantizer, for 96 dB SNR:
- Plain oversampling: f_s=54 GHz
- 1st order : f_s=75.48 MHz
- 2nd order: f_s= 5.81 MHz

- Exam problem (INF4420) below

3 a) (Weight 10 %)

A sampled signal is bandlimited to f_0 = 22 kHz.What is the sampling frequency, f_s, for an oversampling ratio (“OSR”) of 128?
A 1-bit analog-to-digital converter (“ADC”) has an inherent 6-dB SNR. Which maximum SNR is acquired by combining it with strict oversampling and an OSR of 128, if no noise shaping is used?
What is the maximum SNR in the similar case exploiting 2nd order noise shaping?
If a 1-bit ADC using 3rd order noise shaping has a maximum SNR of 125 dB for an OSR of 128, what is the expected maximum SNR if the OSR is reduced to 32?

16. mars 2010

Sigma Delta converters,ISSCC 2008

- ISSCC- Foremost global forum
- ”CT”: continous time

ΔΣ DATA CONVERTERS
Chair: Zhongyuan Chang, IDT Technology, Shanghai, China
Associate Chair: Yiannos Manoli, University of Freiburg, Freiburg, Germany

27.1 A 108dB-SNR 1.1mW Oversampling DAC with a Three-Level DEM Technique **8:30 AM**

K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, P. Baginski
Analog Devices, Wilmington, MA

A multi-bit audio DAC in a 0.18μm CMOS process uses a three-level DEM scheme and an ISI-free output stage to achieve 108dB SNR while consuming a total of 1.1mW per channel from a 1.8V supply.

27.2 A 0.7V 36μW 85dB-DR Audio ΔΣ Modulator Using a Class-C Inverter **9:00 AM**

Y. Chae, I. Lee, G. Han
Yonsei University, Seoul, Korea

An audio ΔΣ modulator is realized in a standard 0.18μm CMOS process, exploiting the possibility of substituting a class-C inverter for an OTA. The measurement results from the fabricated chip demonstrate 81dB SNDR, 84dB SNR, and 85dB DR for a 20kHz signal bandwidth. The chip consumes 36μW from a 0.7V supply.

27.3 An Inverter-Based Hybrid ΔΣ Modulator **9:30 AM**

R. Veldhoven, R. Rutten, L. Breems
NXP Semiconductors, Eindhoven, Netherlands

A hybrid ΔΣ modulator with 1st-order analog filter, 5b quantizer, 2nd-order digital filter, 1b quantizer, and 1b DAC is presented. The active circuitry is implemented solely with inverter circuits and standard digital cells. The 65nm CMOS modulator achieves a peak SNR of 77dB in 200kHz. Power consumption is 950μW at 1.2V and the area is 0.03mm².

Break 10:00 AM

27.4 A Noise-Coupled Time-Interleaved ΔΣ ADC with 4.2MHz BW, -98dB THD, and 79dB SNDR **10:15 AM**

K. Lee[1], J. Chae[1], M. Aniya[2], K. Hamashita[2], K. Takasuka[2], S. Takeuchi[2], G. Temes[1]
[1]Oregon State University, Corvallis, OR
[2]Asahi Kasei, Atsugi, Japan

A two-channel time-interleaved noise-coupled ΔΣ ADC is realized in 0.18μm CMOS technology. Time interleaving doubles the effective clock rate while noise coupling raises the effective order of the noise-shaping loops, implements dithering, and also prevents tone generation in all loops. Using a 1.5V supply, the device achieved SFDR>100dB, THD = -98dB, and an SNDR of 79dB in a 4.2MHz signal band.

27.5 A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMax Receivers **10:45 AM**

P. Malla[1,2], H. Lakdawala[1], K. Kornegay[3], K. Soumyanath[1]
[1]Intel, Hillsboro, OR
[2]Cornell University, Ithaca, NY
[3]Georgia Institute of Technology, Atlanta, GA

A reconfigurable MASH 2-2 ΔΣ ADC, fabricated in 90nm CMOS, has an OSR of 10.5 and uses a 1.2V supply. It achieves SNRs of 72, 62, 60, and 54dB with a 20MHz BW while consuming 28, 20, 15, and 12mW, respectively. The configuration and, therefore, power are determined by signal and blocker power. SNRs of 73, 77, and 78dB are achieved for BWs of 10, 5, 2.5MHz, respectively.

27.6 A 100mW 10MHz-BW CT ΔΣ Modulator with 87dB DR and -91dBc IMD **11:15 AM**

W. Yang, W. Schofield, H. Shibata, S. Korrapati, A. Shaikh, N. Abaskharoun, D. Ribner
Analog Devices, Wilmington, MA

A 5th-order CT ΔΣ modulator with a hybrid feedback-feedforward topology and 9-level quantization is implemented in a 0.18μm CMOS process. When clocked at 640MHz, the modulator achieves 87dB DR, 82dB peak SNDR, and -91dBc IMD over a 10MHz BW. The modulator occupies 0.7mm² and consumes 100mW from a 1.8V supply.

27.7 A 65nm CMOS CT ΔΣ Modulator with 81dB DR and 8MHz BW Auto-Tuned by Pulse Injection **11:45 AM**

Y-S. Shu[1], B-S. Song[1], K. Bacrania[2]
[1]University of California, San Diego, CA
[2]Conexant Systems, Palm Bay, FL

Active filters for CT ΔΣ modulators are calibrated by injecting a binary pulse dither and nulling it with an LMS algorithm. A 3rd-order 4b prototype in 65nm CMOS occupies 0.5mm² and consumes 50mW at 1.3V. At 256MS/s (OSR=16), the DR is 81dB with a 2.4V_{pp} full-scale range. SNR and SNDR at -1dBFS are 76 and 70dB, respectively.

27.8 A CT ΔΣ ADC for Voice Coding with 92dB DR in 45nm CMOS **12:00 PM**

L. Doerrer, F. Kuttner, A. Santner, C. Kropf, T. Puaschitz, T. Hartig
Infineon, Villach, Austria

A 2nd-order CT multi-bit (4b) ΔΣ ADC for voice coding is implemented in a 45nm CMOS process. The input operational amplifier is chopped to eliminate flicker noise and offset. The quantizer, a power-efficient 3-comparator tracking ADC with a capacitive voltage reference DAC, is suitable for low-voltage designs and high clock rates. Over a bandwidth of 20kHz, the DR is 86dB. The ADC consumes 1.2mW from a 1.1V supply when clocked at 12MHz.

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The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency and to network with leading experts.

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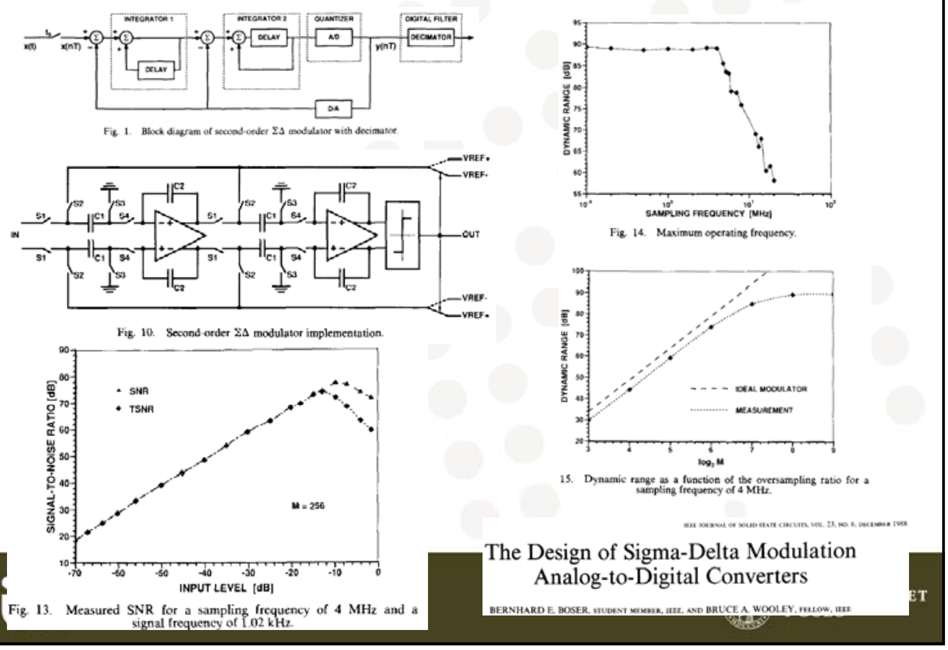
2nd order sigma delta modulator



Additional litterature

- Stanley P. Lipshitz, John Vanderkooy: Why 1-bit Sigma Delta Conversion is Unsuitable for High Quality Applications , Journal of the audio engineering society, 2001.
- Y. Chiu, B. Nicolic, P. R. Gray: Scaling of Analog-to-Digital Converters into Ultra-Deep-Submicron CMOS, Proceedings of Custom Integrated Circuits Conference, 2005.
- Richard Hagelauer, Frank Oehler, Gunther Rohmer, Josef Sauerer, Dieter Seitzer: A GigaSample/Second 5-b ADC with On-Chip Track-And-Hold Based on an Industrial 1 um GaAs MESFET E/D Process, IEEE Journal of Solid-State Circuits ("JSSC"), October 1992.
- Walt Kester: Which ADC Architecture is right for your application?, Analog Dialogue, Analog Devices, 2005.
- Richard Lyons, Randy Yates: "Reducing ADC Quantization Noise", MicroWaves & RF, 2005
- Sangil Park: "Principles of sigma-delta modulators for analog to digital converters", Motorola
- B. E. Boser, B. A. Wooley: "The design of sigma delta modulation analog to digital converters, IEEE JSSC, 1988.
- John P. Bentley: Principles of Measurement Systems, 2nd ed., Bentley, 1989.
- Lecture Notes, University of California, Berkeley,

  EE247 Analog Digital Interface Integrated Circuits, Fall 07;http://inst.eecs.berkeley.edu/~ee247/fa07/

Next Time, 23/3-10:

- More from Chapter 14; Oversampling Converters (14.2, 14.3, 14.4, 14.5, 14.7)
- Beginning of chapter 16; Phase-Locked Loops (16.1)

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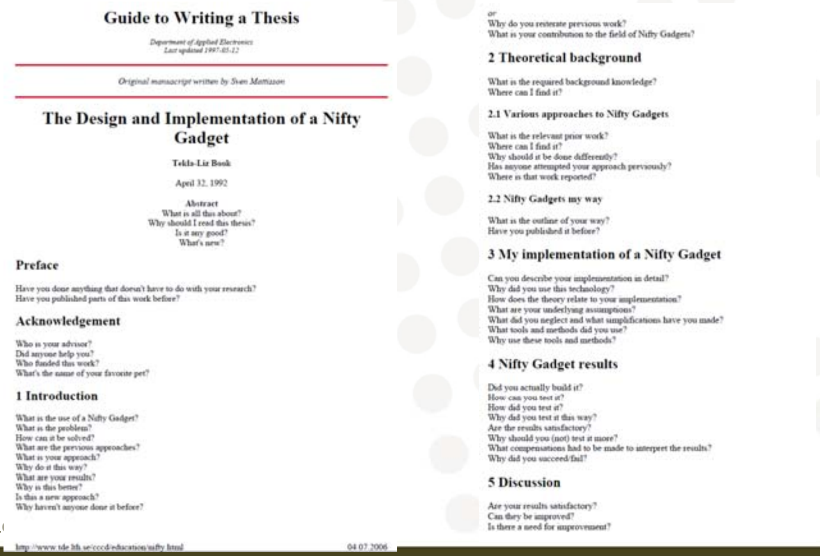
Guide to writing a thesis / report: The Design and implementation of a Nifty Gadget (page 1 and 2)



Guide to Writing a Thesis

Department of Applied Electronics
Last updated 1997-05-12

Original manuscript written by Sven Mattisson

The Design and Implementation of a Nifty Gadget

Tekla-Liz Book

April 32, 1992

Abstract
What is all this about?
Why should I read this thesis?
Is it any good?
What's new?

Preface

Have you done anything that doesn't have to do with your research?
Have you published parts of this work before?

Acknowledgement

Who is your advisor?
Did anyone help you?
Who funded this work?
What's the name of your favorite pet?

1 Introduction

What is the use of a Nifty Gadget?
What is the problem?
How can it be solved?
What are the previous approaches?
What is your approach?
Why do it this way?
What are your results?
Why is this better?
Is this a new approach?
Why haven't anyone done it before?

http://www.tde.lth.se/cccd/education/nifty.html 04.07.2006

or
Why do you reiterate previous work?
What is your contribution to the field of Nifty Gadgets?

2 Theoretical background

What is the required background knowledge?
Where can I find it?

2.1 Various approaches to Nifty Gadgets

What is the relevant prior work?
Where can I find it?
Why should it be done differently?
Has anyone attempted your approach previously?
Where is that work reported?

2.2 Nifty Gadgets my way

What is the outline of your way?
Have you published it before?

3 My implementation of a Nifty Gadget

Can you describe your implementation in detail?
Why did you use this technology?
How does the theory relate to your implementation?
What are your underlying assumptions?
What did you neglect and what simplifications have you made?
What tools and methods did you use?
Why use these tools and methods?

4 Nifty Gadget results

Did you actually build it?
How can you test it?
How did you test it?
Why did you test it this way?
Are the results satisfactory?
Why should you (not) test it more?
What compensations had to be made to interpret the results?
Why did you succeed/fail?

5 Discussion

Are your results satisfactory?
Can they be improved?
Is there a need for improvement?

38

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”Nifty Gadget” page 3 and 4

Are other approaches worth trying out?
Will some restriction be lifted?
Will you save the world with your Nifty Gadget?

6 References

What is the background reading list?
Where is the related work?
Where is the prior work?
Where can I find important material?

Appendix A

Can you outline fatilary calculus or whatever complicated theory or results you are using that will obscure the text?

Appendix B

A thesis should discuss the following topics:

- **Introduction**

  Presentation of the problem or phenomenon to be addressed, the situation where the problem or phenomenon occurs, and references to earlier relevant research.

  Common errors
  Problem is not properly specified or formulated; insufficient references to earlier work.

- **Purpose**

  What can be gained by more knowledge about the problem or phenomenon.

  Common errors
  The purpose is not mentioned, not connected to earlier research, or not in line with what the actual contents of the thesis.

- **Problem/Hypothesis**

  Questions that need to be answered to reach the goal and/or hypothesis formulated be means of underlying theories.

  Common errors
  Missing problem description; deficiencies in the connections between questions; badly formulated hypothesis.

- **Method**

  Choice of an adequate method with respect to the purpose and problem/hypothesis.

  Common errors
  An inappropriate method is used, for example due to lack of knowledge about different methods; erroneous use of chosen method.

- **Result**

  Answers to the forwarded questions by means of the achieved results.

  Common errors
  The results are not properly connected to the problem; blurry presentation; the results are inter-mixed with discussion.

- **Discussion**

  Discussion of the accuracy and relevance of the results; comparison with other researchers results.

  Common errors
  Too far reaching conclusions; guesswork not supported by the data; introduction of a new problem and a discussion around this.

- **Conclusion**

  Consequences of the achieved results, for example for new research, theory and applications.

  Common errors
  The conclusions are too far reaching with respect to the achieved results; the conclusions do not correspond with the purpose.

Home Page for the Department of Applied Electronics

Oversampling Converters and PLLs

Tuesday 23rd of March, 2010, 9:15 – 11:10

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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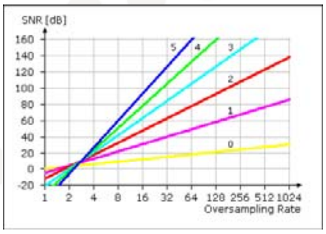
Last time – and today, Tuesday 16th of March:

Last time:

13.6 Interpolating A/D Converters
13.7 Folding A/D Converters
14.1 Oversampled converters

Today:

14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
 2nd order sigma delta design example
16.1 Basic Phase Locked Loop Architecture



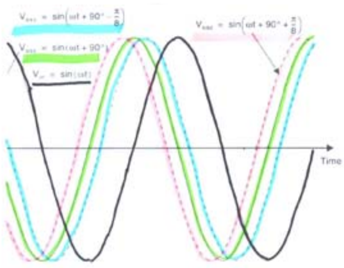


Fig. 16.3

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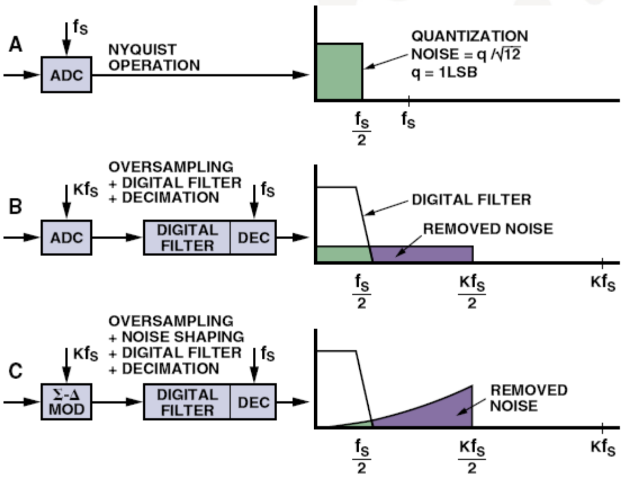
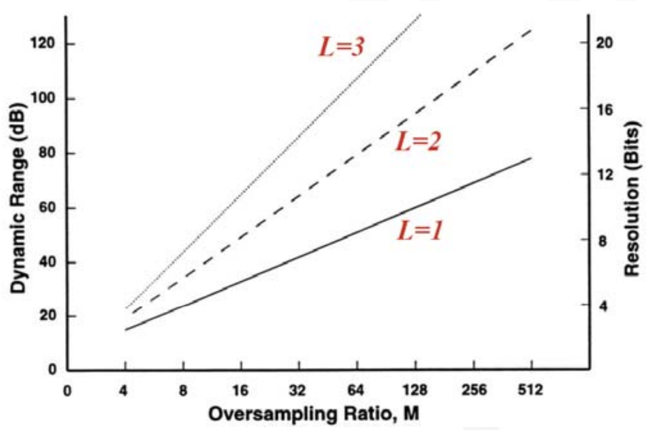
Nyquist Sampling, Oversampling, Noise Shaping



- Figure from [Kest05]
- Straight over-sampling gives an SNR improvement of 3 dB / octave
- fs > $2f_0$ ($2f_0$ = Nyquist Rate
- OSR = $f_s/2f_0$
- SNRmax = 6.02N+1.76+ 10log (OSR)

OSR, modulator order and Dynamic Range



- 2 X increase in M → (6L+3)dB or (L+0.5) bit increase in DR.
- L: sigma-delta order
- Oversampling and noise shaping

14.2 Oversampling with noise shaping

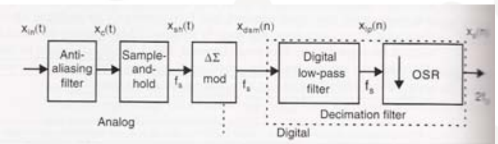


Fig. 14.5 Block diagram of an oversampling A/D converter.

- The anti aliasing filter bandlimits the input signals less than $f_s/2$.
- The continous time signal $x_c(t)$ is sampled by a S/H (not necessary with separate S/H in Switched Capacitor impl.)
- The Delta Sigma modulator converts the analog signal to a noise shaped low resolution digital signal
- The decimator converts the oversampled low resolution digital signal into a high resolution digital signal at a lower sampling rate usually equal to twice the desired bandwidth of the desired input signal (conceptually a low-pass filter followed by a downsampler).

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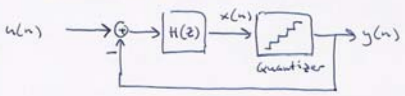
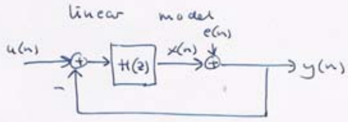
Noise shaped Delta Sigma Modulator

General ΔΣ modulator

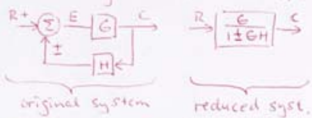


linear model

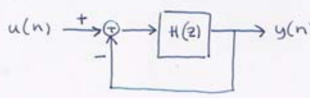


The linear model can be treated as having two independent inputs (which is an approximation).

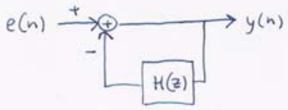
BLOCK DIAGRAM ALGEBRA, Cathey & Nasar p. 292; eliminating a feedback loop:



Signal:



Noise:



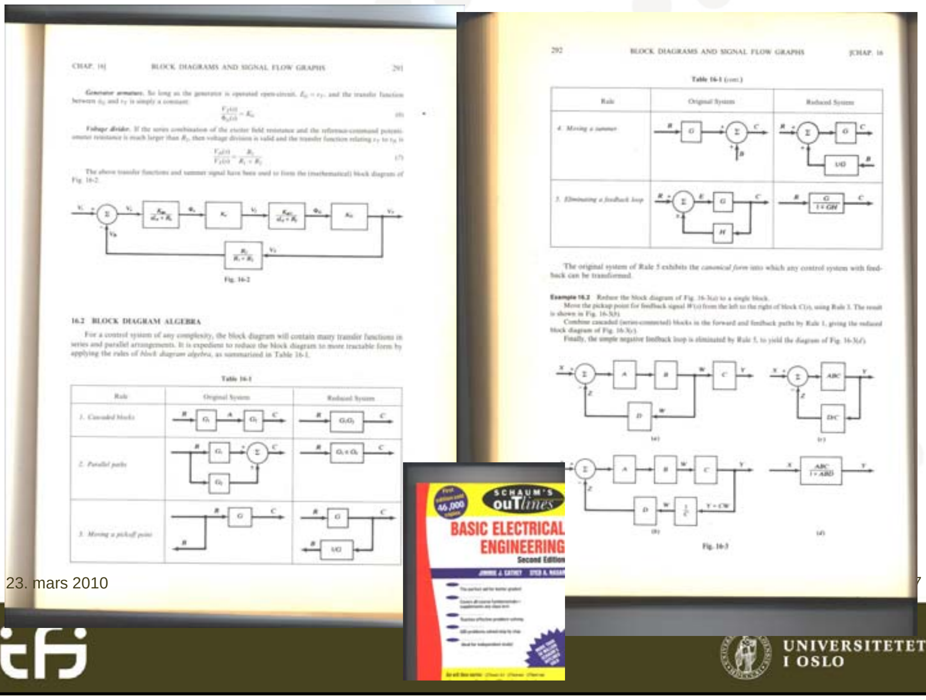
Signal transfer function, $S_{TF}(z)$:

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}$$

Noise transfer function, $N_{TF}(z)$:

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$$

The output is the combination of the input and noise: $Y(z) = S_{TF}(z)U(z) + N_{TF}(z)E(z)$



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First-Order Noise Shaping (Figures from Schreier & Temes '05)

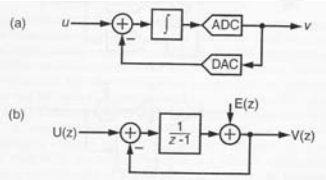

Figure 1.4: (a) A delta-sigma modulator used as an ADC and (b) its linear z-domain model.

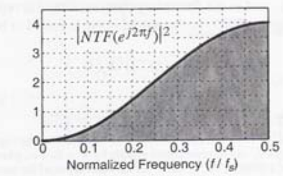

Figure 1.5: Noise-shaping function for the ΔΣ modulator shown in Fig. 1.4.

- $S_{TF}(z) = [H(z)/1+H(z)]$ (eq. 14.15) $N_{TF}(z) = [1/1+H(z)]$
- $Y(z) = S_{TF}(z)\, U(z) + N_{TF}(z)\, E(z)$
- $H(z) = 1/z-1$ (discrete time integrator) gives 1st order noise shaping
- $S_{TF}(z) = [H(z)/1+H(z)] = 1/(z-1)/[1+1/(z-1)] = z^{-1}$
- $N_{TF}(z) = [1/1+H(z)] = 1/[1+1/(z-1)] = (1 - z^{-1})$
- The signal transfer function is simply a delay, while the noise transfer function is a discrete-time differentiator (i.e. a high-pass filter)

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14.2 Oversampling with noise shaping

$$N_{TF}(f) = 1 - e^{-j2\pi f/f_s} = \left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right)\cdot e^{-j\pi f/f_s} = \frac{\left(e^{j\pi f/f_s} - e^{-j\pi f/f_s}\right)\cdot 2j\cdot e^{-j\pi f/f_s}}{2j}$$

$$= \sin\left(\frac{\pi f}{f_s}\right)\cdot 2j\cdot e^{-j\pi f/f_s}$$

$$\boxed{\cos z = \frac{e^{jz}+e^{-jz}}{2} \qquad \sin z = \frac{e^{jz}-e^{-jz}}{2j}}$$

$$|N_{TF}(f)| = 2\sin\left(\frac{\pi f}{f_s}\right) \quad \text{("high-pass")}$$

Quantization noise power over the frequency band 0 to f_0 is now given by

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\cdot|N_{TF}|^2\,df = \int_{-f_0}^{f_0}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \qquad (14.23)$$

Making the approximation that $f_0 << f_s$ ($OSR >> 1$) so that $\sin\left(\frac{\pi f}{f_s}\right) \approx \frac{\pi f}{f_s}$:

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_0}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3, \quad OSR = \frac{f_s}{2f_0}$$

It is assumed that the maximum signal power is the same as obtained before, in equation 14.11 ($P_s = \Delta^2 2^{2N}/8$), making maximum SNR:

$$SNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}\cdot 2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right], \text{ or:}$$

$$\boxed{SNR_{max} = 6.02N + 1.76 - 5.17 + 30\log(OSR)}$$

Doubling the OSR gives an SNR improvement for a 1st order modulator of 9 dB/octave or, equiv. 1.5 bits/octave.

Quantization noise power for linearized model of a general ΔΣ modulator

$$P_e = \int_{-f_0}^{f_0} S_e^2(f)\,|N_{TF}(f)|^2\,df = \int_{-f_0}^{f_0}\left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \quad (14.23)$$

Using the approximation that $f_0 << f_s$ (i.e. $OSR >> 1$) so that we may approximate $\sin\frac{\pi f}{f_s}$ to be $\frac{\pi f}{f_s}$:

$$P_e = \int_{-f_0}^{f_0}\frac{\Delta^2}{12}\frac{1}{f_s}\left[2\frac{\pi f}{f_s}\right]^2 df = \int_{-f_0}^{f_0}\frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2}\cdot f^2\,df$$

Letting $K = \frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2}$

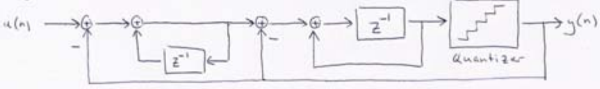
$$P_e = K\int_{-f_0}^{f_0} f^2\,df = \frac{K}{3}\left(f_0^3 - (-f_0)^3\right) = \frac{K}{3}\cdot 2f_0^3$$

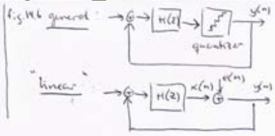
$$= \frac{\Delta^2}{12}\frac{1}{f_s}\frac{4\pi^2}{f_s^2\cdot 3}\cdot f_0^3 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\cdot\frac{2\cdot 2\cdot 2}{f_s^3}\cdot f_0^3 = \frac{\Delta^2}{12}\frac{\pi^2}{3}\left(\frac{2f_0}{f_s}\right)^3$$

Using $\boxed{OSR = \frac{f_s}{2f_0}} \Leftrightarrow \frac{2f_0}{f_s} = \frac{1}{OSR}$: $P_e = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \quad (14.24)$

Second-order noise shaping

Fig. 14.10 2nd order modulator





The above modulator realizes 2nd order noise shaping.

The signal transfer function is given by

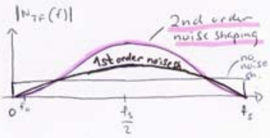
$$S_{TF}(f) = z^{-1}$$

The noise transfer function is given by

$$N_{TF}(f) = (1 - z^{-1})^2$$

Magnitude: $|N_{TF}(f)| = \left[2 \sin\left(\frac{\pi f}{f_s}\right)\right]^2$

fig. 14.11:



The quantization noise power over the frequency band of interest: $P_e \cong \frac{\Delta^2 \pi^4}{60}\left(\frac{1}{OSR}\right)^5$

Max SNR:

$$SNR_{max} = 10 \log\left(\frac{P_s}{P_e}\right) = 10 \log\left(\frac{3}{2} 2^{2N}\right) + 10 \log\left[\frac{5}{\pi^4}(OSR)^5\right]$$

or:

$$SNR_{max} = 6.02N + 1.76 - 12.9 + 50 \log(OSR) \quad (14.32)$$

Doubling the OSR improves the SNR for a 2nd order mod. by 15dB.

Ex. 14.5 p. 545:
1-bit A/D, 6-bit SNR. f_0 = 25 kHz
96 dB SNR is the goal.
Sample rate needed?
- oversampling: 54 THz
- 1st order n.s.: 75 MHz
- 2nd order n.s.: 5.8 MHz

ETET

14.3 System Architectures (A/D)

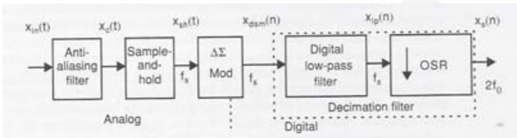
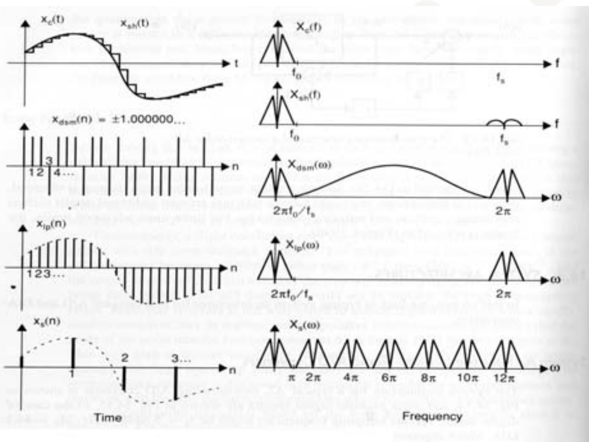


Fig. 14.14 Block diagram of an oversampling A/D converter.



- $X_c(t)$ is sampled and held, resulting in $x_{sh}(t)$.
- $x_{sh}(t)$ is applied to an A/D Sigma Delta modulator which has a 1-bit output, $x_{dsm}(n)$. The 1-bit signal is assumed to be linearly related to the input $X_c(t)$ (accurate to many orders of resolution), although it includes a large amount of out-of-band quantization noise (seen to the right).
- A digital LP filter removes any high frequency content, including out of band quantization noise, resulting in $X_{lp}(n)$
- Next, $X_{lp}(n)$ is resampled at $2f_0$ to obtain $X_s(n)$ by keeping samples at a submultiple of the OSR

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System Architectures (D/A)

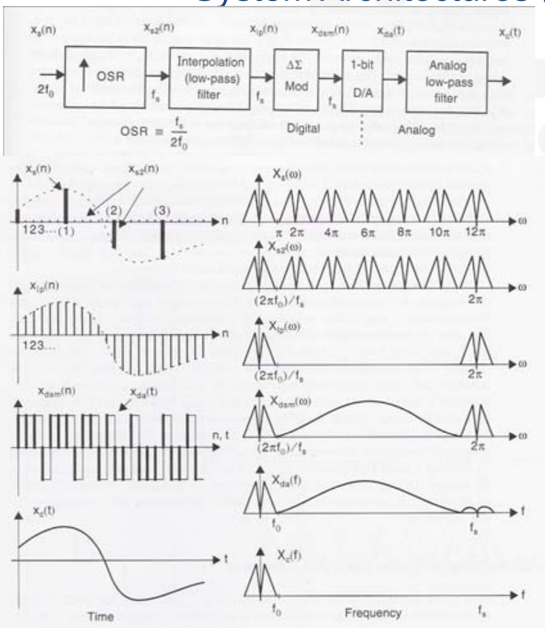

Fig. 14.17 Signals and spectra in an oversampling D/A converter.

- The digital input, $X_s(n)$ is a multi-bit signal and has an equivalent sample rate of $2f_0$, where f_0 ,is slightly higher than the highest input signal frequency.
- Since $X_s(n)$ is just a series of numbers the frequency spectrum has normalized the sample rate to 2π.
- The signal is upsampled to an equivalent higher sampling rate, f_s, resulting in the signal $x_{s2}(n)$
- $x_{s2}(n)$ has images left that are filtered out by the interpolation filter (brick-wall type) to create the multi-bit signal $X_{lp}(n)$, by digitally filtering out the images.
- $X_{lp}(n)$ is applied to a fully digital sigma delta modulator producing the 1-bit signal, $X_{dsm}(n)$, containing shaped quantization noise.
- $X_{dsm}(n)$ is fed to a 1-bit D/A producing $X_{da}(t)$, which has excellent linearity properties but still quantization noise.
- The desired signal, $X_c(t)$ can be obtained by using an analog filter to filter out the out-of-band quantization noise. (filter should be at least one order higher than the modulator.)

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14.4 Digital decimation filters

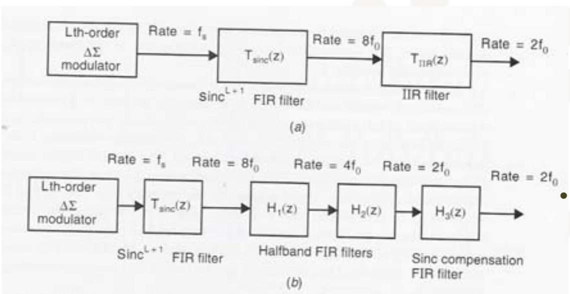

Fig. 14.18 Multi-stage decimation filters: (a) sinc followed by an IIR filter; (b) sinc followed by halfband filters.

- Many techniques
- a) FIR filter removes much of the quantization noise, so that the output can be downsampled by a 2nd stage filter which may be either IIR type (as in a), uppermost) or a cascade of FIR filters (as in b), below)
- In b) a few halfband FIR filters in combination with a sinc compensation FIR-filter are used.

  In some applications, these halfband and sinc compensation filters can be realized using no general multi-bit multipliers [Saramaki, 1990]

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14.5 Higher-Order Modulators – Interpolative structure

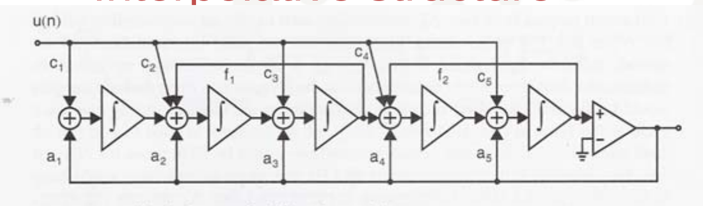

Fig. 14.20 A block diagram of a fifth-order modulator.

- Lth order noise shaping modulators improve SNR by 6L+3dB/octave.
- Typically a single high-order structure with feedback from the quantized signal.
- In figure 14.20 a single-bit D/A is used for feedback, providing excellent linearity.
- Unfortunately, modulators of order two or more can go unstable, especially when large input signals are present (and may not return to stability) Guaranteed stability for an interpolative modulator is nontrivial.

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Multi-Stage Noise Shaping architecture ("MASH")

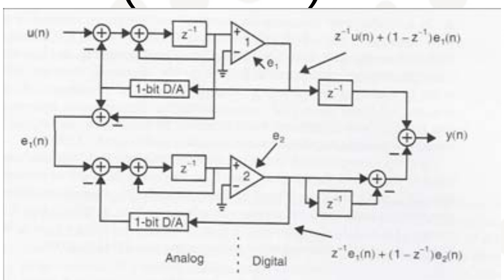

Fig. 14.21 A second-order MASH modulator using two first-order modulators. Note that the output, y(n), is a four-level signal.

- Overall higher order modulators are constructed using lower-order, more stable, ones → more stable overall system.
- Fig. 14.21: 2nd order using two first-order modulators.
- Higher order noise filtering can be achieved using lower-order modulators.
- Unfortunately sensitive to finite opamp gain and mismatch

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14.7 Practical considerations

- Stability
- Linearity of two-level converters
- Idle tones
- Dithering
- Opamp gain

(1/3 + 1/24) = 3/8 to the same modulator. For this case, the output sequence becomes

$$y(n) = \{1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, \dots\} \quad (14.47)$$

The period of this output pattern is now 16 cycles long and has some power at $f_s/16$. With an oversampling ratio of eight (i.e., $f_0 = f_s/16$), the post low-pass filter will not attenuate the signal power at $f_s/16$ since that frequency is just within the frequency band of interest. In other words, a dc level of 3/8 into this modulator will produce the correct dc output signal but ...

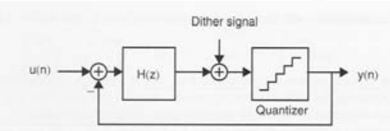
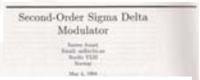


Fig. 14.26 Adding dithering to a delta-sigma modulator. Note that the dithered signal is also noise shaped.

Design example, 14b 2nd order Sigma-Delta mod



BOSER AND WOOLEY: SIGMA-DELTA MODULATION ANALOG-TO-DIGITAL CONVERTERS

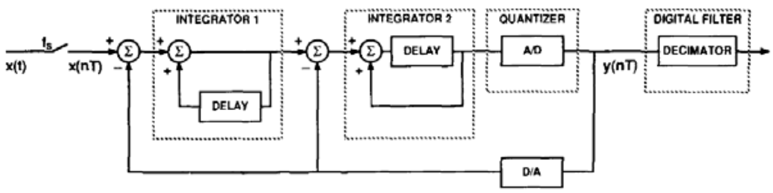


Fig. 1. Block diagram of second-order ΣΔ modulator with decimator.

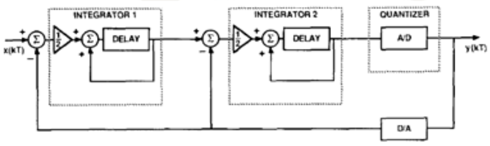


Fig. 2. Modified architecture of second-order ΣΔ modulator.

- 16 bit, 24 kHz , OSR as powers of two, and allowing for increased baseband noise due to nonidealities: OSR 512 was chosen

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Design example, 14b 2nd order Sigma-Delta mod

- Among most relevant nonidealities:
- Finite DC gain
- Bandwidth,
- Slew rate
- Swing limitation
- Offset voltage
- Gain nonlinearity
- Flicker noise
- Sampling jitter
- Voltage dependent capacitors
- Switch on-resistance
- Offset voltage and settling time for comparators

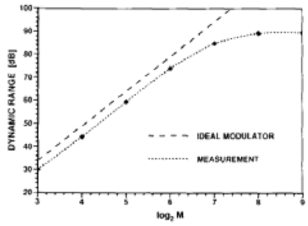
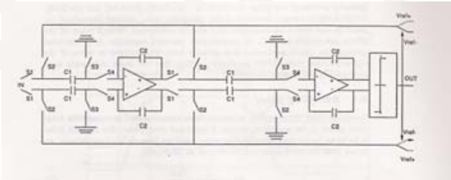
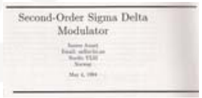
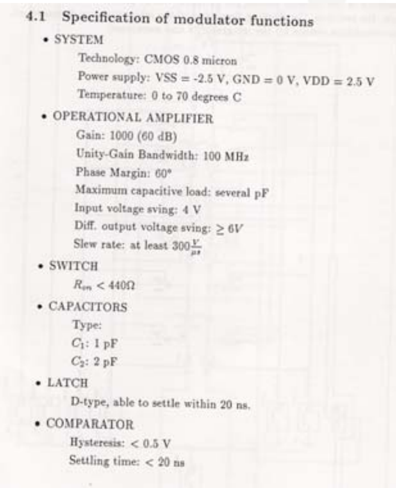


Fig. 15. Dynamic range as a function of the oversampling ratio for a sampling frequency of 4 MHz.



Design example, 14b 2nd order Sigma-Delta mod


Second-Order Sigma Delta Modulator



4.1 Specification of modulator functions

- SYSTEM
  - Technology: CMOS 0.8 micron
  - Power supply: VSS = -2.5 V, GND = 0 V, VDD = 2.5 V
  - Temperature: 0 to 70 degrees C
- OPERATIONAL AMPLIFIER
  - Gain: 1000 (60 dB)
  - Unity-Gain Bandwidth: 100 MHz
  - Phase Margin: 60°
  - Maximum capacitive load: several pF
  - Input voltage swing: 4 V
  - Diff. output voltage swing: $\geq 6V$
  - Slew rate: at least $300\frac{V}{\mu s}$
- SWITCH
  - $R_{on} < 440\Omega$
- CAPACITORS
  - Type:
  - C_1: 1 pF
  - C_2: 2 pF
- LATCH
  - D-type, able to settle within 20 ns.
- COMPARATOR
  - Hysteresis: < 0.5 V
  - Settling time: < 20 ns

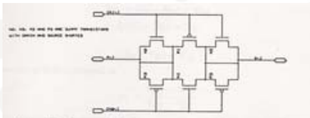


Figure 11: Dummy switch charge injection ...

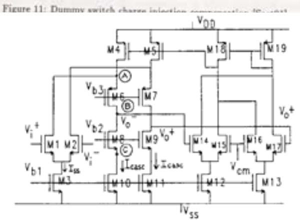
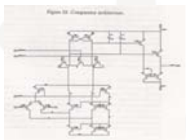
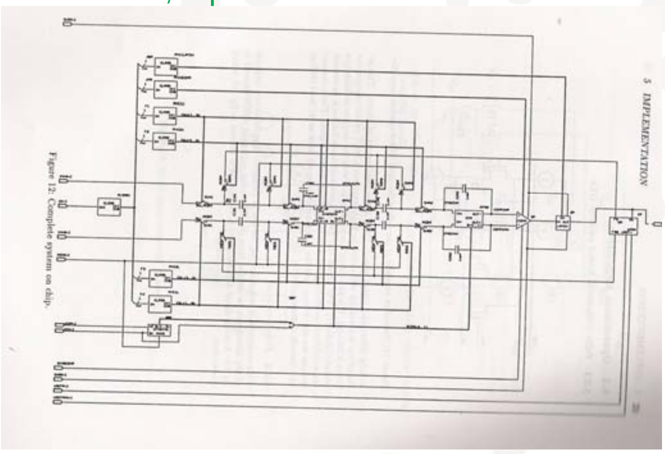


Fig. 1. Fully differential folded-cascode amplifier (after [4]).



- Noninverting parasitic insensitive integrator (fig 10.9) was used (fully differential implementation)

2nd order modulator; top level schematics

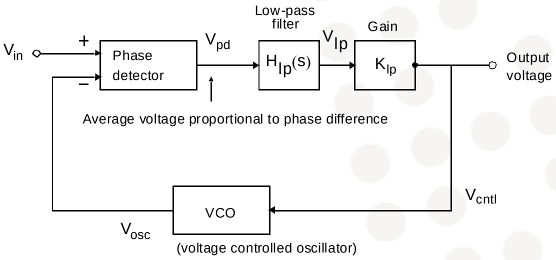


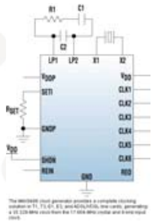
- Two-phase clock generator, switches, chopper stabilized OTA (1st int.), OTA (2nd int.- fully differential folded cascode), comparator, latch, two-level DAC. Biasing circuit. Functional after test.

Phase-locked loops (chapter 16)

- **Phase-locked loop**
- From Wikipedia, the free encyclopedia
- A **phase-locked loop** or **phase lock loop** (PLL) is a control system that generates a signal that has a fixed relation to the phase of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A phase-locked loop is an example of a control system using negative feedback.
- Phase-locked loops are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors. Since a single integrated circuit can provide a complete phase-locked-loop building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a cycle per second up to many gigahertz.

Phase-locked loops (chapter 16)





- Clock multiplication:
  - The input signal is reference oscillator with fixed frequency
  - The PLL output is a signal with frequency N times the input frequency where N is an integer
- Data recovery and clock resynchronization:
  - The input signal is a digital signal containing data
  - The output is digital data at a certain clock rate
  - The system clock is recovered from the digital input signal
- Frequency synthesis (ex: to select channels in television or wireless communication systems):
  - The input signal is reference oscillator with fixed frequency
  - The PLL output is a signal with frequency N times the input frequency where N may be a fractional number
- FM demodulation:
  - The input is a FM signal (IF)
  - The output is the demodulated baseband signal

Phase-Locked Loop, typical architecture

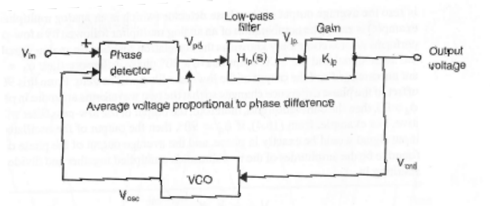
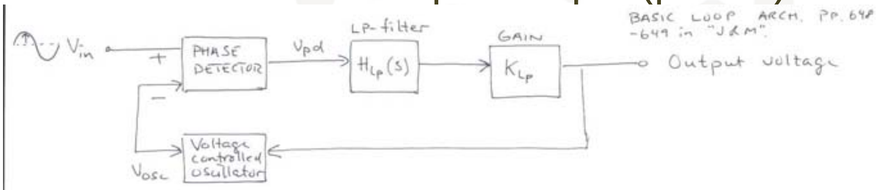


Fig. 16.1 The basic architecture of a phase-locked loop.

- The *phase detector* ("PD") normally has an output voltage with an average value proportional to the phase difference between the input signal and the output of the VCO ("Voltage Controlled Oscillator").
- The *low-pass filter* is used to extract the average value from the output of the PD.
- The average value is amplified by the *Gain* block and used to drive the VCO.
- The negative feedback of the loop results in the output of the VCO being synchronized with the input signal.

Phase-locked loop example (p. 649)

BASIC LOOP ARCH. PP. 648–649 in "J&M".



- The input signal, V_{in}, is assumed to be a sinusoid with known amplitude.
- The phase detector is realized as an analog multiplier with $V_{pd} = K_M \cdot V_{in} \cdot V_{osc}$ ∧ K_M: multiplication constant.
- $H_{LP}(s) = \dfrac{1 + s\tau_z}{1 + s\tau_p}$, $\tau_z << \tau_p$; first-order LEAD-LAG filter.
- $V_{in} = E_{in} \cdot \sin(\omega t)$
- $V_{osc} = E_{osc} \sin(\omega t - \Phi_d + 90^\circ) = E_{osc} \cos(\omega t - \Phi_d)$

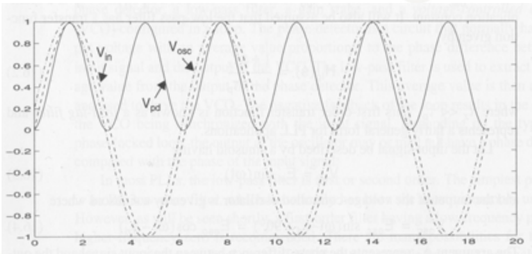
Φ_d represents the phase difference between the input signal and the output of the oscillator. The reason for the 90° offset is that the PD (analog mult.) has a zero average output for a phase difference of zero.

V_{in} and V_{osc} exactly in phase when Φ_d=90º

- $V_{in} = E_{in} \sin(\omega t)$,
- Vosc = $E_{osc} \sin(\omega t - \Phi_d + 90^\circ) = E_{osc} \sin(\omega t - 90^\circ + 90^\circ) = E_{osc} \sin(\omega t)$
- The input signal and the output of the oscillator will be exactly in phase, and the output from the phase detector (" PD") is found to be the amplitudes of the two sinusoids multiplied together and divided by 2, resulting in

$V_{cntl} = K_{lp} K_M E_{in} E_{osc}/2$ (Eq. 16.5, p 650 in J&M)

Fig. 16.2, below, shows the output from the PD when V_{in} and V_{osc} are nearly in phase.



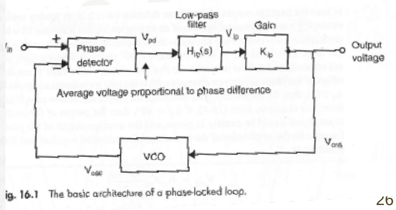
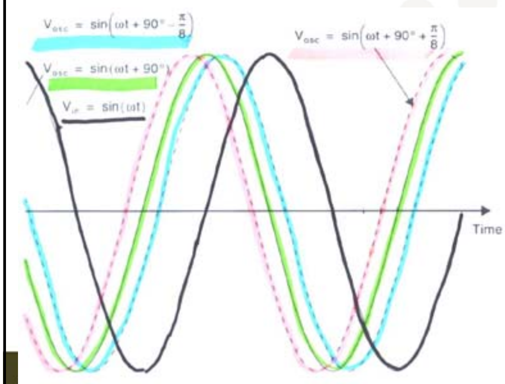


Fig. 16.1 The basic architecture of a phase-locked loop.

Examples of different waveforms, as a function of different Φ_d,
(J&M p 650-651 ,fig. 16.3)

- $V_{osc} = E_{osc}\sin(\omega t - \Phi_d + 90°) = E_{osc}\cos(\omega t - \Phi_d)$ (16.4)
- $\Phi_d > 0$ corresponds to waveforms that are more in phase.
- When the input signal and VCO output have a 90º phase diff. ($\Phi_d = 0$), they are uncorrelated and the output of the LP-filter will be zero.)



he relative phase angles of the input signal and the output of the oscillator.
Fig. 16.3

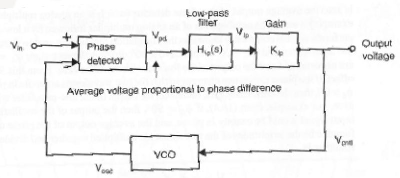
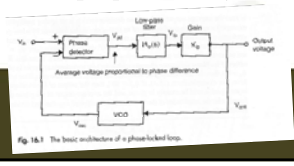


Fig. 16.1 The basic architecture of a phase-locked loop.

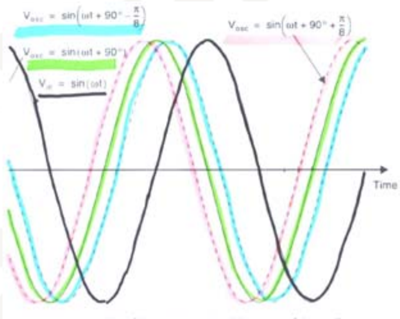
Some relevant mathematical relationships from 16.1, pages 650-652 in "J&M"

- The output of the phase detector:
- $Vpd = K_M V_{in} V_{osc} = K_M E_{in} E_{osc} \sin(\omega t)\cos(\omega t-\Phi_d)$ (16.6)
- Using $\sin(A)\cos(B) = (1/2)[\sin(A+B)+\sin(A-B)]$ we have
  $Vpd = K_M V_{in} V_{osc}/2\ [\sin(\Phi_d)+2\sin(2\omega t-\Phi_d)]$ (16.8)
- The LP-filter removes the second term at twice the frequency of the input signal, so V_{cntl} is therefore given by
  $V_{cntl} = K_{lp} K_M (E_{in} E_{osc}/2) \sin(\Phi_d)$ (16.9)
- Since V_{cntl} is either a dc value or slowly varying, for small Φ_d the following approximation for (16.9) may be used:
  $V_{cntl} \approx K_{lp}\, K_M (E_{in} E_{osc}/2)\, \Phi_d \quad = \quad K_{lp} K_{pd}\, \Phi_d$ (16.10)
  Thus, the output of the LP-filter is approximately proportional to the phase difference between the output of the oscillator and the input signal, assuming the 90 ofset bias is ignored. The approximation is used in analyzing the PLL to obtain a linear model. The constant of proportionality is called K_{pd} and is given by
  $Kpd = K_M (E_{in} E_{osc}/2)$ (16.11)



More on PLL operation (p. 652-653)

- Assume that the VCO has a free-running frequency ω_{fr} when it's input is zero, and that the input signal is initially equal to ω_{fr}, and the system has $\Phi_d = 0$ (in lock).
- NEXT, assume the input frequency slowly increases. Now, with $\Phi_d > 0$, the two waveforms will become more in phase (See fig. 16.3). After a short time the output of the LP-filter will go positive. Since the two waveforms are at slightly different frequencies, the output of the LP-filter will slowly increase. Since the VCO frequency is proportional to V_{cntl}, this increase will cause the VCO frequency to increase until it is the same of that of the input signal again, which will keep the two signals in synchronism (i.e. locked). (The opposite would occur for a decrease in the input signal frequency.)



he relative phase angles of the input signal and the output of the oscillator.

Fig. 16.3

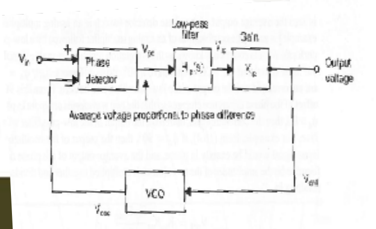


Fig. 16.1 The basic architecture of a phase-locked loop.

More on PLL operation (p. 652-653)

- At a new input frequency, ($\neq \omega_{fr}$) which does not equal the free-running frequency, we can find the new phase difference for the two locked signals by noting that the frequency of the oscillator's output signal is given by

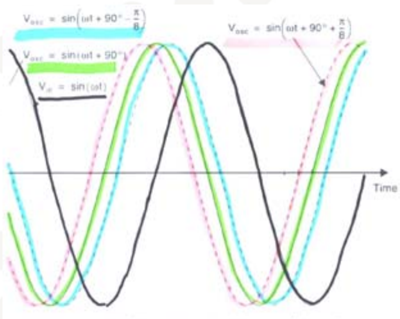
  $\omega_{osc} = K_{osc}V_{cntl} + \omega_{fr}$ (16.12).

  K_{osc} is a constant relating the change in frequency to control voltage ratio. The output voltage of the amplified LP-filter is now given by

  $V_{cntl} = (\omega_{in}\omega_{fr})/K_{osc}$ (16.13)

  where ω_{in} is the frequency of the input signal, which is equal to the frequency of the oscillator's output. From (16.10):

  $\Phi_d = V_{cntl}(K_{lp}K_{pd}) = (\omega_{in}-\omega_{fr})/K_{lp}K_{pd}K_{osc}$ (16.14)



he relative phase angles of the input signal and the output of the oscillator.

Fig. 16.3

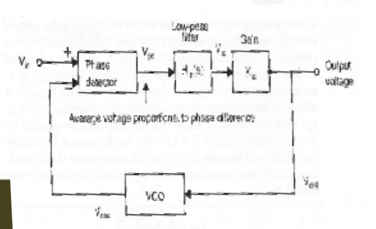
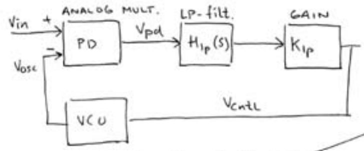


Fig. 16.1 The basic architecture of a phase-locked loop.

Ex. 16.2



Ex. 16.1 problem to the right

Ex. 16.1

Consider a PLL where the amplitudes of the inp. signal and the oscillator output are both at a 0.75 V peak. The analog mult. ~~which~~ would have 2V output when both inputs are DC values of 2V. The VCO free-running frequency is 10 MHz, and would decrease to zero for $V_{cntl} = -1V$. The gain block is unity, i.e. $K_{lp} = 1$. When in lock, what is the phase difference between the input and osc. output when $f_{in} = 11$ MHz? What is the phase difference when the input is 9 MHz? How does the phase difference change if $K_{lp} = 2$?

$$\Phi_d = \frac{V_{cntl}}{K_{lp} \cdot K_{pd}} = \frac{\omega_{in} - \omega_{fr}}{K_{lp} \cdot K_{pd} \cdot K_{osc}} \quad (16.14)$$

K_{pd} and K_{osc} are needed in 16.14:

The phase detector realized as an analog multiplier has the following relationship:

$V_{pd} = K_M \cdot V_{in} \cdot V_{osc}$ (16.1)

$$K_M = \frac{2.0\,V}{2.0V \cdot 2.0V} \quad \left(= \frac{V_{pd}}{V_{in} \cdot V_{osc}}\right) \Leftrightarrow \underline{K_M = 0.5\,\frac{1}{V}}$$

$$\underline{K_{pd}} = K_M \cdot \frac{E_{in} \cdot E_{osc}}{2} = 0.5\,\frac{1}{V} \cdot \frac{0.75V \cdot 0.75V}{2} = \underline{0.140625\,V}$$

$\underline{K_{osc}}$ is a constant relating the change in freq. to control voltage ratio: $\frac{\Delta\omega_{osc}}{\Delta V_{cntl}} = \frac{2\pi \cdot 10^7\,rad/s}{1V}$

Using 16.14: $\underline{\Phi_d} = \frac{2\pi\,(11\,MHz - 10\,MHz)}{K_{lp} \cdot K_{pd} \cdot K_{osc}} = 0.7112\,rad = \underline{\underline{40.8^\circ}}$

(Counting in 90° offset: 90° − 40.8° = 49.2°)

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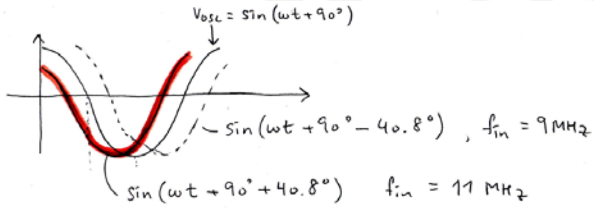
Ex. 16.1

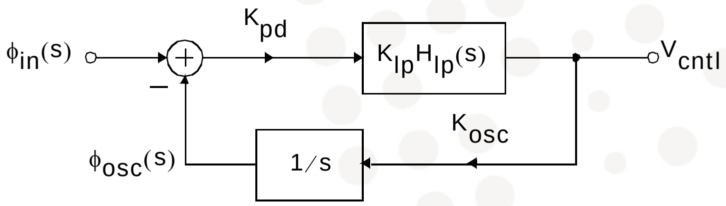


$f_{in} = 11$ MHz: The phase difference between the input and oscillator output becomes $90^\circ - 40.8^\circ = 49.2^\circ$.

$f_{in} = 9$ MHz: $\Phi_d = -40.8^\circ \Rightarrow$ phase difference of $90^\circ - (-40.8^\circ) = 130.8^\circ$

For $K_{lp} = 2$, half the phase difference results in the same VCO control voltage, V_{cntl}. So, for $\omega_{in} = 11$ MHz, $\Phi_d = \frac{40.8^\circ}{2} = 20.4^\circ$, and for 9 MHz, $\Phi_d = -20.4^\circ$. $\left(\text{Since } \Phi_d = \frac{\omega_{in} - \omega_{fr}}{K_{lp} \cdot K_{pd} \cdot K_{osc}}\right)$

Linear model of the PLL – when in lock



$$V_{cntl}(s) = K_{pd} K_{lp} H_{lp}(s) \left[\phi_{in}(s) - \phi_{osc}(s)\right]$$

$$\phi_{osc}(s) = \frac{K_{osc} V_{cntl}(s)}{s}$$

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PLL transfer functions

- Combining equations from previous slide:

$$\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{s K_{pd} K_{lp} H_{lp}(s)}{s + K_{pd} K_{lp} K_{osc} H_{lp}(s)}$$

- This is a highpass response from input phase to the control voltage.
- Rewriting gives:

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{K_{pd} K_{lp} K_{osc} H_{lp}(s)}{s + K_{pd} K_{lp} K_{osc} H_{lp}(s)}$$

- This is a lowpass response from the input phase

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Additional litterature

- Walt Kester: Which ADC Architecture is right for your application?, Analog Dialogue, Analog Devices, 2005.
- Behzad Razavi: "Design of Analog CMOS Integrated Circuits", McGraw-Hill, reprint 2009.
- Jimmy J. Cathey, Syed A. Nasar: Basic Electrical Engineering , Schaum's Outlines, McGraw Hill 1997.
- Richard Schreier, Gabor C. Temes: Understanding Delta-Sigma Data Converters, IEEE Press / Wiley Interscience, 2005
- Tapio Saramaki et. Al: Multiplier-Free Decimator Algorithms for Super-Resolution Oversampled Converters, IEEE International Symposium on Circuits and Systems, 1990.
- Bernhard A. Boser, Bruce A. Wooley: The Design of Sigma-Delta Modulation Analog-to-Digital Converters, IEEE Journal of Solid-State Circuits, December 1988.
- Sudhir M. Mallya, Joseph H. Nevin: Design Procedures for a Fully Differential Folded-Cascode CMOS Operational Amplifier , IEEE Journal of Solid-State Circuits, December 1989.
- http://www.wikipedia.org (on PLLs)
- Snorre Aunet: Second-Order Sigma Delta Modulator, Nordic VLSI, May 4, 1994.

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Next Time, 13/4-10:

- More from Chapter 16; PLLs
- About report writing

23.03.2010	SA	Lille Aud.	Chapter 14; Oversampling Converters	preliminary...Slides Slides, two per page
30.03.2010				No teaching in week 13.
06.04.2010				No teaching in week 14, due to Easter holidays.

13.04.2010	SA	Lille Aud.	chapter 16; PLLs	Later... Slides, Slides, two per page.

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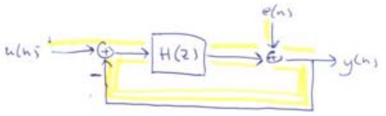
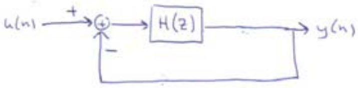
TRANSFER

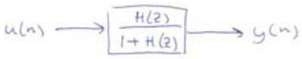


Johns & Martin are treating the linear model as having two independent inputs.

SIGNAL



Eliminating the feedback loop:



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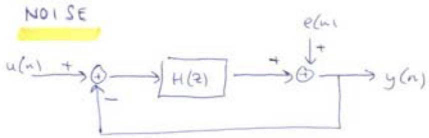
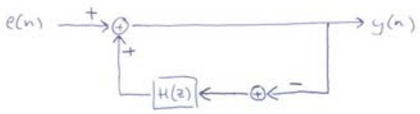
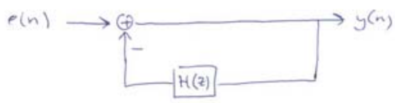
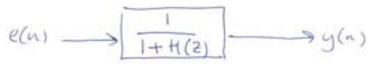
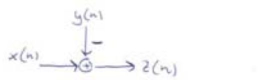
NOISE











$z(n) = x(n) - y(n)$

$$S_{TF}(z) \equiv \frac{Y(z)}{U(z)} \quad (14.15)$$

$$N_{TF}(z) \equiv \frac{Y(z)}{E(z)} \quad (14.16)$$

THE OUTPUT SIGNAL CAN BE WRITTEN AS A COMBINATION OF THE INPUT SIGNAL AND THE NOISE SIGNAL EACH BEING FILTERED BY THE CORRESPONDING TRANSFER FUNCTION.

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PLLs, report writing

Tuesday 13th of April, 2009, 9:15 – 11:00

Snorre Aunet, sa@ifi.uio.no
Nanoelectronics Group, Dept. of Informatics
Office 3432

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Last time – and today, Tuesday 13th of April:

March the 23rd:

14.2 Oversampling with noise shaping
14.3 System Architectures
14.4 Digital Decimation Filters
14.5 Higher-Order Modulators
(14.6 Bandpass Oversampling Converters)
14.7 Practical Considerations
14.8 Multi-bit oversampling converters
  2nd order sigma delta design example
16.1 Basic Phase Locked Loop Architecture

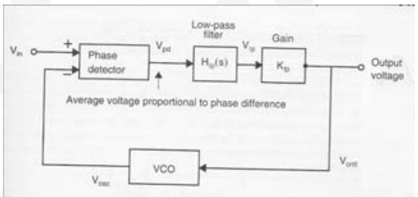

Fig. 16.1 The basic architecture of a phase-locked loop.

Today:
16.1Linearized small-signal analysis of general PLLs
16.2 PLLs with charge-pump phase comparators
16.3 Voltage controlled oscillators
16.4 Computer Simulations of PLLs
About writing the report

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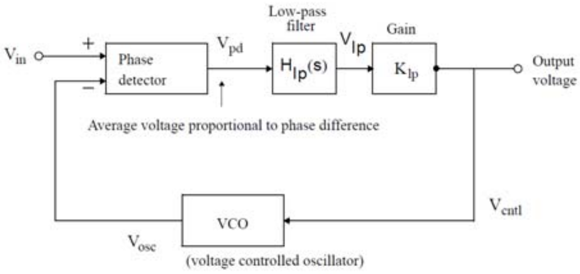
PLL Basic Architecture



- In general, output may be V_{cntl} or V_{osc}

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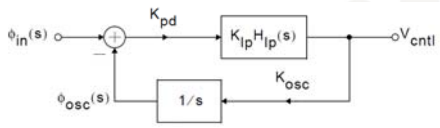
PLL linear model applying to almost every PLL



$$V_{cntl}(s) = K_{pd}K_{lp}H_{lp}(s)[\phi_{in}(s) - \phi_{osc}(s)]$$

$$\phi_{osc}(s) = \frac{K_{osc}V_{cntl}(s)}{s}$$

$$H_{lp}(s) = \frac{1 + s\tau_z}{1 + s\tau_p}$$

- Combining above 2 equations ...

$$\frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{sK_{pd}K_{lp}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a highpass response from input phase to control voltage
- Can also be written as

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{K_{pd}K_{lp}K_{osc}H_{lp}(s)}{s + K_{pd}K_{lp}K_{osc}H_{lp}(s)}$$

- This is a lowpass response from input phase to output phase

- Differences between PLLs are determined only by what is used for the LP-filter ($H_{lp}(s)$), the Phase Detector (K_{pd}) or the oscillator (K_{osc}).

12. april 2010

4

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More on the 2nd order PLL model

2nd order transfer functions are often written in the form

$$H(s) = \frac{N(s)}{D(s)}$$

$$D(s) = 1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}$$

ω_0: resonant frequency

Transient time for the complete loop:

$$\tau_{pll} \cong \frac{1}{\omega_0}$$

Q: Q-factor, damping factor

Good settling: $Q = 0.5$

max. flat group delay: $Q = \frac{1}{\sqrt{3}} = 0.577$

max. flat amplitude resp: $Q = \frac{1}{\sqrt{2}} = 0.707$

$$\omega_0 = \frac{K_{pll}}{\sqrt{\tau_p}} \quad (16.32)$$

$$Q = \frac{\sqrt{\tau_p}}{\frac{1}{K_{pll}} + \tau_z K_{pll}}$$

$$K_{pll} = \sqrt{K_{pd} \cdot K_{lp} \cdot K_{osc}}$$

Usually, when $\omega_0 << \omega_{lp}$:

$$Q \cong \frac{1}{\omega_0 \tau_z} = \frac{\sqrt{\tau_p}}{\tau_z K_{pll}} \quad (16.35)$$

When $Q = 0.5$:

$$\tau_z = \frac{2\sqrt{\tau_p}}{K_{pll}} = \frac{2}{\omega_0}.$$

Capture range, lock range, false lock

- The maximum difference between the input signal's frequency and the oscillator's free-running frequency where lock can eventually be attained is defined as the capture range
- One lock is attained, as long as the input signal's frequency changes only slowly it will remain in lock over a range that is much larger than the capture range
- When a multiplier is used for the phase detector the loop may lock to harmonics (multiple of the frequency) of the input signal. This is called a false lock.

Exclusive-OR Phase comparators

V_{in}	V_{osc}	V_{pd}
0	0	0
0	1	1
1	0	1
1	1	0

put given by $V_{pd} = V_{in} \oplus V_{osc}$, where the amplitudes of the signals are determin by the logic levels. Some typical waveforms are shown in Fig. 16.6. It is seen tl

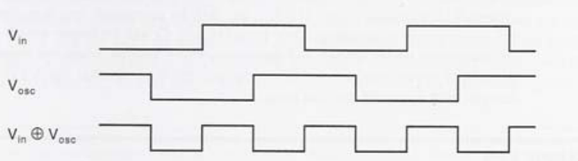

Fig. 16.6 Typical waveforms when an exclusive-OR gate is used as a phase comparator

- When the waveforms are 90 degrees out of phase the output is a waveform at twice the frequency of the input signal and has a 50 percent duty cycle.
- If all waveforms are symmetric about 0 volts the average value extracted by the low-pass filter would be zero.

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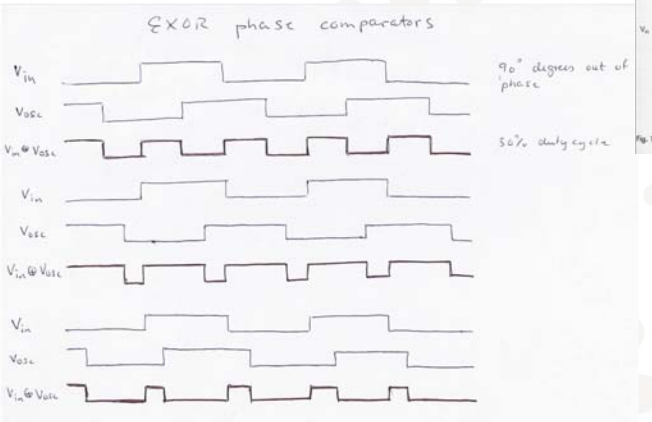
EXOR phase comp



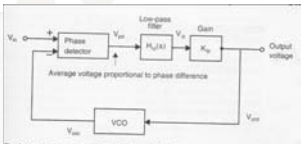


Fig. 16.1 The basic architecture of a phase-locked loop.

- When the waveforms become more out of phase, the average value of the output signal is positive; whereas when they become more in phase, the average value of the output signal is negative

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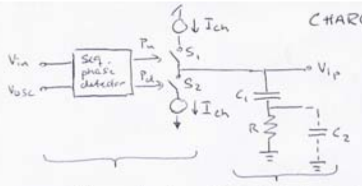
CHARGE-PUMP COMPARATOR

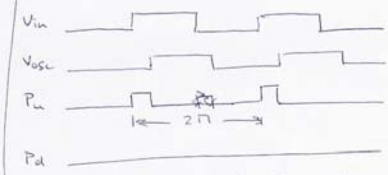


- no false lock, attains lock quickly
- V_{in} and V_{osc} are exactly in phase when the system is in lock.
- injects, leaves alone, or subtracts charge on the capacitor in the LP-filter, depending on P_u and P_d.
- S_1 closed: I_{ch} increases the control voltage into the VCO

  S_2 closed: I_{ch} flows out of the LP-filter, decreasing the control voltage.

  S_1 and S_2 open: Steady state
- P_u and P_d are digital signals
- IF V_{in} goes to 1 before V_{osc}, then P_u will be 1 during the time that the signals are different. ⇒ injecting charge

  ELSE if V_{osc} goes to 1 before V_{in}, P_d will be 1 during the time that the input's are different ⇒ S_2 will be closed, removing charge from the loop-filter and decreasing the VCO frequency.



OBS! Notice that P_u only goes high at the leading edges and is insensitive to the falling edges.

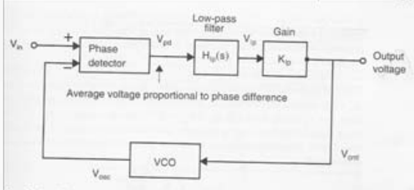
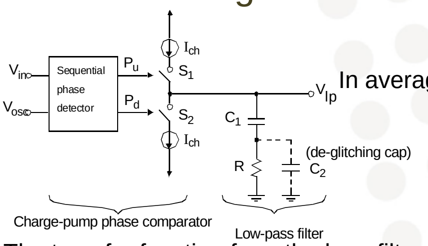


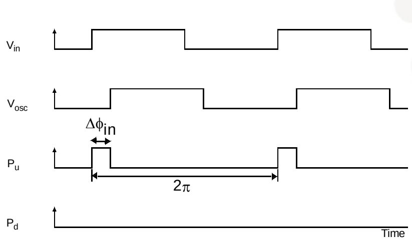
Fig. 16.1 The basic architecture of a phase-locked loop.

Small-Signal Model of the Charge-Pump PLL



In average the current from the CP is: $I_{avg} = \frac{\Delta\phi_{in}}{2\pi} I_{ch}$

The transfer function from the loop filter is (C2 ignored):



$$H_{lp}(s) = \frac{V_{lp}(s)}{I_{avg}(s)} = R + \frac{1}{sC_1} = \frac{1 + sRC_1}{sC_1}$$

$$\frac{\phi_{osc}(s)}{\phi_{in}(s)} = \frac{(1 + sRC_1)}{1 + sRC_1 + \frac{s^2 C_1}{K_{pd} K_{osc}}}$$

$$\omega_0 = \frac{1}{\tau_{pll}} = \sqrt{\frac{I_{ch} K_{osc}}{2\pi C_1}}$$

$$Q = \frac{1}{RC_1\omega_0} = \frac{1}{R}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}}$$

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Ex. 16.4

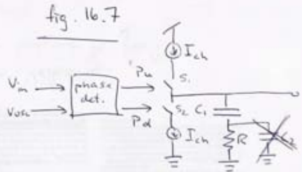
Ex. 16.4

$K_{osc} = 2\pi \times 50$ Mrad/V

$I_{ch} = 10\ \mu A$. $\omega_{fr} = 50$ MHz

and the loop has a time constant of 100 cycles, or $2\mu s$. Design the components of the LP-filter in fig. 16.7

fig. 16.7



$$\omega_0 = \frac{1}{2\mu s} = 500\ \text{k rad/s}$$

$$\omega_0 = \sqrt{\frac{K_{pd} \cdot K_{osc}}{C_1}} \wedge K_{pd} = \frac{I_{ch}}{2\pi} \quad (16.60 \wedge 16.56)$$

$$\omega_0^2 = \frac{K_{pd} \cdot K_{osc}}{C_1} \Leftrightarrow C_1 = \frac{K_{pd} \cdot K_{osc}}{\omega_0^2}$$

$$C_1 = \frac{I_{ch}}{2\pi} \cdot \frac{K_{osc}}{\omega_0^2}$$

$$= \frac{10\mu A}{\cancel{2\pi}} \cdot \frac{\cancel{2\pi} \times 50\ \text{M rad/s}}{(500\ \text{k rad/s})^2} = 2\text{nF}$$

Let $C_2 = \frac{C_2}{10} = 200$ pF

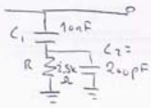
Let $Q = 0.4$

From 16.61 :

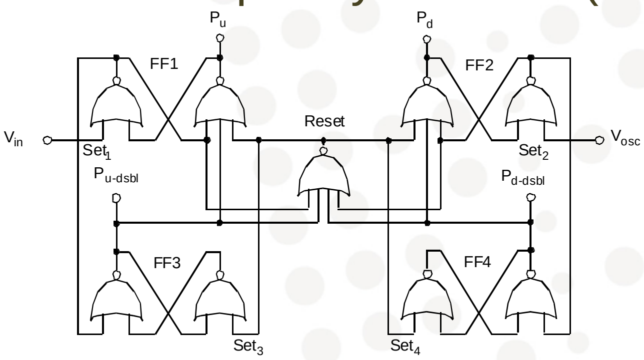
$$Q = \frac{1}{RC_1\omega_0} = \frac{1}{R}\sqrt{\frac{2\pi}{C_1 I_{ch} K_{osc}}}$$

$$R = \frac{1}{Q}\sqrt{\frac{2\pi}{2\text{nF} \cdot 10\mu A \cdot 2\pi 50\ \text{M rad/s}}}$$

$$= \underline{2.5\ \text{k}\Omega}$$

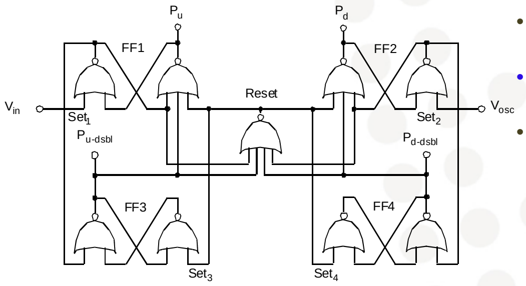


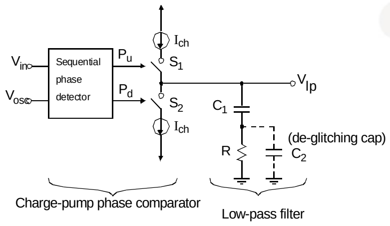
Phase Frequency Detector (PFD)



- Most commonly used sequential phase detector is the Phase Frequency Detector (PFD).
- This circuit handles phase differences up to 2π.

Phase Frequency Detector (PFD)

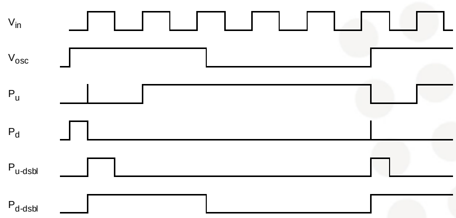


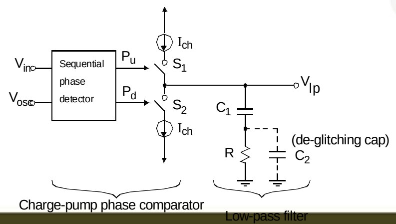


- Assume P_u, P_d, $P_{u\text{-dsbl}}$, $P_{d\text{-dsbl}}$, Reset, V_{in}, V_{osc} are low
- V_{in} goes high; FF1 set/ Pu goes high -> VCO frequency increases
- V_{osc} goes high; FF2 set temporarily, reset goes high, causing P_u and P_d go low after some delay. Reset going high causes FF3 and FF4 to be set and $P_{u\text{-dsbl}}$ and $P_{d\text{-dsbl}}$ go high, which later causes reset to go low. FF1 and FF2 are kept in reset mode and P_u and P_d low.
- V_{in} goes back to 0; FF3 reset and $P_{u\text{-dsbl}}$ is turned off.
- Similarly, when V_{osc} goes low, FF4 is reset goes low, FF4 is reset and $P_{d\text{-dsbl}}$ goes low. (back to original state).

  (The operation is very similar if V_{osc} leads V_{in})

PFD waveforms – when V_{in} has a much higher frequency than Vosc





- Whenever a positive going edge of Vin occurs, Pu goes high causing the VCO frequency to increase, and stays high until both Vin and Vosc go to 1. Then reset goes high, setting both Pu-dsbl and Pd-dsbl, and causing Pu and Pd to go low. The next time Vin goes to o, FF1 is reset, which resets FF3, turning Pu-dsbl off.
- Most of the time (here) Pu is high, causing Vosc to quickly increase in frequency until lock is achieved.
- No false lock
- Only suitable for digital (non-sine) inputs

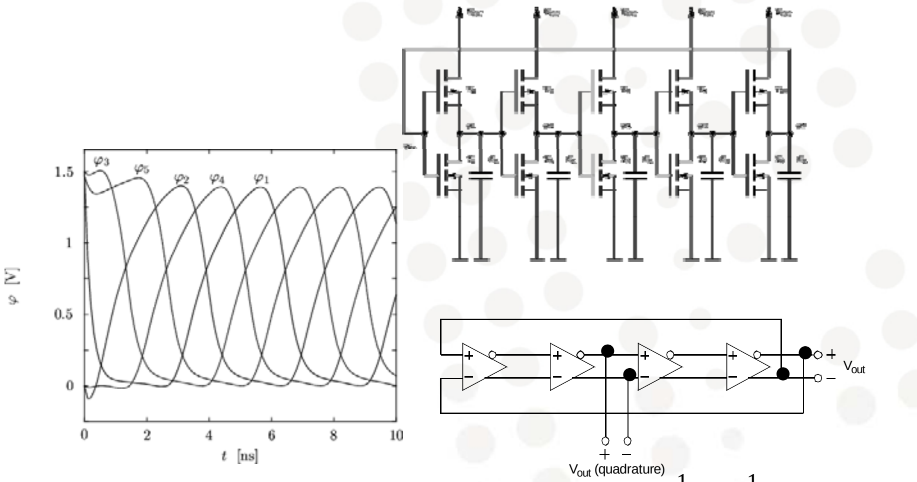
Voltage controlled oscillators (VCO)

Oscillators

- Tuned oscillators
  - RC osc.
  - SC osc.
  - LC osc.
  - Crystal osc.
- Nonlinear oscillators
  - Relaxation osc.
  - Ring osc.

- Sinusoidal output oscillators usually realized some frequency selective or tuned circuit in feedback configuration, while square-wave output oscillators are usually realized using a nonlinear feedback config.
- The tuned oscillators offers better frequency stability, but limited tuning range.

Ring oscillators



τ_{inv} is the delay of each inverter

$$f_{osc} = \frac{1}{T} = \frac{1}{2n\tau_{inv}}$$

0.2 V subthreshold VCO

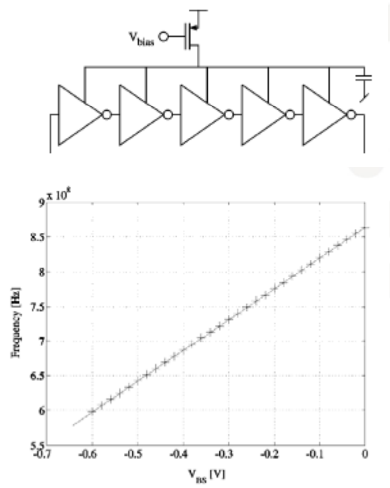


Figure 3. RVCO transfer function for a 5 stage RVCO simulated in Cadence

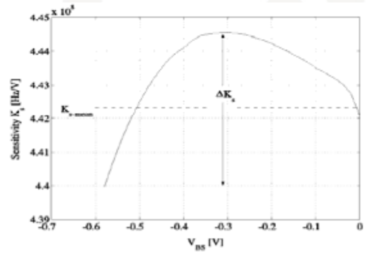


Figure 4. Sensitivity of the RVCO illustrates a nonlinearity of 0.5 %

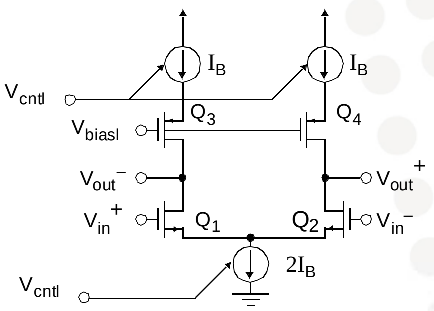
Linearity of Bulk-Controlled Inverter Ring VCO in Weak and Strong Inversion

Ulrik Wismar, Dag Wisland**, Pietro Andreani**

*Centre for Physical Electronics, Orsted•DTU
Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark

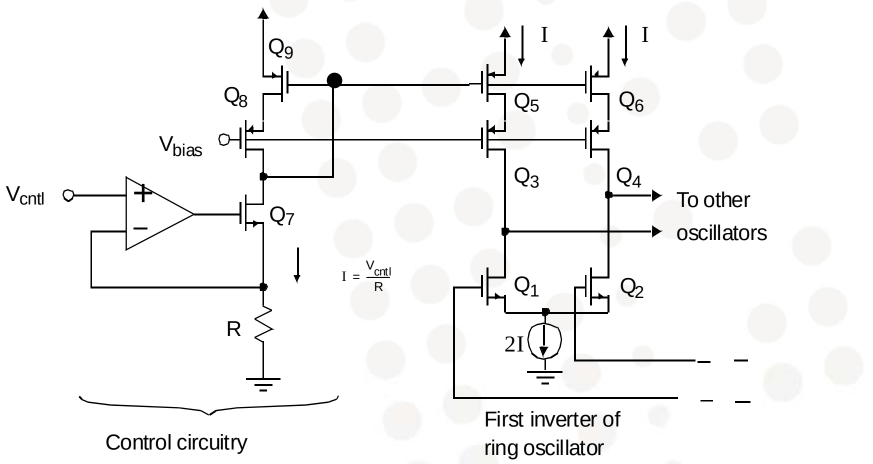
**Microelectronic Systems, Department of Informatics
University of Oslo, N-0316 Oslo, Norway

Differential inverter



- Programmable delay
- Cascode transistors Q3, Q4 to increase output impedance of programmable current sources for better PSRR
- I_B = Kbias Vcntl (proportional)
- Tau proportional to C_L / g_m, f_{osc} proportional to SQRT(V_{cntl}) ;nonlinear

Bias circuit



Computer simulations of PLLs

- Nontrivial due to often very wide range of time constants present in PLLs.
- SPICE simulations only may be highly impractical and take too long time.
- Possible approach:

  Simulate the individual components using SPICE over a few periods of the VCO's output waveform before simulating the complete system using simplified models where continous time components are replaced by approximately equivalent difference-equation models;

  Simulink in Matlab (easy, don't need much expertise)

  or custom difference equations using for example C. (fast and may be modified for greater accuracy)

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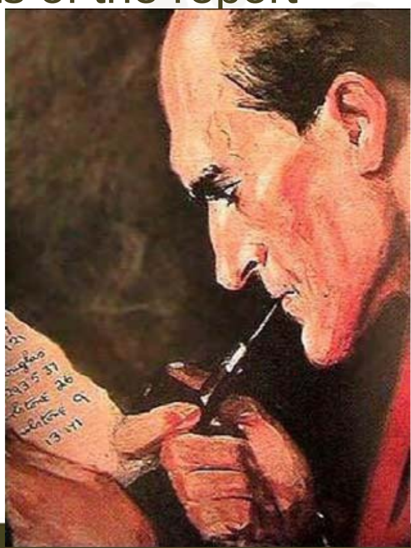
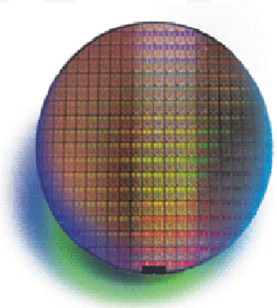
Additional litterature

- Ulrik Wismar, Dag T. Wisland, Pietro Andreani: Linearity of Bulk-Controlled Inverter Ring VCO in weak and strong inversion, Proceedings of IEEE Norchip Conference, 2005.
- http://www.eecg.toronto.edu/~johns/nobots/Book/book.html
- http://www.iue.tuwien.ac.at/phd/grasser/node83.html (Ring osc.)

Remember: Grading is based on the contents of the report





Some pointers

- http://www.idi.ntnu.no/~lasse/DM/SkriveTips.php

- **Preface**
- **(Acknowledgement)**
- **1 Introduction**
- **2 Theoretical background**
- **(2.1 Various approaches to Nifty Gadgets)**
- **2.2 Nifty Gadgets my way**
- **3 My implementation of a Nifty Gadget**
- **4 Nifty Gadget results**
  5 Discussion

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Nifty Gadget / DAC chapter 3

- **3 My implementation of a Nifty Gadget**
- Can you describe your implementation in detail?
  Why did you use this technology?
  How does the theory relate to your implementation?
  What are your underlying assumptions?
  What did you neglect and what simplifications have you made?
  What tools and methods did you use?
  Why use these tools and methods?

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Nifty Gadget / DAC chapter 4

- **4 Nifty Gadget results**
- Did you actually build it?
  How can you test it?
  How did you test it?
  Why did you test it this way?
  Are the results satisfactory?
  Why should you (not) test it more?
  What compensations had to be made to interpret the results?
  Why did you succeed/fail?

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Nifty Gadget / DAC chapter 5

- **5 Discussion**
- Are your results satisfactory?
  Can they be improved?
  Is there a need for improvement?
  Are other approaches worth trying out?
  Will some restriction be lifted?
  Will you save the world with your Nifty Gadget?

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Guide to writing a thesis

Guide to Writing a Thesis — Page 1 of 4

Guide to Writing a Thesis

Department of Applied Electronics
Last updated 1997-03-12

Original manuscript written by Sven Mattisson

The Design and Implementation of a Nifty Gadget

Tekla-Liz Book

April 32, 1992

Abstract
What is all this about?
Why should I read this thesis?
Is it any good?
What's new?

Preface

Have you done anything that doesn't have to do with your research?
Have you published parts of this work before?

Acknowledgement

Who is your adviser?
Did anyone help you?
Who funded this work?
What's the name of your favorite pet?

1 Introduction

What is the use of a Nifty Gadget?
What is the problem?
How can it be solved?
What are the previous approaches?
What is your approach?
Why do it this way?
What are your results?
Why is this better?
Is this a new approach?
Why haven't anyone done it before?
or
Why do you reiterate previous work?
What is your contribution to the field of Nifty Gadgets?

Guide to Writing a Thesis — Page 2 of 4

2 Theoretical background

What is the required background knowledge?
Where can I find it?

2.1 Various approaches to Nifty Gadgets

What is the relevant prior work?
Where can I find it?
Why should it be done differently?
Has anyone attempted your approach previously?
Where is that work reported?

2.2 Nifty Gadgets my way

What is the outline of your way?
Have you published it before?

3 My implementation of a Nifty Gadget

Can you describe your implementation in detail?
Why did you use this technology?
How does the theory relate to your implementation?
What are your underlying assumptions?
What did you neglect and what simplifications have you made?
What tools and methods did you use?
Why use these tools and methods?

4 Nifty Gadget results

Did you actually build it?
How can you test it?
How did you test it?
Why did you test it this way?
Are the results satisfactory?
Why should you (not) test it more?
What compensations had to be made to interpret the results?
Why did you succeed/fail?

5 Discussion

Are your results satisfactory?
Can they be improved?
Is there a need for improvement?
Are other approaches worth trying out?
Will some restriction be lifted?
Will you save the world with your Nifty Gadget?

6 References

What is the background reading list?

TETET

Guide to writing a thesis

Guide to Writing a Thesis — Page 3 of 4

Where is the related work?
Where is the prior work?
Where can I find important material?

Appendix A

Can you outline fatilary calculus or whatever complicated theory or results you are using that will obscure the text?

Appendix B

A thesis should discuss the following topics:

- **Introduction**

  Presentation of the problem or phenomenon to be addressed, the situation where the problem or phenomenon occurs, and references to earlier relevant research.

  Common errors
  Problem is not properly specified or formulated, insufficient references to earlier work.

- **Purpose**

  What can be gained by more knowledge about the problem or phenomenon.

  Common errors
  The purpose is not mentioned, not connected to earlier research, or not in line with what the actual contents of the thesis.

- **Problem/Hypothesis**

  Questions that need to be answered to reach the goal and/or hypothesis formulated be means of underlying theories.

  Common errors
  Missing problem description; deficiencies in the connections between questions; badly formulated hypothesis.

- **Method**

  Choice of an adequate method with respect to the purpose and problem/hypothesis.

  Common errors
  An inappropriate method is used, for example due to lack of knowledge about different methods; erroneous use of chosen method.

- **Result**

  Answers to the forwarded questions by means of the achieved results.

  Common errors
  The results are not properly connected to the problem; blurry presentation; the results are inter-

Guide to Writing a Thesis — Page 4 of 4

  mixed with discussion.

- **Discussion**

  Discussion of the accuracy and relevance of the results; comparison with other researchers results.

  Common errors
  Too far reaching conclusions; guesswork not supported by the data; introduction of a new problem and a discussion around this.

- **Conclusion**

  Consequences of the achieved results, for example for new research, theory and applications.

  Common errors
  The conclusions are too far reaching with respect to the achieved results; the conclusions do not correspond with the purpose.

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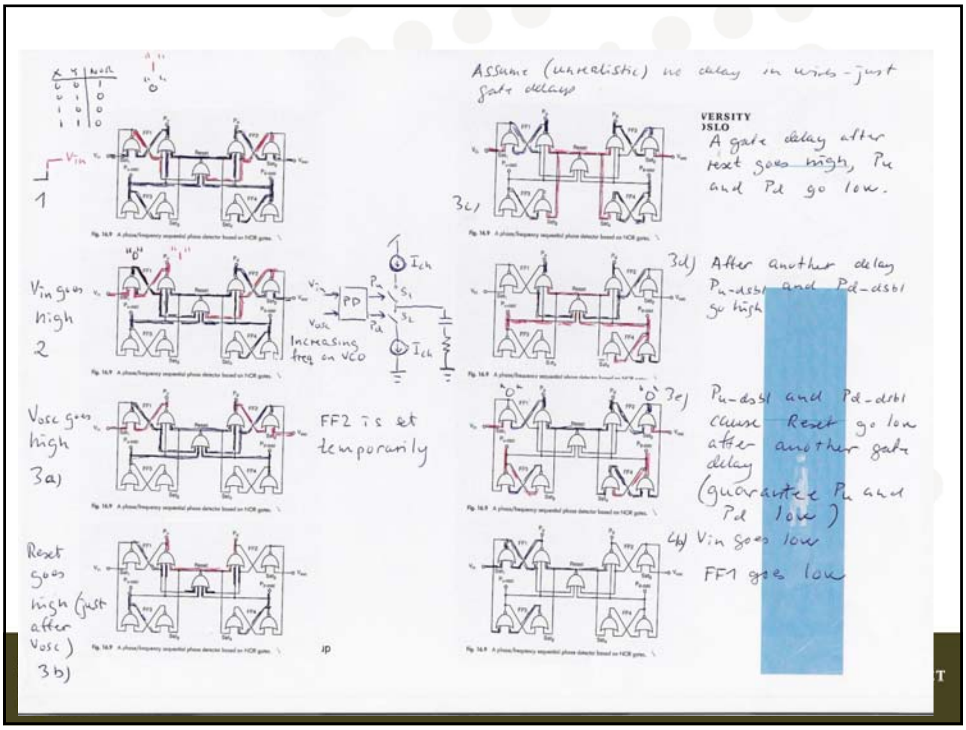
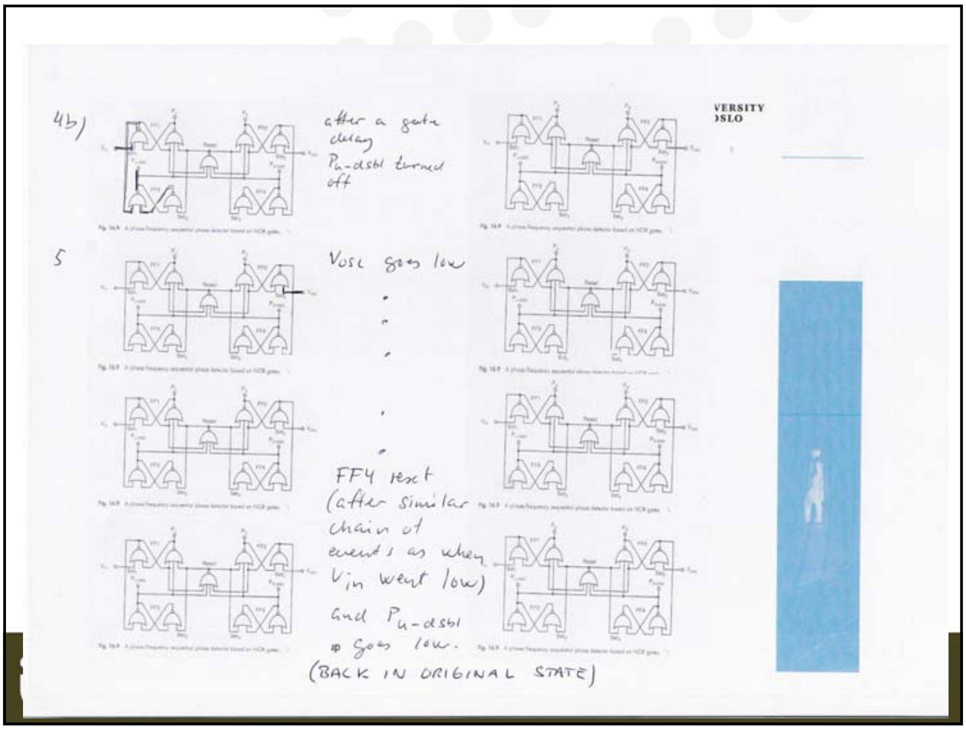
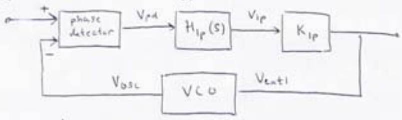

Assume (unrealistic) no delay in wires - just gate delays
1
Vin goes high
2
Vosc goes high
3a)
FF2 is set temporarily
Reset goes high (just after Vosc)
3b)
PD
Increasing freq on VCO
3c)
A gate delay after reset goes high, Pu and Pd go low.
3d) After another delay Pu-dsbl and Pd-dsbl go high
3e) Pu-dsbl and Pd-dsbl cause Reset go low after another gate delay (guarantee Pu and Pd low)
4a) Vin goes low
FF1 goes low


4b)
after a gate delay Pu-dsbl turned off
5
Vosc goes low
FF4 reset (after similar chain of events as when Vin went low) and Pu-dsbl goes low.
(BACK IN ORIGINAL STATE)

Ex. 16.2

Ex. 16.2



Assume the same conditions as in example 16.1. Design a LP-filter for the loop so that the loop time constant is approximately 10 periods at 10 MHz. $Q = \frac{1}{2}$

Equation 16.34: $K_{pll} = \sqrt{K_{pd} \cdot K_{lp} \cdot K_{osc}}$

$= \sqrt{0.1406 \frac{V}{rad} \cdot 1 \cdot 6.28 \cdot 10^7 \frac{rad}{Vs}}$

$= \sqrt{8829680 \left[\frac{1}{s}\right]} = 2972\ s^{-1/2}$

Having a loop-time constant of 100 periods:

$\omega_0 = \frac{1}{\tau_{pll}} = \frac{10^7}{100}\ s^{-1} = 10^5\ s^{-1}$

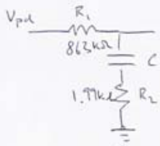
16.32: $\omega_0 = \frac{K_{pll}}{\sqrt{\tau_p}} \Leftrightarrow \tau_p = \left(\frac{K_{pll}}{\omega_0}\right)^2 = 0.883\ ms$

The pole is located at $f_p = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\tau_p}$

$= \frac{1}{2\pi \cdot 0{,}000883} = 180\ Hz$

16.33 $Q = \frac{\sqrt{\tau_p}}{\frac{1}{K_{pll}} + \tau_2 \cdot K_{pll}}$

$\tau_2 = \frac{\sqrt{\tau_p}}{Q K_{pll}} - \frac{1}{K_{pll}^2} = 19.87\ \mu s$



Choose $C_1 = 10nF$

$R_2 = \frac{\tau_2}{C_1} = \frac{19.89 \cdot 10^{-6} s}{10\ nF}$

$= 1.99k\Omega$

$R_1 = \frac{\tau_p}{C_1} - R_2 = \frac{0.883ms}{10nF} - 1.99\ k\Omega$

$88.3k - 1.99k = 86.3k\Omega$

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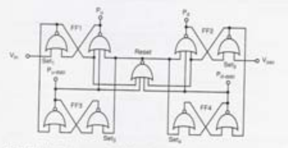


Fig. 16.9 A phase/frequency sequential phase detector based on NOR gates.

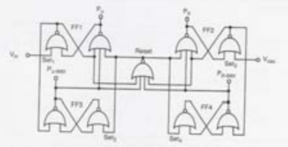
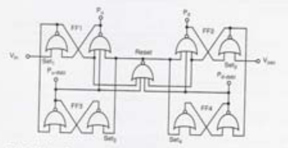


Fig. 16.9 A phase/frequency sequential phase detector based on NOR gates.



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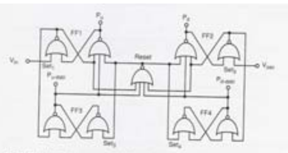

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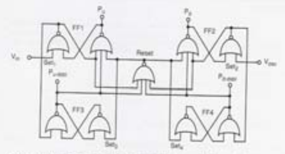

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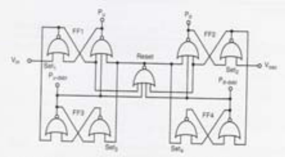

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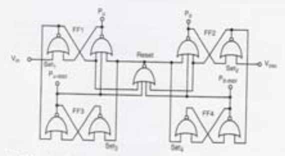

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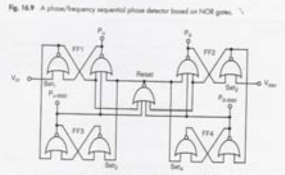

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