UNIVERSITY OF OSLO

Faculty of mathematics and natural sciences

Examination in INF9425 — Projects in analog/mixed-signal CMOS construction

Day of examination: 7. June 2012

Examination hours: 14:30 – 18:30

This problem set consists of 6 pages.

Appendices: None

Permitted aids: Any written material and approved calculator

Please make sure that your copy of the problem set is complete before you attempt to answer anything.

Contents

Problem 1 Oscillators and PLLs 20 %

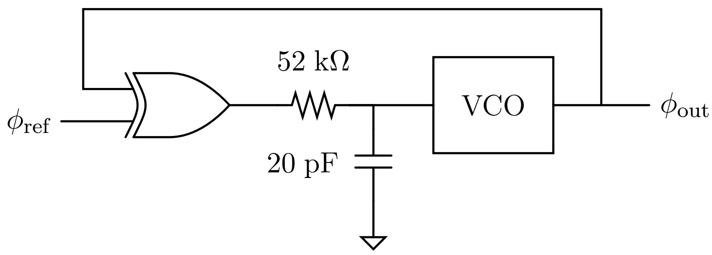

Figure 1: Type I PLL

1a Phase error 5 %

The PLL in figure 1 is a so called "type I PLL" with an XOR phase detector. The supply voltage is 1 V, the VCO has a center frequency of $f_0 = 1.9$ GHz and $K_{\text{VCO}} = 120\ \frac{\text{kHz}}{\text{V}}$. If the reference frequency is $f_{\text{ref}} = f_0 + 40$ kHz, what is the phase difference between the reference signal and the output signal assuming the PLL is in lock?

(Continued on page 2.)

1b Dynamic properties 5 %

What is the damping ratio, ζ, and the natural frequency, ω_n, in this case?

1c Lock range 5 %

Will the PLL be able to achieve lock in all cases? Why or why not?

1d Delay line 5 %

The VCO is reconfigured as a delay line for use in a DLL. Using the parameters from the previous problems, what is the nominal delay?

Problem 2 Switched capacitor circuits 25 %

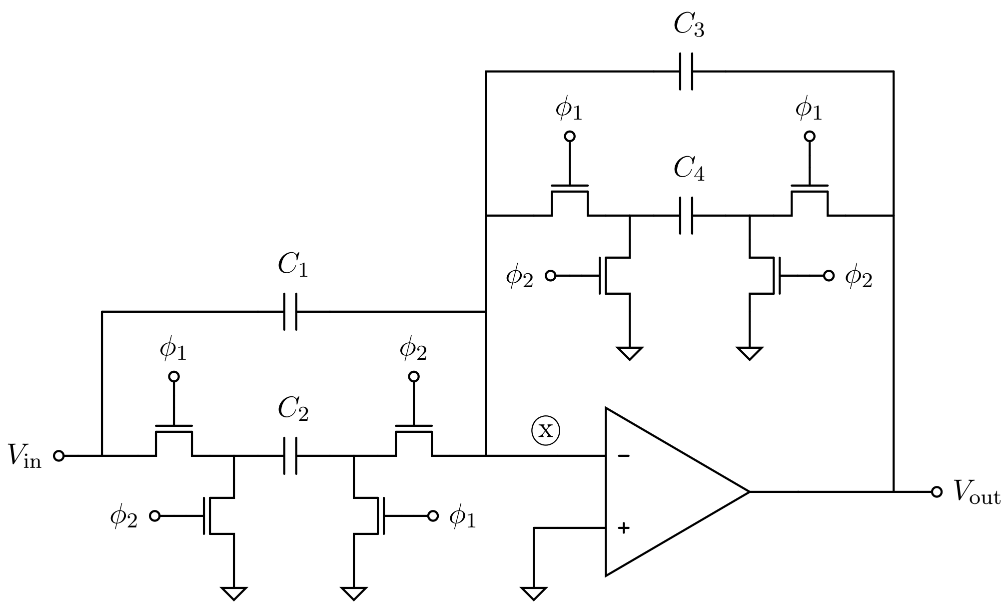

Figure 2: Switched capacitor circuit

All questions in this problem refer to the switched capacitor (SC) circuit in figure 2.

2a Continuous time equivalent 3 %

Draw a continuous time equivalent of this circuit.

2b Frequency response 8 %

Derive an expression for the frequency response given the following transfer function

$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = -\frac{C_1 - (C_1 + C_2)z^{-1}}{(C_4 + C_3) - C_4 z^{-1}}$$

(Continued on page 3.)

2c Large time constants 3 %

If large time constants are required for this circuit, is the SC or the continuous time circuit preferable in an integrated circuit application?

2d Precise time constants 3 %

If precisely defined time constants are required for the circuit, is the SC or the continuous time circuit preferable in an integrated circuit application?

2e Poly-poly capacitors 4 %

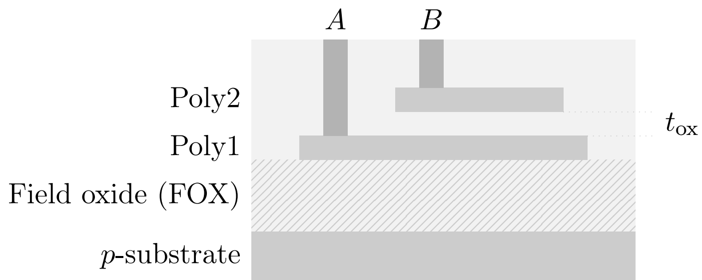

Figure 3: Poly-poly capacitor

The circuit is implemented in an older CMOS process where poly-poly capacitors (see figure 3) are available. Explain why the capacitor is not symmetric with respect to the terminals A and B. Which terminal would you connect towards node ⓧ in the SC circuit?

2f MoM capacitors 4 %

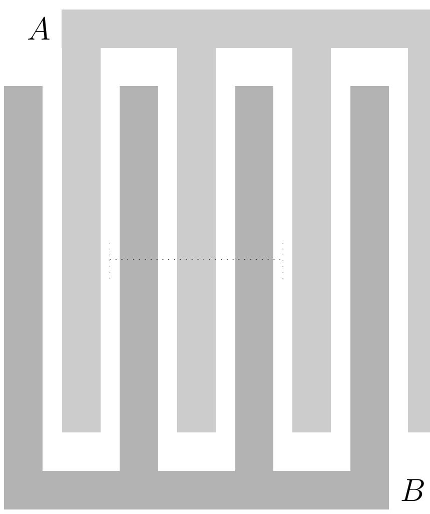

Figure 4: MoM top view

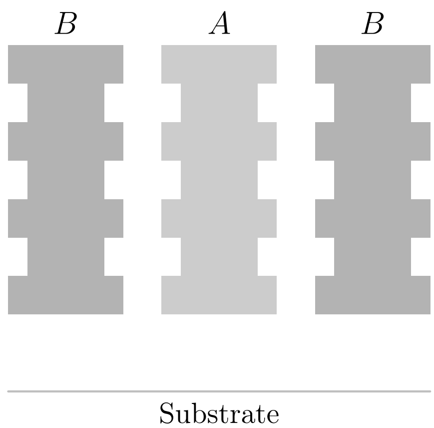

Figure 5: MoM side view

(Continued on page 4.)

If the circuit is implemented in a deep sub-micron (DSM) CMOS process, a metal-oxide-metal (MoM) capacitor (see figure 4 and 5) may be used instead. Explain how you can reduce the parasitic capacitance. What is the trade-off in this case?

Problem 3 Flash ADCs 25 %

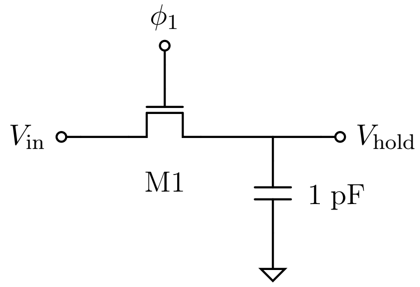

Figure 6: Track and hold (T/H) circuit

3a Track and hold 7 %

The track and hold (T/H) circuit of figure 6 is used as a front end in a flash ADC clocked at 200 MHz with a reference voltage of 1 V. If the settling error can be no larger than 4 mV, what is the highest value the "on" resistance, R_{on}, of M1 can have? (Ignore the body effect.)

3b Sizing 7 %

Assume the circuit is to be implemented in a 0.18 µm process with $\mu_n C_{\text{ox}} \approx 328.5 \, \frac{\mu\text{A}}{\text{V}^2}$ and $V_{\text{TH}} = 530$ mV. The supply voltage is $V_{\text{dd}} = 1.8$ V. These are nominal parameters, and you do not have to consider different PVT conditions. How would you choose the size of M1?

3c Resolution 4 %

What is the maximum attainable resolution of the converter if we require the settling error to be less than $\frac{1}{2}$ LSB?

3d Figure of Merit 3 %

If the converter uses 26 mW, what is the figure of merit (FoM)?

3e Time interleaving 4 %

If this converter needs to run at 800 MHz, can time interleaving be used to achieve this?

(Continued on page 5.)

Problem 4 Pipelined ADCs 20 %

4a Offset 7 %

The comparator in the first stage of this converter is implemented in a 0.18 µm process with $t_{\text{ox}} = 4$ nm. The input transistors are $W = 12$ µm and $L = 0.4$ µm. What is the standard deviation, σ, of the input referred offset voltage, V_{os}, if the threshold voltage is the most significant source of variability? (Use a reasonable value for A_{VTH} based on the information you have.)

4b Sizing 7 %

The desired resolution of the converter is 8 bit, and the reference voltage is 1.2 V. What is the required size of the input transistors if we only scale the width, and we want the worst case (3σ) V_{os} to be less than $\frac{1}{2}$ LSB?

4c Residue 6 %

Calculate the residue from each stage of a 5 bit pipelined ADC with a reference voltage of 1.2 V and 1 bit per stage when the input voltage is 340 mV. What is is the final digital output? Compare the digital output to the analog input voltage. Is the quantization error less than one LSB?

Problem 5 Current Steering DACs 10 %

5a Switch resistance, R_{on} 4 %

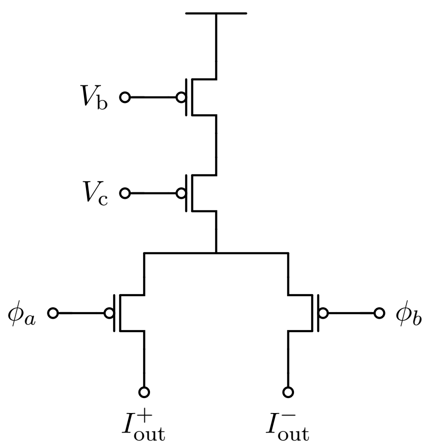

Figure 7: CS DAC unit

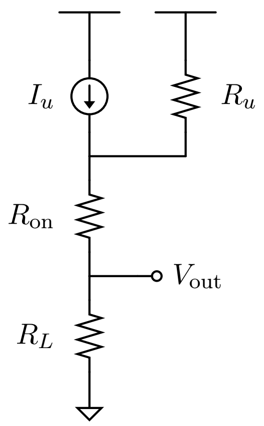

Figure 8: Equivalent circuit

Figure 7 shows one unit of a current steering (CS) DAC, and figure 8 is a simplified model of the same circuit (with an added load resistor). Assume

(Continued on page 6.)

that a high output resistance is required for a given linearity specification. Discuss why or why not the switch resistance, R_{on}, can be used to significantly contribute to the output resistance.

5b CMOS process configurations 6 %

According to [1], present and future CMOS process technology nodes come in different configurations suitable for different applications, such as low power (LP) and high performance (HP). Discuss how choosing a LP or HP process configuration impacts the CS DAC implementation.

References

[1] L.L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin. Analog Circuit Design in Nanoscale CMOS Technologies. *Proceedings of the IEEE*, 97(10):1687–1714, October 2009.