INF4420 Project Spring 2013

This project counts 40% towards your final grade. The workload is approximately 100 hours each for TWO persons. Always assume V_{DD} = 1.2V and T = 27°C, unless otherwise mentioned. You can skip the DRC errors on density and TSMC recommended rules. You are required to sign the NDA before accessing the PDK.

1. Introduction

You are working in an IC design company, and your team is now working on an ADC design using the TSMC 90 nm CMOS process. Your boss J is asking you to design a sample-and-hold circuit (S/H) shown in Fig 11.19 of the textbook. Your colleague K will design the amplifier, and you and your partner will finish the rest. K gave you a library (see the course webpage), and you can find an ideal amplifier there, you will use it through-out your design. Also, an ideal four-phase clock generator can be found in the library, you can use it before your clock generator design is finished.

1.1 S/H Design:

The following is the specification of the S/H:

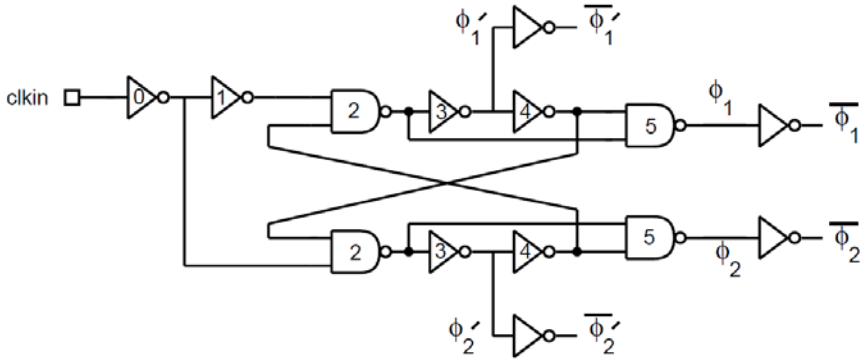
- Input signal bandwidth: 1 MHz
- Input swing: 300 mV_{pp}
- In-band attenuation: < 3 dB
- Input common mode voltage: 600 mV
- Dynamic range: > 8 bits
- Settling error: < 1 %
- Cload: 200 fF

Tasks to be completed:

1. Considering only the switching (kT/C) noise (i.e. ignore the noise of the amplifier), how large should be the sampling capacitor (C1) in order to achieve a SNR of 10 bits (i.e. ~62dB)? Discuss the choice of capacitor type.
2. Size the switches in order to get proper settling.
3. Where should AC ground be connected to?
4. Determine the ratio of C1 to C2 and the sampling frequency. State your design trade-offs clearly.
5. Finish the schematic.
6. Sweep the input frequency from 100kHz to 1MHz with a step size of 100kHz. What is the in-band attenuation? Discuss where the attenuation comes from.
7. Sweep the magnitude of the input signal with f_{in} = 100kHz. Estimate the dynamic range of your circuit.
8. Finish the layout and repeat tasks 6 and 7.
9. Compare the pre- and post-layout simulation results. If there is any difference, discuss and comment.

1.2 Four-phase Clock Generator Design.

You can use ONE ideal square wave generator. K recommends the structure shown in the figure below (more details can be found in [1]). It contains only NAND gates and inverters.



Tasks to be completed:

1. Change the parameters of the ideal clock generator so that you can get the clock signals you want before you finish your clock generator design.
2. Finish the schematic and layout.
3. Combine the S/H and Clock generator and do the top-level simulations.

1.3 Optional tasks

If you finish the tasks above early, you can do the following tasks.

1. Modify your design and the ideal amplifier model to a fully-differential structure and compare with the old structure.

2. The simulator offers analysis suitable for sampled data systems [2]. Simulate your design with periodic steady state (PSS) analysis, periodic noise (PNOISE), periodic AC (PAC), and other relevant analysis. Compare the results with results from the transient analysis.

3. The S/H can be modified to a digital-to-analog converter (DAC) (see [3]). Modify your design to a 3 bits DAC.

4. Design another S/H you can find in the literature and compare them. You can use the ideal amplifier model.

5. Help K to design the amplifier. He would suggest you to use single-stage folded-cascode structure. You can use ideal voltage or current sources for biasing.

IMPORTANT: You have to submit your S/H design first before you start doing the optional tasks. Approval from J is required.

2. Deadlines

**** Notice that the workload in this project is intended for groups consisting of two students!!! ****

You **HAVE** to meet the deadlines below.
Assignment 1: 15.2.2013
- Draw layout templates for the NAND gate and inverter used in the clock generator. They have to be DRC and LVS clean. Remember you may need to change the transistor size later in order to get the clocks signal you want.

Assignment 2: 15.3.2013
- Finish schematics of the S/H and clock generator and all pre-layout simulations.

Assignment 3: 19.04.2013
- Finish layouts of the S/H and clock generator and all pre-layout simulations.

Final report due 26.4.2013

3. Report requirements

The length of the report body (i.e. excluding index and appendix etc.) is limited to **10 pages** with font size of minimum 10, unimportant content should be put in the appendix. **Single column format**! The report may be written with the text editor of your choice, but it must be well organized and easy to read. All central aspects of the project must be supplied by relevant figures and plots. Plots of all the schematics and layout, with clearly visible parameters such as dimensions, must be included. References that you may have used in the project must also be included. All schematics and layouts must be made available for inspection, with the exact directory path specified in your final report. Everything must be clear from just reading the final report.

Some tips:
- Don't trust the simulators! Do some hand calculations, or at least predict the results before you do simulations. Simulations without any thinking will only give you doubts, not answers.
- Try to use top-down design approach.
- If you find problems on your layout, correct them as early as possible!
- Record all the reasons and statements to support your decisions. Trial and error approach will not make J happy. K will also be angry because you ruin his chance of promotion.
- Monte-Carlo and post-layout simulations are always time-demanding, be aware!

** Make sure you think thoroughly and carefully before you come to us.

References

[1] Andrew Masami Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," Ph.D. Dissertation, U.C. Berkeley, 1999.

[2] Ken Kundert, "Simulating Switched-Capacitor Filters with SpectreRF," Designer's Guide Consulting, Inc., July 2006.

[3] Ichiro Fujimori, Akihiko Nogi, and Tetsuro Sugimoto, "A Multibit Delta–Sigma Audio DAC with 120-dB Dynamic Range," *IEEE J. Solid-State Circuits* vol. 35, pp. 1066 - 1073, August 2000.