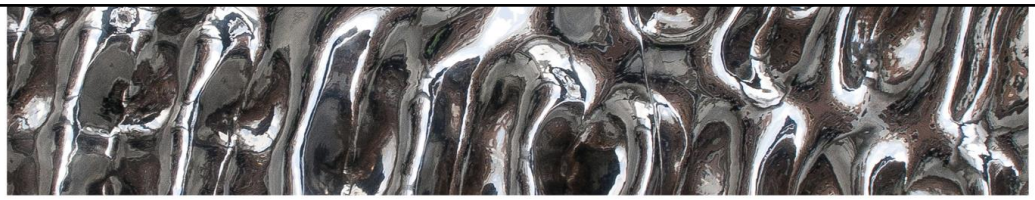

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INF4420

Sample and Hold

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Outline

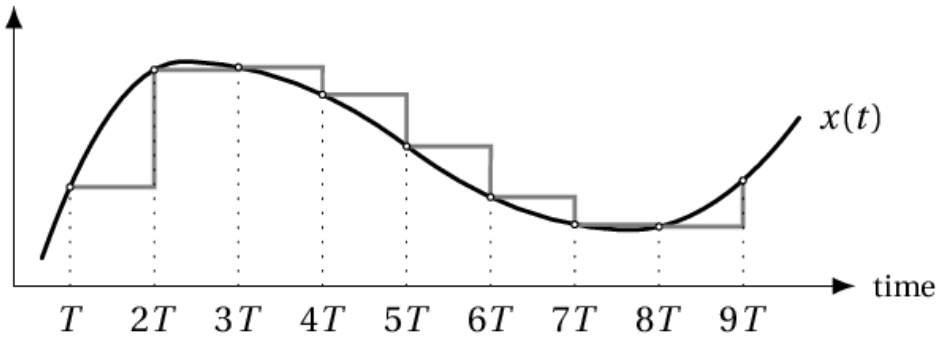
- Sample and hold basics
- Non-ideal behavior
- Sample and hold circuits

Introduction

- Take a “snapshot” of the input signal at an instant (sampling)
- Need “memory” to keep the signal value

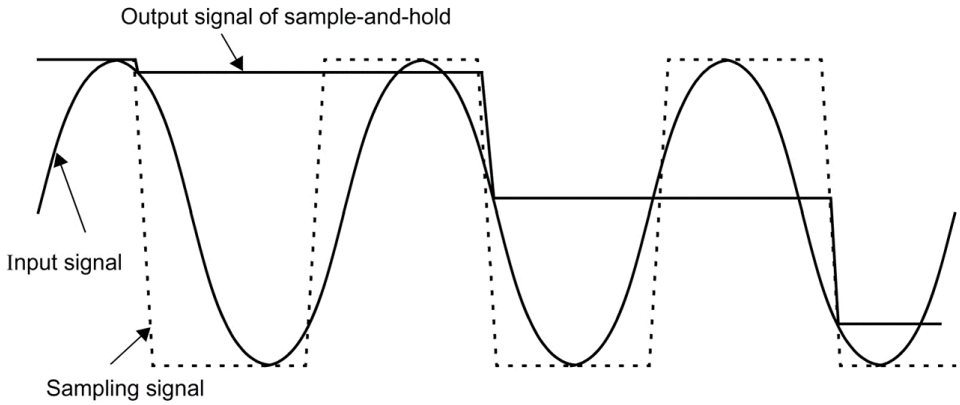
- We know how to store digital values (latches and flip-flops)
- Capacitor as a memory element

Introduction



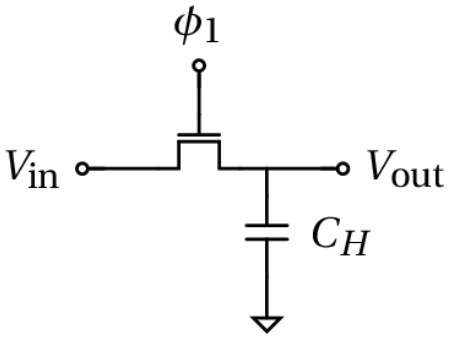
- Signal, *x(t)*, sampled at discrete time points, *nT*.

Introduction



Basic circuit

- Sample and hold vs. track and hold



Sample and hold

Typically used to hold the input constant while converting from analog to digital.

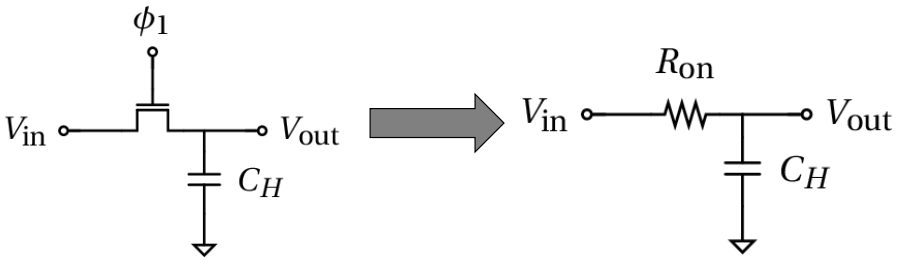
Limits performance, imperfections add directly to the input signal.

In a later lecture we will see how sampling affects the signal.

Non-ideal behaviour

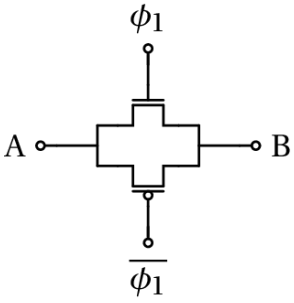
- Hold step (signal dependence)
- Coupling from output to sampled signal
- Finite speed
- Droop
- Aperture jitter
- Noise …

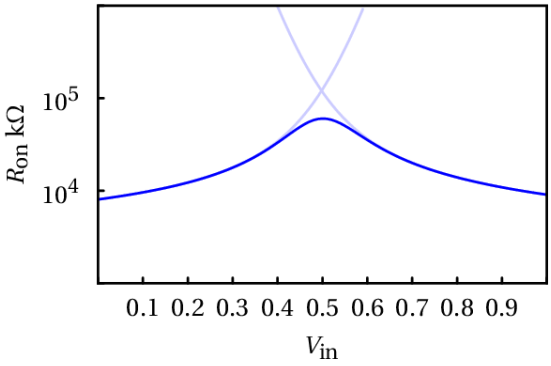
Finite speed



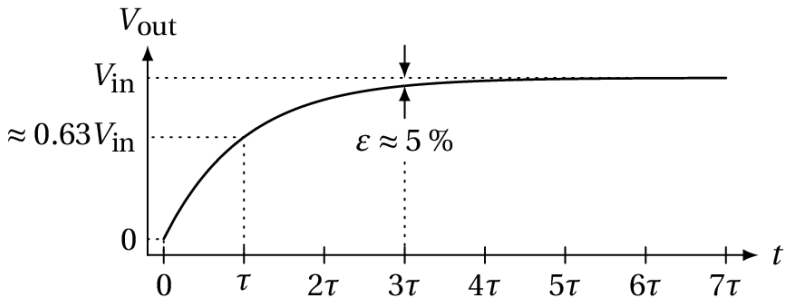
Finite speed

$$R = \frac{1}{\beta(V_{GS} - V_{tn})}$$





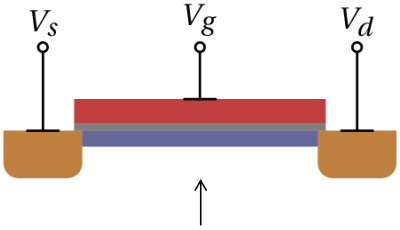
Settling time



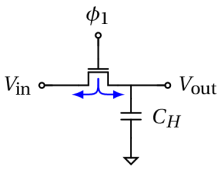
$$t_s = \tau \ln \frac{1}{\varepsilon}$$

Charge injection

- Switch transistor has *channel charge* when "on"
- Charge flows out of the channel when the transistor turns off
- Assume half the charge to source and half to drain. (Depends …)



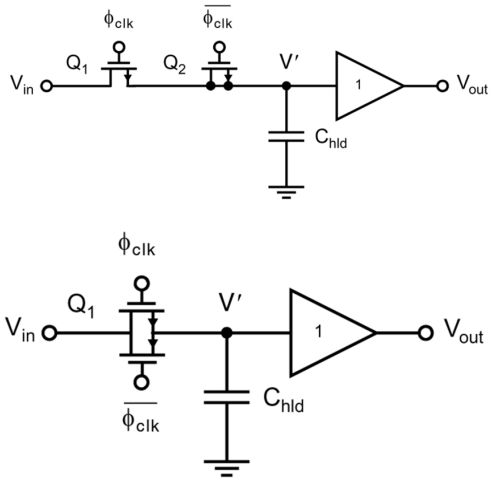
$$Q_{ch} = WLC_{ox}(V_{dd} - V_{in} - V_{TH})$$



$$\Delta V \approx \frac{Q_{ch}}{2C_H}$$

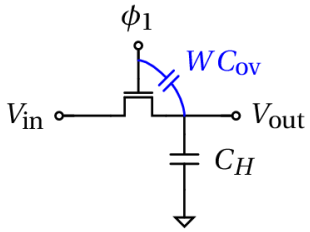
Charge injection

- Why is charge injection a problem?
- Depends on V_{in} and V_{th}.
- To make matters worse: V_{th} depends on V_{in}.
- Try to eliminate charge injection.

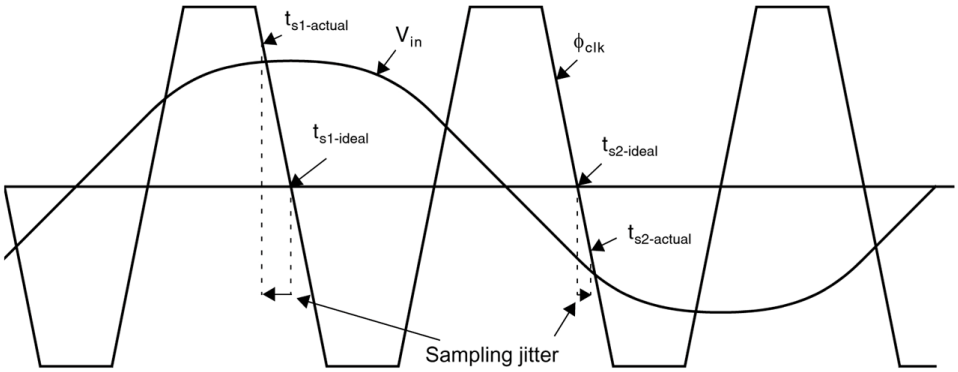


Clock feedthrough

- Overlap capacitance
- $\Delta V = -\frac{C_{\text{ox}} W L_{\text{ov}} V_{\text{dd}}}{C_H}$
- Constant, depends on clock voltage only
- Clock may have noise …



Jitter



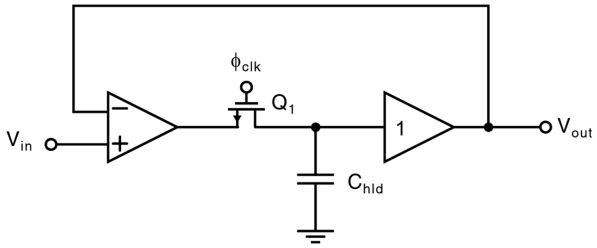
Closed loop S/H

Generic solution to mitigate non-ideal properties

⇒ Gain + Negative feedback

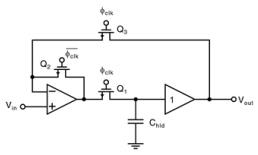
A better (?) S/H

- Switch configures circuit in two states. Analyze separately

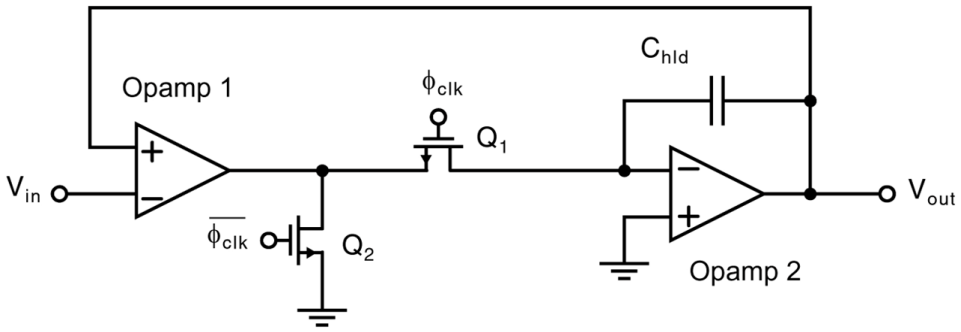


A better (?) S/H

- Eliminates non-linearity of output buffer +
- High input impedance +
- Open loop opamp when switch is open –
- Stability –
- Can add switches to make sure the opamp is closed loop when holding



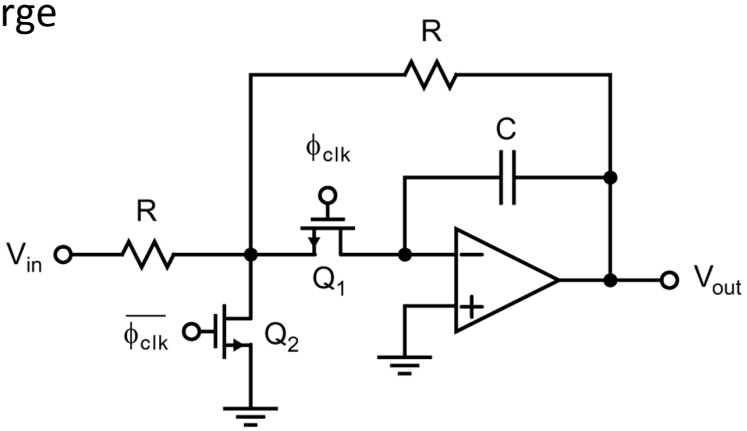
A better S/H



- No signal dependent charge injection +
- No signal dependent clock jitter +
- Stability (worse than before) –

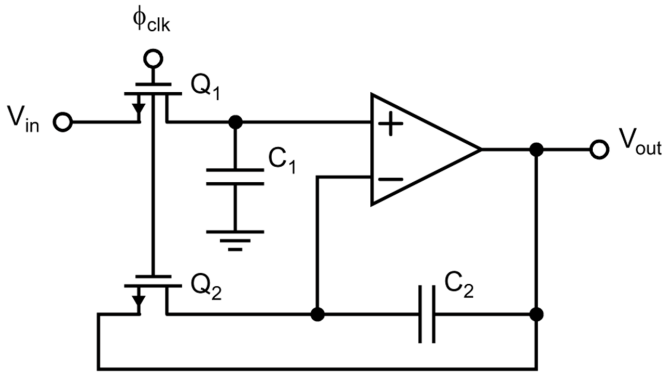
Inverting T/H

Lowpass in track mode and signal independent charge

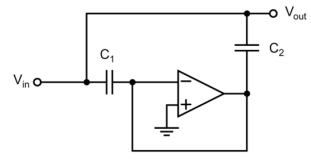


Non-inverting with cancelation

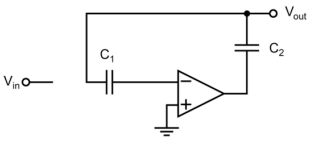
Charge injection from Q1 ≈ Q2.



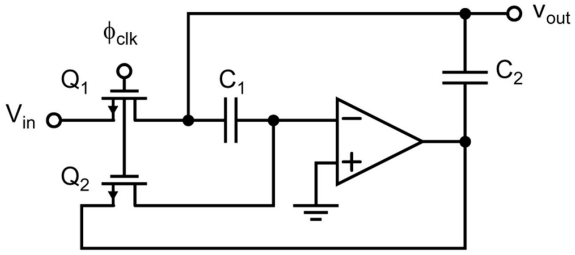
Miller hold capacitance



(a)



(b)

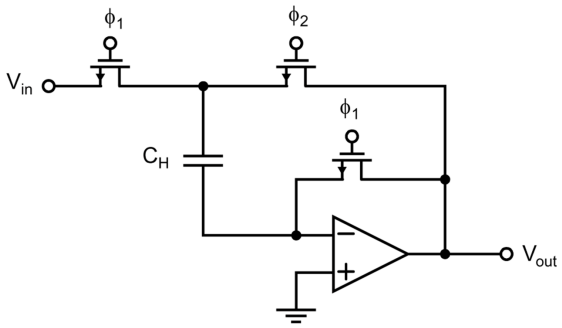


Tracking: $C_1 + C_2$

Holding: $(1 + A)\frac{C_1 C_2}{C_1 + C_2}$

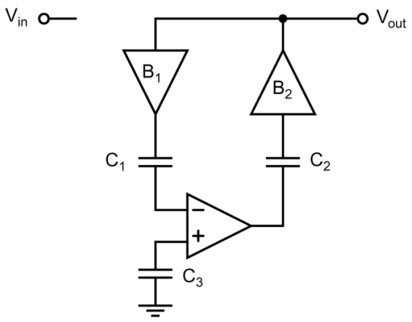
Switched capacitor (SC) S/H

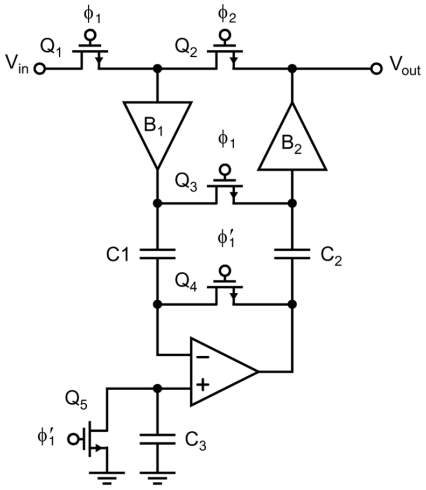
Two non-overlapping clock phases, ϕ_1 and ϕ_2.



Recycling S/H

Adds buffering

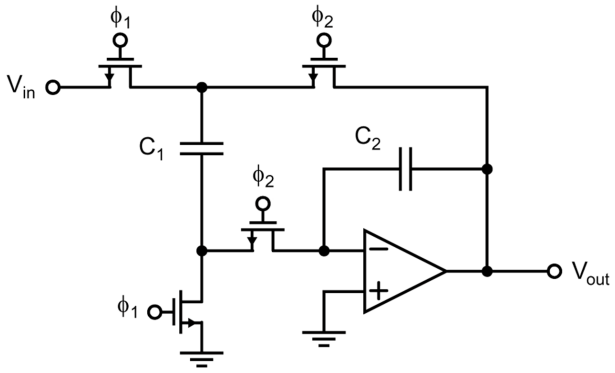




SC S/H with lowpass filtering

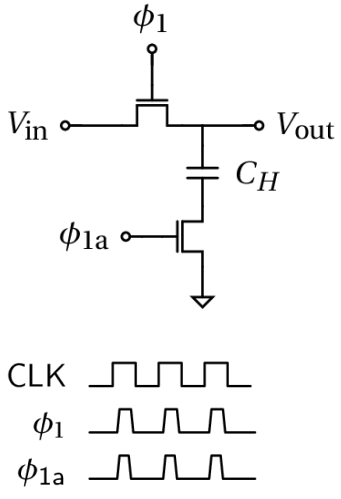
C_2 averages the charge from C_1.

$f_c = \frac{1}{2\pi}\frac{C_1}{C_2} f_{\text{clk}}$.

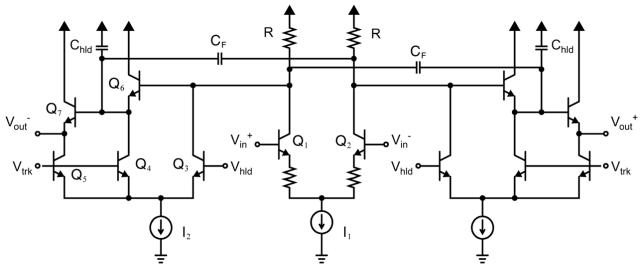


Bottom plate sampling

ϕ_{1a} turns off slightly before ϕ_1, injecting a constant charge. Signal dependent charge from ϕ_1 does not enter C_H because there is no path to ground.



High speed bipolar T/H



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A 40 Gs/s Time Interleaved ADC Using SiGe BiCMOS Technology

Michael Chu, *Member, IEEE*, Philip Jacob, *Student Member, IEEE*, Jin-Woo Kim, Mitchell R. LeRoy, *Associate Member, IEEE*, Russell P. Kraft, and John F. McDonald, *Senior Member, IEEE*

Fully differential sample and hold

- "Real" S/Hs are fully differential
- We can modify many of the S/H discussed today to become fully differential