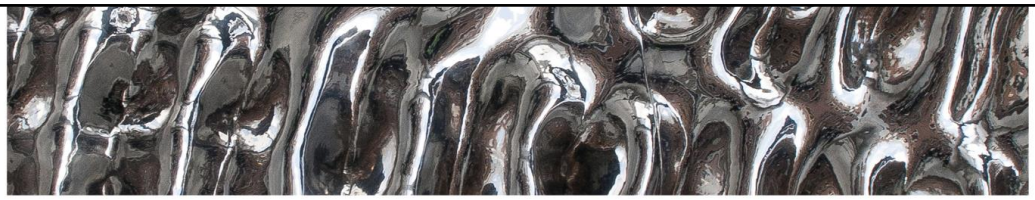

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Comparators

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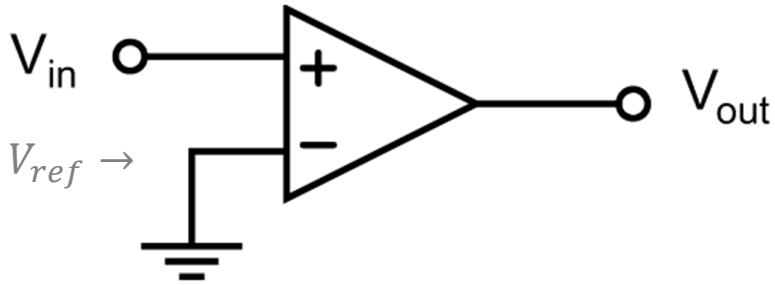
Outline

- Comparator limitations
- Latched comparators

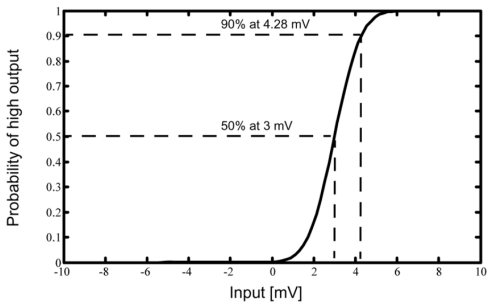
Introduction



- Important building blocks in ADCs (later)
- If $V_{in} > V_{ref}$: V_{out} is logic '1'
- If $V_{in} < V_{ref}$: V_{out} is logic '0'

Comparator performance

Non-ideal behavior limits performance.
→ Not a one-to-one mapping between input voltage and output, but a probability.

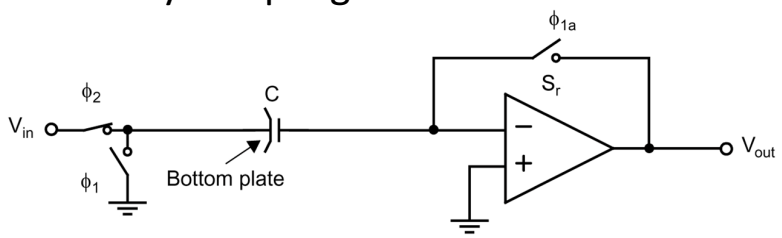


- Offset (mismatch)
- Noise
- Hysteresis ('0' → '0' and '1' → '1' more likely)

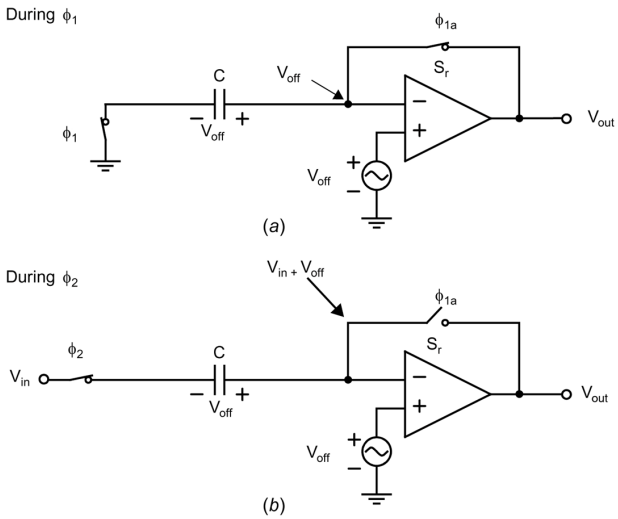
The opamp as a comparator

We already know how to make an opamp. Can we use it as a comparator?

The offset voltage is typically large, but we cancel the offset by sampling:



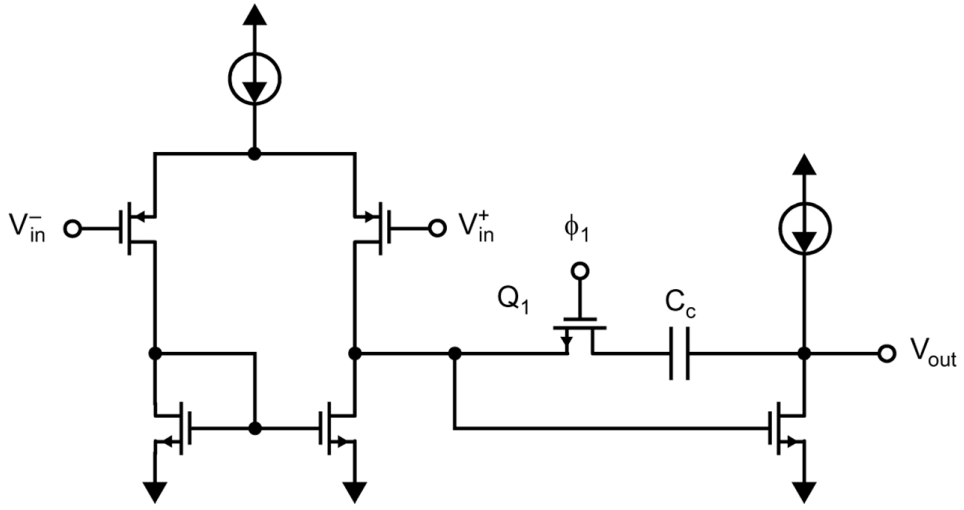
The opamp as a comparator



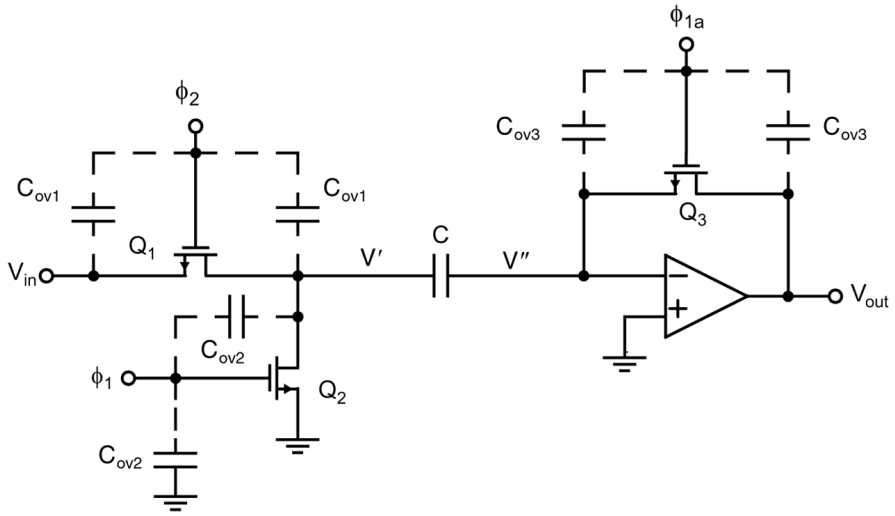
The opamp as a comparator

- A small difference in the input voltage is amplified and easily resolved to digital.
- The opamp has to be unity gain stable during ϕ_1 (compensation)
- Takes time to settle during ϕ_2
- Requires too much power to achieve sufficient speed.
- We can do better!

The opamp as a comparator

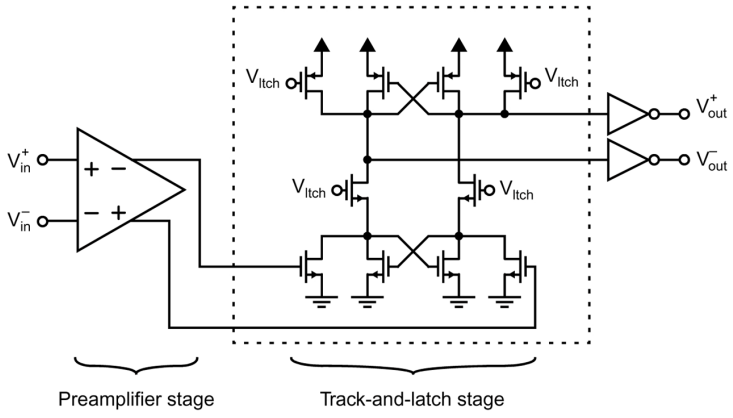


Charge injection and clock feedthrough



Latched comparators

- Low gain preamplifier and latch example



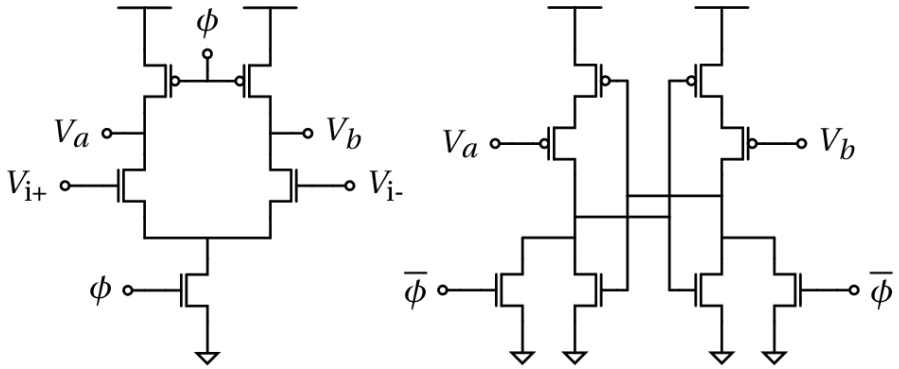
Latched comparators

- Reset phase when V_{ltch} is low, pulls the internal nodes high
- The reset ensures the latch starts from the same state regardless of the previous output (hysteresis)
- The latch uses positive feedback to resolve when V_{ltch} is high
- The pre-amplifier also serves to isolate the input from kickback noise due to the latch

Latched comparators

- If the voltage difference is too small, metastability occurs. The latch is not able to correctly resolve the input.
- Two halves of the latch are subject to mismatch (systematic and random)
- Possible to tune the offset. Program some voltage to compensate for the offset. However, we need to find an appropriate voltage to cancel the offset.

Latched comparator example



Van Elzakker, ISSCC, 2008