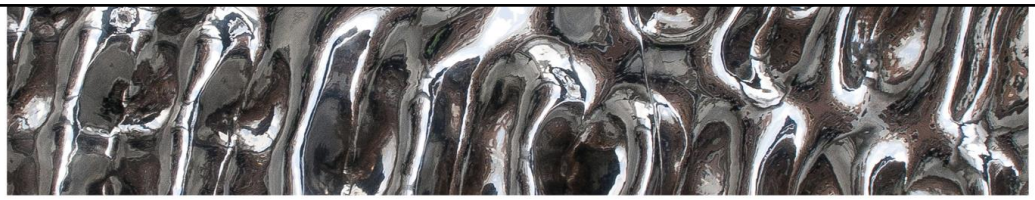

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INF4420

Analog to Digital Converters

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Outline

Overview of architectures for implementing analog to digital conversion

Introduction

ADCs are used in numerous applications with differing requirements on speed, accuracy, and energy efficiency.

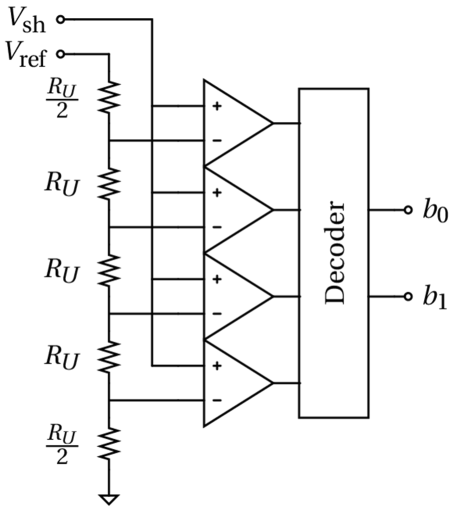
ADC architectures have different strengths and weaknesses with respect to these trade offs. It is therefore important to understand not only how each converter works, but also its limitations and key aspects for performance.

Numerous architectures

- Flash
- Interpolating
- Folding
- Interleaved
- Successive approximation
- Algorithmic
- Pipelined
- Two-step
- Integrating

Flash ADC

- The Kelvin divider is used to generate 2^N reference voltages
- Comparators compare the sample and held inputs to each derived reference voltage
- Thermometer output decoded to binary



Flash ADC considerations

- Fast: conversion is done in parallel
- Large number of comparators: power and area. Limits the practical number of bits.
- S&H output must drive all 2^N comparator inputs. Large capacitive load. Drives up power requirement for S&H. Must also be fast.
- Comparator input current results in errors in the derived reference voltages, “resistor-string bowing”

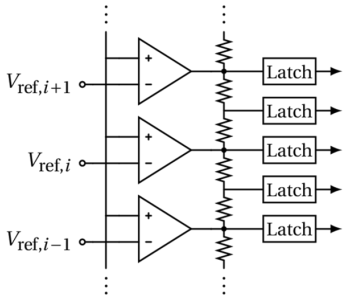
Flash ADC considerations

- Substrate and power supply noise: shielded (differential) clocks and separate analog supply to the comparator preamp. Bypass capacitors.
- Comparator errors such as metastability, noise, crosstalk, bandwidth, etc. cause “bubbles” in the thermometer code near the transition point. Thermometer decoder must take this into account.
- Comparator kickback noise.

Interpolating ADC

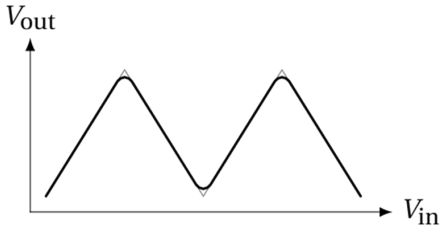
Similar to the flash ADC but comparator preamps are shared, and less derived reference voltages are needed. Less loading on the input.

Latches will see different delays. Can be compensated by adding resistance to laches close to the preamp.

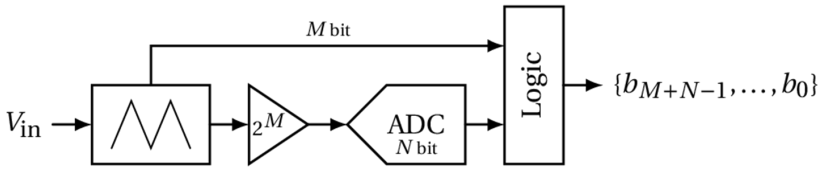


Folding ADC

Preprocess the input to compress the signal range and decide the MSBs. Often used with interpolating ADCs.



Difficult to implement the folding circuit.



Time-interleaved ADC

- Flash converters are fast (conversion in parallel)
- Still, there is a limit to how fast we can make the comparators
- Techniques considered so far have focused on how we can reduce hardware complexity (avoiding 2^N full comparators)
- We can make ADCs even faster by running multiple flash ADCs in parallel—time interleaved

Time-interleaved ADC

Example:

Monolithic 40 Gs/s ADC in an SiGe process

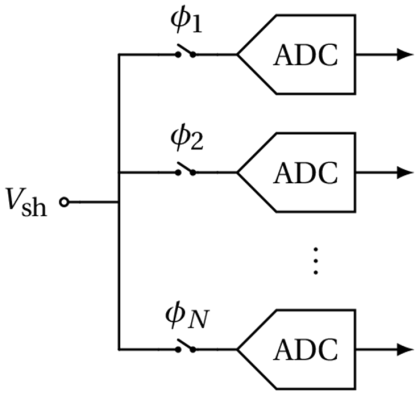
http://www.lecroy.com/tm/Library/WhitePapers/PDF/DBI_Explained.pdf

Time-interleaved ADC

Technique to increase the sampling rate by interleaving.

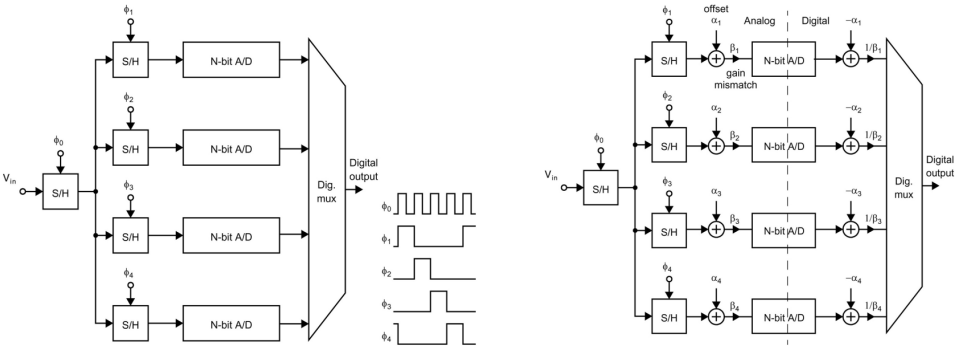
Run N ADCs in parallel. Requires fast S/H

Offset and gain mismatch between channels and clock misalignment



Time-interleaved ADC

Digital correction of gain and offset

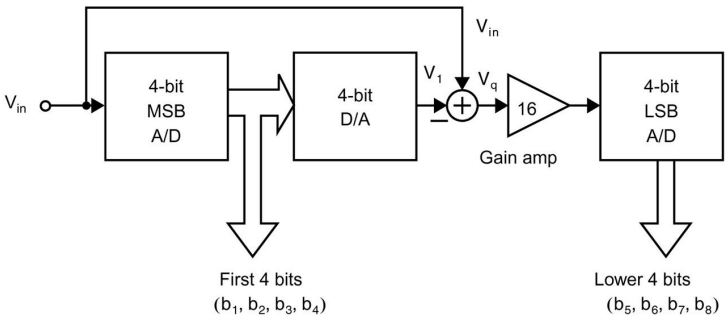


Two-step ADC

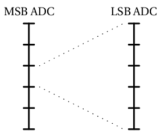
A system of two ADCs and one DAC. First ADC resolves the MSBs, M bits, and the second ADC resolves the LSBs, N bits. $2^N + 2^M$ comparators (if flash is used), rather than 2^{N+M}.

The MSB ADC must be accurate to $M + N$ bits.

Two-step ADC

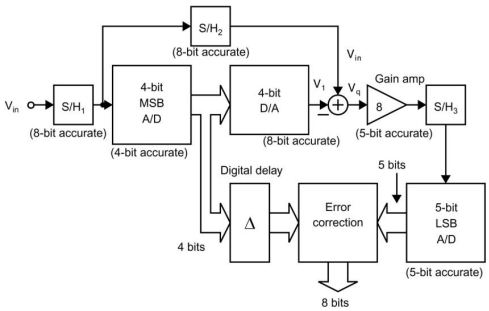


The residue is multiplied by 16 to scale it to a more practical range for the LSB ADC.



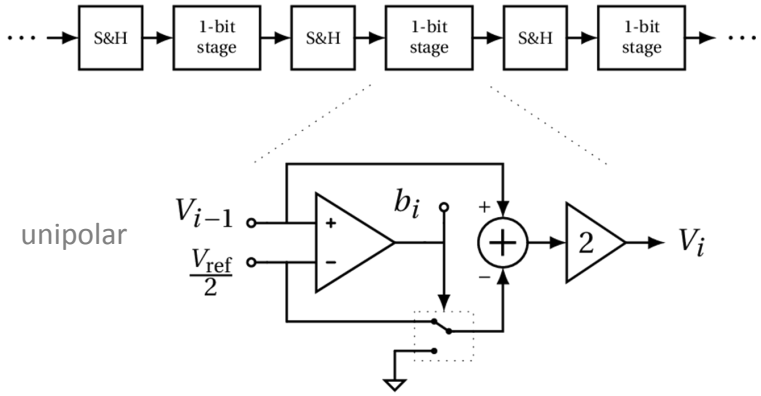
Two-step ADC error correction

Relax the accuracy requirement for the MSB ADC by overlapping the ranges of the ADCs.



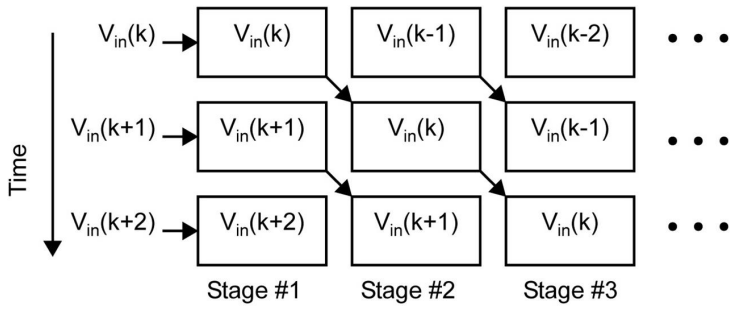
Pipelined ADC

Rather than using two ADC in sequence (two-step), we can use many.

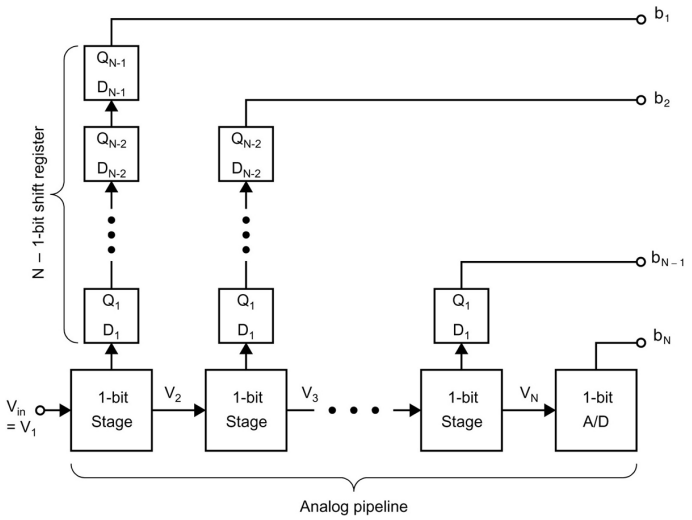


Pipelined ADC

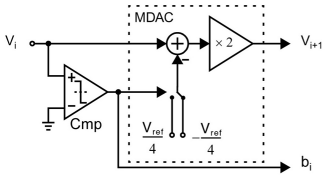
Outputs a sample every clock cycle but the *latency* is N (number of stages = number of bits assuming 1 bit per stage).

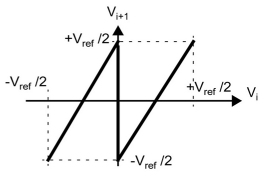


Pipelined ADC



Pipelined ADC





Error free			Offset in second stage (30 mV)		
	b_i	residue		b_i	residue
$V_1 = V_{in}$	1	-20 mV	$V_1 = V_{in}$	1	-20 mV
V_2	0	460 mV	V_2	1	-540 mV
V_3	1	420 mV	V_3	0	-580 mV

Bipolar input, $V_{in} = 240$ mV, $V_{ref} = 1$ V, three stages (3 bit)
Quantized output 187.5 mV vs 312.5 mV (error is 52.5 mV vs 72.5 mV)

Pipelined ADC

The signal is gained up by each stage → First stage must be the most accurate. Accuracy requirement relaxed by $\times 2$ (input referred)

We can relax the offset accuracy requirements by adding redundancy, two comparators per stage, 1.5 bit, rather than one. Need more logic to decode the output value

Pipelined ADC

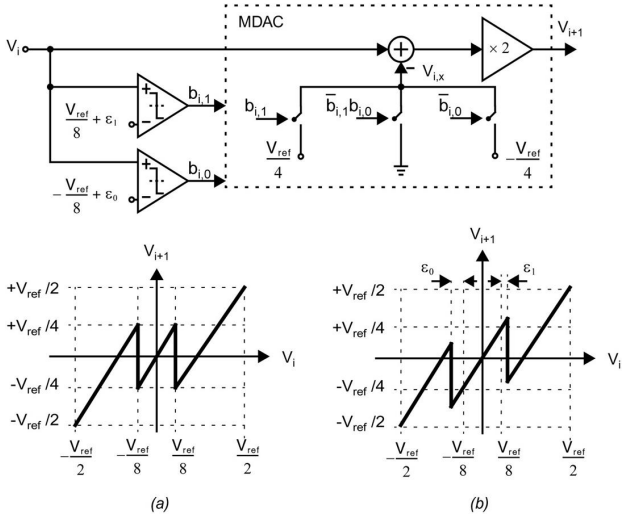
1.5 bit gives three possible output values from the DAC, $\left\{-\frac{V_{ref}}{4}, 0, \frac{V_{ref}}{4}\right\}$, rather than $\left\{-\frac{V_{ref}}{4}, \frac{V_{ref}}{4}\right\}$.
The two LSBs are determined by a 2 bit ADC. The final equivalent quantized input voltage is

$$\widehat{V_{in}} = \frac{V_{ref}}{2}\left(\sum_{i=1}^{N-2}(b_{i,1}+b_{i,0}-1)\cdot 2^{-i} + B_{N-1,1}\cdot 2^{N-2} + B_{N-1,0}\cdot 2^{N-1}\right)$$

Decoder must do this addition

Pipelined ADC

Random comparator offset, ε_0 and ε_1 is canceled if less than $V_{ref}/4$. Residue remains within $\pm V_{ref}/2$.



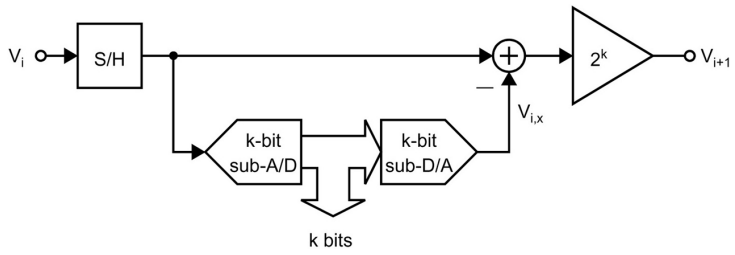
Pipelined ADC

Inaccuracy and noise in the DAC and gain circuit appear in the residue and is not canceled by the digital correction. Limits performance. Mismatch and noise in the first stage is most significant (more area, power).

Pipelined ADC

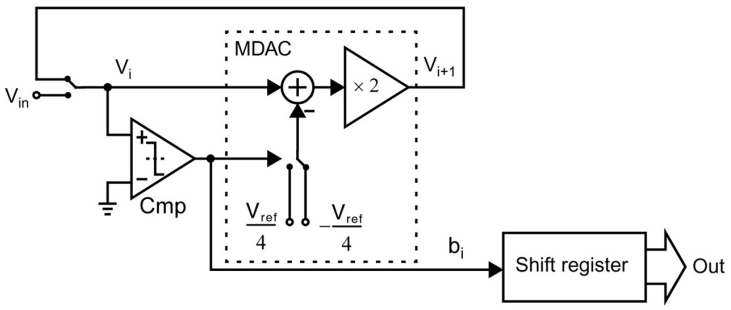
Generally, we can have k bit per stage. Two stages equivalent to a two-step ADC.

More bits per stage gives less latency



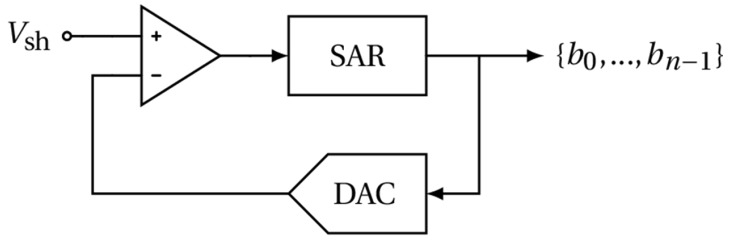
Algorithmic ADC

Instead of cascading multiple stages in hardware, like the pipelined ADC, the same stage can be reused. However, each conversion takes N clock cycles.



SAR ADC

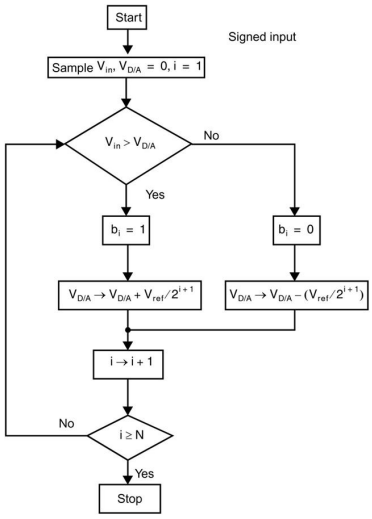
The successive approximation register (SAR) tests each bit sequentially (MSB first, one clock period per bit), and decides whether too keep the bit or not based on the comparator's output.



SAR ADC

Loop through N bits in N clock cycles. Binary search for the digital word (quantized representation) that is the closest match to the input voltage.

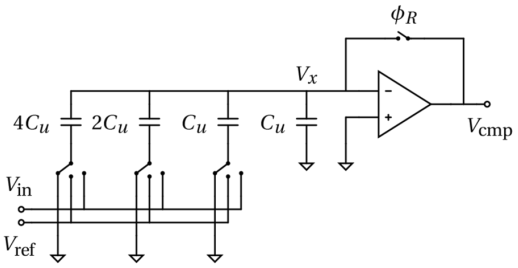
MSB determined first.



Charge redistribution SAR ADC

SAR ADCs are the most energy efficient ADCs (in terms of FoM).

Limited in resolution by capacitor matching (~ 10 bits).



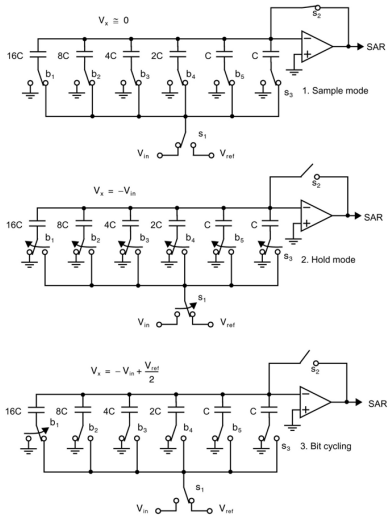
1. Sample mode
2. Hold mode
3. Bit cycling

- Inherent S/H function.
- Auto zero of the comparator is optional

Charge redistribution SAR ADC

No amplifiers needed (except for the comparator preamp). Saves power.

Comparator and charging of the capacitive array determines power consumption.

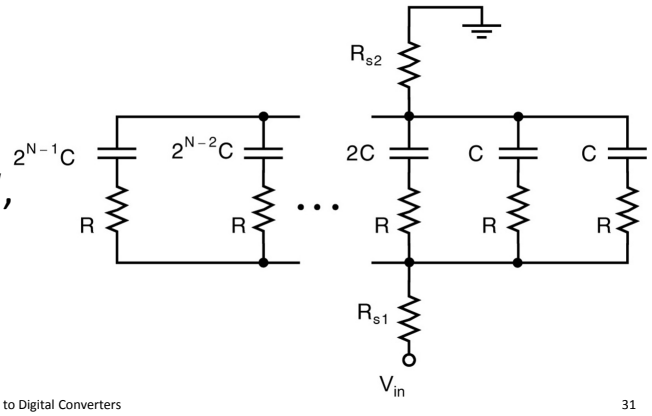


Charge redistribution SAR ADC speed

Speed limitation due to the RC time constant of the capacitor array and switches. $T > 0.69(N+1)\tau_{eq}$

τ_{eq} estimated from zero value time constant.

Charging time, T, assuming better than $^1/_2$ LSB.



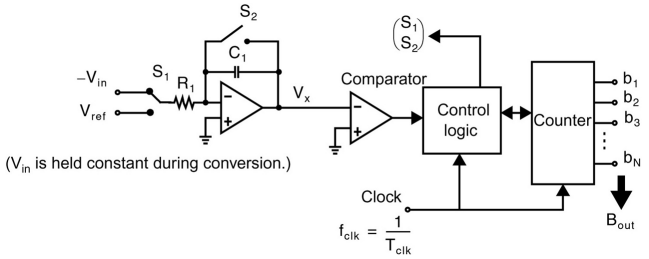
Charge redistribution SAR ADC

Error correction systems can be used to extend the resolution beyond the ~ 10 bit set by capacitor matching. Example in the textbook, fig. 17.11

We have considered SAR ADCs that determine one bit per clock cycle. To speed up, could consider converters that determine more than one bit per clock cycle.

Integrating ADC

High accuracy, but low speed.



Phase I: Integrate V_{in} for a fixed amount of time

Phase II: Measure the time it takes to discharge the integrator to zero with a fixed voltage

Integrating ADC

Phase I lasts for $T_1 = 2^N \cdot T_{clk}$, counter value when phase II completes is the digital output.

Output word does not depend on RC.