Exercises to inf5442_h14_8

Submit latest 1-Dec-2014

1. When a CMOS image sensors outputs pixel data, how does the receiver know which position in the array the pixel value corresponds to? What additional output signals from the sensor are used to help aligning the pixel position?
2. Draw up a timing diagram that illustrates the pixel output timing from a CMOS image sensor with DVP interface
3. Explain why two sensors capturing stereo pictures must stay time synchronized and how this is achieved?
4. What is a pull-up resistor? What purpose does such a circuit serve?
5. A sensor outputs uses 12b DVP output with 100MHz pixel clock. Load on output pins is 20pF. VDDIO=1.8V. Calculate worst case current spike during transition and explain how this can result in image noise. Calculate the average current assuming 50% toggling rate. Why is high power a concern? Can you suggest a method to reduce this power?
6. Why is the analog supply voltage higher than the digital supply in most CMOS image sensors?
7. Why is it important to keep the voltage supplies as low-noise as possible in CMOS image sensors?
8. Why is external I/O supply voltage (DOVDD or VDD_{IO}) typically separated from the internal digital supply voltage (DVDD)? Can the two values be different? If so, how is this handled inside the chip?
9. Explain how CMOS I/O pins are ESD protected.
10. What does “tri-state of I/O pins” mean? Why is this concept used?
11. List at least three reasons why the CMOS image sensor industry is starting to move away from parallel output and over to serial output.
12. Draw a conceptual diagram of LVDS sender/receiver and list the reasons why this has become such a popular industry standard
13. A CMOS sensor has 4+1 (4x data+ 1x clk) LVDS output lanes. Calculate the estimated power consumption.
14. Optional: Make a flow chart to describe an I2C read sequence.
15. Optional: Make a flow chart to describe an I2C write sequence.