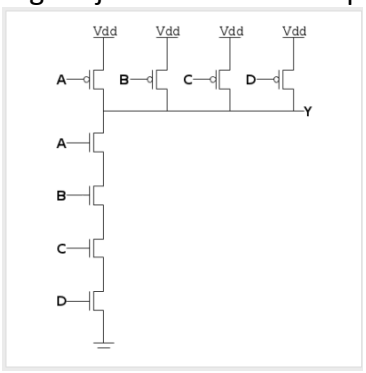
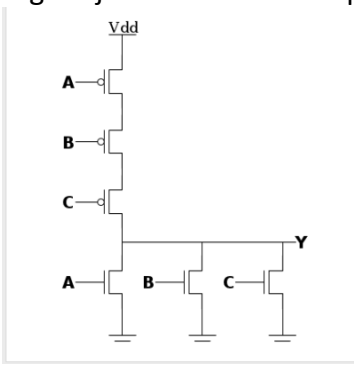
– CMOS

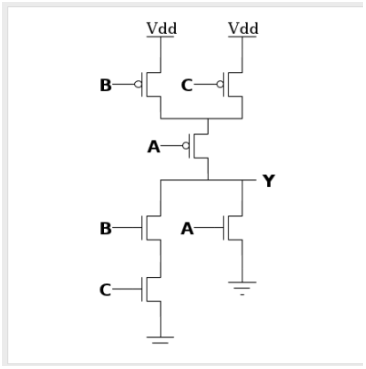
A. Tegn skjematikk for en 4 input NAND gate:



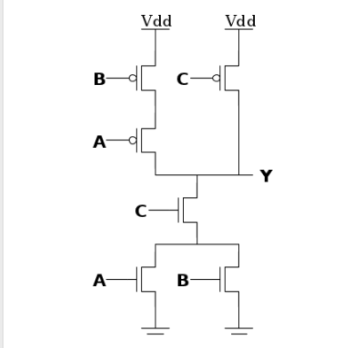
B. Tegn skjematikk for en 3 input NOR gate:



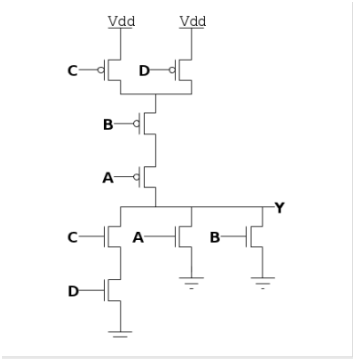
C. Tegn skjematikk for funksjonen Y = (A + (B*C))’



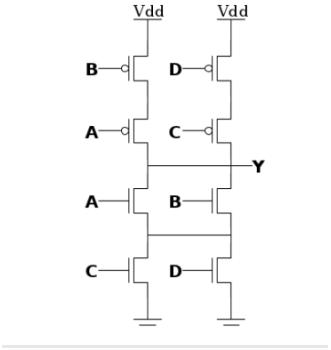
D. Tegn skjematikk for funksjonen Y = ((A*C) + (B*C))’



E. Tegn skjematikk for funksjonen Y = ((A + B) + (C*D))’



F. Tegn skjematikk for funksjonen Y = ((A + B)*(C + D))’



G. Tegn skjematikk for funksjonen Y = ((A*B)*(C*D) + E)’