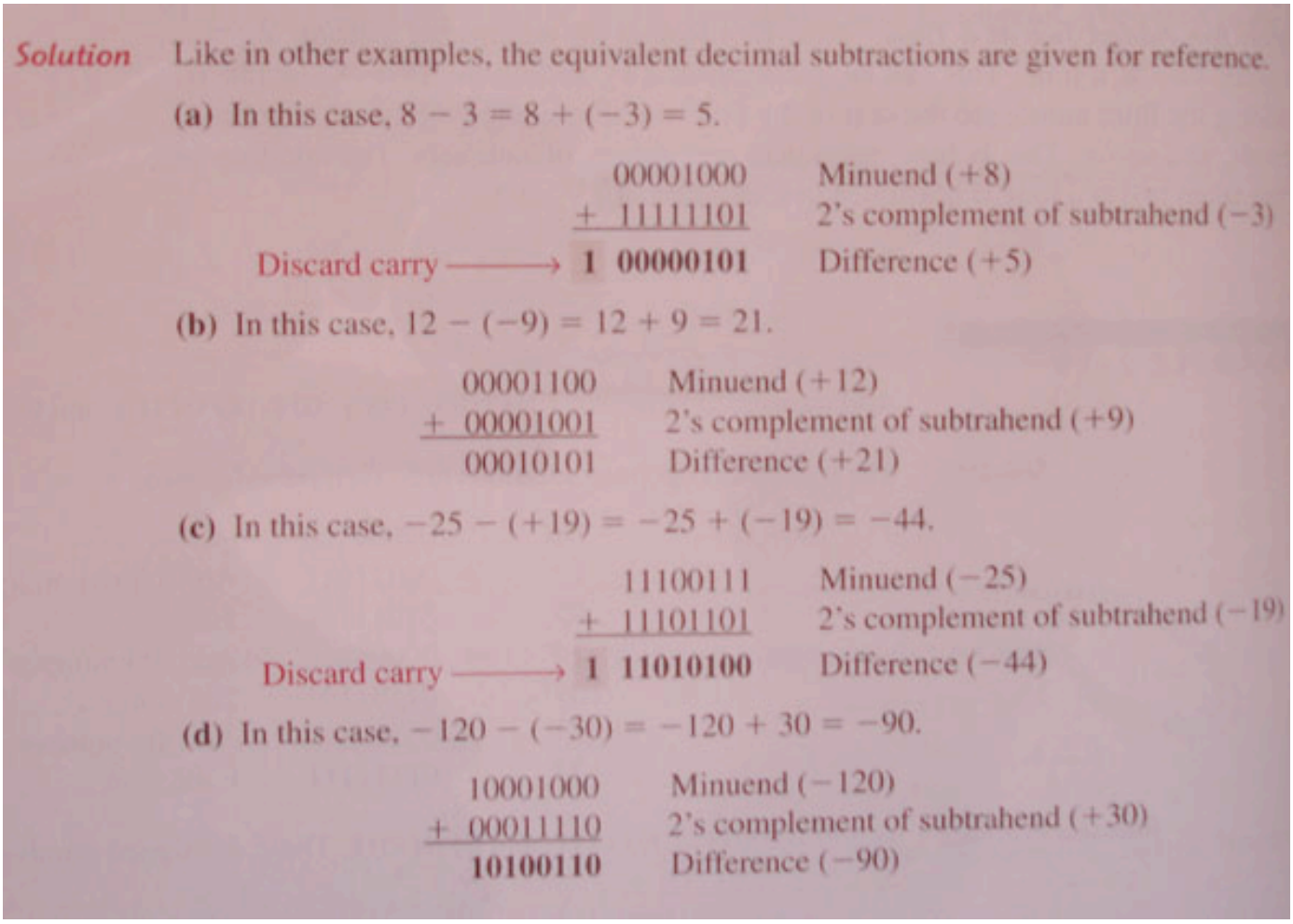
INF1400- Uke 04-FASIT

1. Regn ut følgende subtraksjon
    a. 00001000 – 00000011
    b. 00001100 – 11110111
    c. 11100111 – 00010011
    d. 10001000 – 11100010



Solution Like in other examples, the equivalent decimal subtractions are given for reference.

(a) In this case, $8 - 3 = 8 + (-3) = 5$.

00001000	Minuend (+8)
+ 11111101	2's complement of subtrahend (−3)
Discard carry ⟶ **1 00000101**	Difference (+5)

(b) In this case, $12 - (-9) = 12 + 9 = 21$.

00001100	Minuend (+12)
+ 00001001	2's complement of subtrahend (+9)
00010101	Difference (+21)

(c) In this case, $-25 - (+19) = -25 + (-19) = -44$.

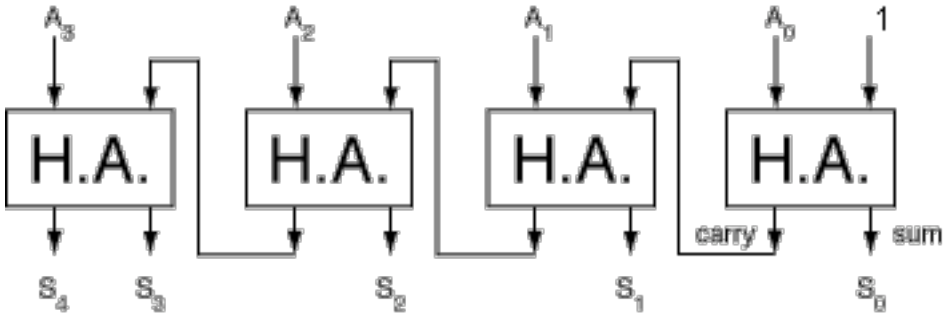
11100111	Minuend (−25)
+ 11101101	2's complement of subtrahend (−19)
Discard carry ⟶ **1 11010100**	Difference (−44)

(d) In this case, $-120 - (-30) = -120 + 30 = -90$.

10001000	Minuend (−120)
+ 00011110	2's complement of subtrahend (+30)
10100110	Difference (−90)

2. Design a combinational circuit that adds one to a 4-bit binary number. For example, if the input of the circuit is 1101, the output is 1110. (HINT! The circuit can be designed using four half-adders)

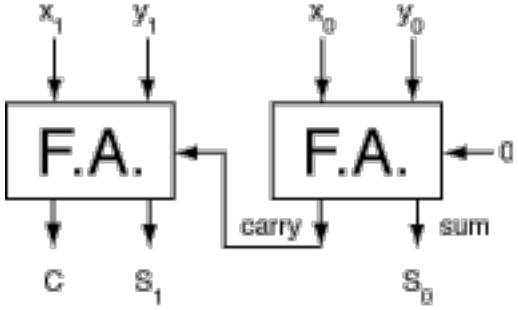
   Let A3A2A1A0 + 1 = S4S3S2S1S0



3. A combinational circuit produces the binary sum of two 2-bit numbers, x1x0 and y1y0. The outputs are C, S1, and S0. Provide a truth tableof the combinational circuit.

x_1	x_0	y_1	y_0	C	S_1	S_0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

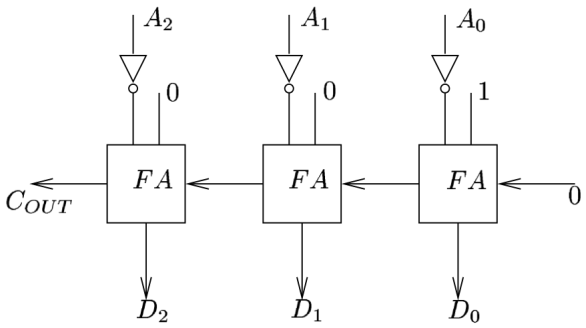
4. Design a circuit for the above problem using two full-adders.



5. (VANSKELIG) Consider the 3-bit, 2-complement conversion below and implement it using full-adders

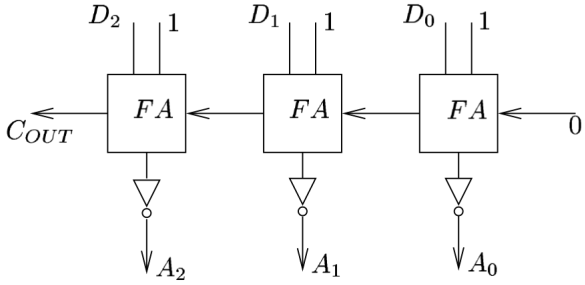
A_2	A_1	A_0	D_2	D_1	D_0
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

The 1-Complement is simply an inversion, while the addition of 1 can be done using full-adders, as seen in Figure 1.



6. Now implement the inverse operation, i.e. one that takes D2, D1, D0 and produces the output (A2,A1,A0). (HINT! Remember how to perform subtraction using 2-complements)

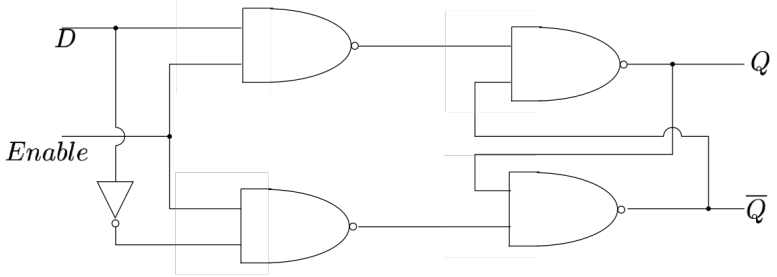
We note that the inverse operation is obtained by first subtracting 1, and then taking the 1-Complement. But, $(D_2, D_1, D_0) - (0, 0, 1)$ can be rewritten as $(D_2, D_1, D_0) + (1, 1, 1)$, since $(1, 1, 1)$ is the 2-Complement of $(0, 0, 1)$. The solution is shown in Figure 2.



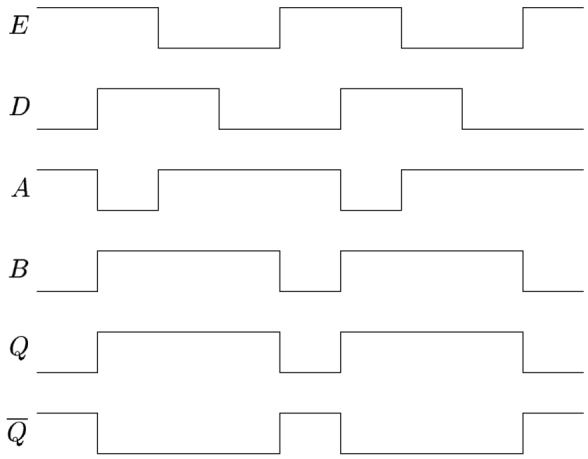
7. Regn ut alle oppgavene i slutten av kapittel 4.

SE FASIT I SLUTTEN AV BOKA

8. (UTFORDRING) Consider the network in the figure below
    a. Draw a timing-diagram that illustrates the behaviour of the network
    b. Is the network a transparant latch?



(a)



(b) From the timing diagram we see that when E = 1, Q follows D faithfully, while when E = 0, Q does not change. The system is thus a transparant latch.