Intel IA32 OS Support

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Areas of Support

- Kernel support
  - now
- Interrupt support
  - now
- Virtual memory support
  - MOS Chapter Four
- Cache support
- I/O support
  - MOS Chapter Five
- Multiprocessor support
  - MOS Chapter Eight

Kernel support

- Four privilege levels
- Privileged instructions
- Privileged registers
  - Flag register, EFLAG
    - Processor state indicator bits
  - Control registers
    - CR0 System control flags
    - CR2 Page fault linear address
    - CR3 Page directory base
    - CR4 Extensions
  - Instruction pointer register, EIP

Interrupt support

- Separate slides; for now at least

Virtual memory support

- Segmentation and paging
- Basic flat memory model
  - Contiguous unsegmented address space
  - Set up (at least) one code and one data segment that both map entire address space
- Protected flat memory model
  - As above except segment limits set to match physical memory present
- Multi segment model
  - Each process is given its own table of segment descriptors and its own segments
- Works intimately with privilege level and access control
- *Let's skip the grimy details for now*

Virtual memory support ii

- Segment registers contain segment selectors (14 bit)
- Segment selectors index into one of two (GDT/LDT) descriptor tables, containing segment descriptors
- Segment descriptors contain page directory base address and limit, ++

Cache support

- Cache policy set through CD and NW bits in CR3 (bits 4 and 3)
  - Write back
  - Write through
  - Cache disabled
- INVD, Invalidate internal caches
- WBINVD, Write back, and invalidate internal caches

I/O support

- Later

Multiprocessor support

- Lock
- BTS, Bit test and set
- BTR, Bit test and reset