Protection and System Calls

Otto J. Anshus

Recall the Protection Issues

- I/O protection
 - Prevent users from performing illegal I/O's
- · Memory protection
 - Prevent users from modifying kernel code and data structures
 - ...and each others code and data
- · CPU protection
 - Prevent a user from using the CPU for too long
 - Throughput of jobs, and response time to events (incl. user interactive response time)

Architecture Support: Privileged Mode

QuickTime™ and a TIFF (Uncompressed) decompressor are needed to see this picture.

Interrupts and Exceptions

- Interrupt sources
 - HW (from external devices)
 - SW: int n
- Exceptions
 - Program errors: faults, traps, aborts
 - SW generated: int 3
 - Machine-check exceptions
- See Intel doc Vol. 3 for details

Interrupts and Exceptions

QuickTimeTM and a TIFF (Uncompressed) decompressor are needed to see this picture.

Interrupts and Exceptions

QuickTime™ and a TIFF (Uncompressed) decompresse are needed to see this picture.

Privileged Instruction Examples

- · Memory address mapping
- Cache flush or invalidation
- Invalidating TLB entries
- · Loading and reading system registers
- Changing processor mode from kernel to user
- Changing the voltage and frequency of the processor
- · Halting a processor
- I/O operations

Instruction	Description	Useful to Application?	Protected from Application?
LLDT	Load LDT Register	No	Yes
SLDT	Store LDT Register	No	No
LGDT	Load GDT Register	No	Yes
SGDT	Store GDT Register	No	No
LTR	Load Task Register	No	Yes
STR	Store Task Register	No	No
LIDT	Load IDT Register	No	Yes
SIDT	Store IDT Register	No	No
MOV CRn	Load and store control registers	Yes	Yes (load only)
SMSW	Store MSW	Yes	No
LMSW	Load MSW	No	Yes
CLTS	Clear TS flag in CR0	No	Yes
ARPL	Adjust RPL	Yes¹	No
LAR	Load Access Rights	Yes	No
LSL	Load Segment Limit	Yes	No

Instruction	Description	Useful to Application?	Protected from Application?
VERR	Verify for Reading	Yes	No
VERW	Verify for Writing	Yes	No
MOV DBn	Load and store debug registers	No	Yes
INVD	Invalidate cache, no writeback	No	Yes
WBINVD	Invalidate cache, with writeback	No	Yes
INVLPG	Invalidate TLB entry	No	Yes
HLT	Halt Processor	No	Yes
LOCK (Prefix)	Bus Lock	Yes	No
RSM	Return from system management mode	No	Yes
RDMSR ³	Read Model-Specific Registers	No	Yes
WRMSR ³	Write Model-Specific Registers	No	Yes
RDPMC ⁴	Read Performance-Monitoring Counter	Yes	Yes ⁹
RDTSC ³	Read Time-Stamp Counter	Yes	Yes

IA32 Protection Rings

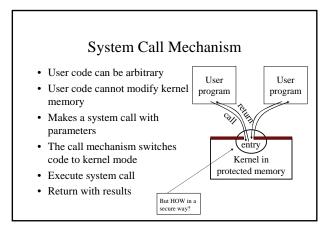
2^16=0-FFFFh 8-bit ports 2*8=16 bit port 4*16=32 bit port I/O • I/O ports: · created in system HW for com. w/peripheral devices • Examples - connects to a serial device - connects to control registers of a disk controller • I/O address space Will look at this and memory mapped I/O later • I/O instructions - in, out: between ports and registers - ins, outs: between ports and memory locations I/O protection mechanism VO Privilege Level (IOPL): I/O instr. only from Ring Level 0 or 1 (typical) VO permission bit map: Gives selective control of individual

System Calls

- Operating System API
 - Interface between a process and OS kernel
- Categories
 - Process management
 - Memory management
 - File management
 - Device management
 - Communication

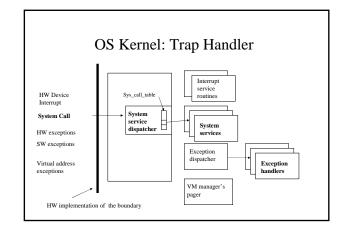
System Calls

- · Process management
 - end, abort, load, execute, create, terminate, set, wait
- Memory management
 - mmap & munmap, mprotect, mremap, msync, swapon & off,
- File management
 - create, delete, open, close, R, W, seek
- Device management
 - res, rel, R, W, seek, get & set atrib., mount, unmount
- Communication
 - get ID's, open, close, send, receive



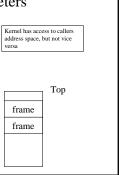
System Call Implementation

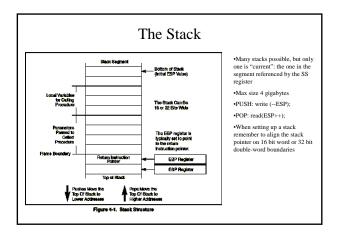
- Use an "interrupt"
 - Hardware devices (keyboard, serial port, timer, disk,...) and **software** can request service using interrupts
 - The CPU is interrupted
 - · ...and a service handler routine is run
 - ...when finished the CPU resumes from where it was interrupted (or somewhere else determined by the OS kernel)

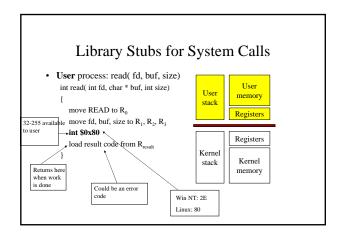


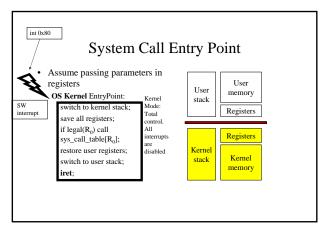
Passing Parameters

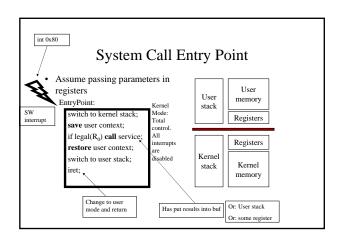
- · Pass by registers
 - Simple, but limited
 - #registers
 - #usable registers
 - #parameters in syscall
- Pass by memory vector
- A register holds the address of a location in users memory
- · Pass by stack
 - Push: done by library
 - Pop: done by Kernel

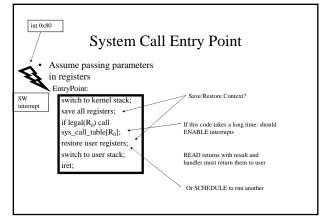












Polling instead of Interrupt?

- · OS kernel could check a request queue instead of using an interrupt?
 - · Waste CPU cycles checking
 - All have to wait while the checks are being done
 - · When to check?
 - Non-predictable
 - Pulse every 10-100ms?
 - » too long time

But used for Servers

- · Same valid for HW Interrupts vs. Polling
- However, spinning can give good performance (more later)

Design Issues for Syscall

- · We used only one result reg, what if more results?
- In kernel and in called service: Use caller's stack or a special stack?
 - Use a special stack
- · Quality assurance
 - Use a single entry or multiple entries?
 - · Simple is good?
 - Then a single entry is simpler, easier to make robust
- · Can kernel code call system calls?
 - Yes, but should avoid the entry point mechanism

System calls vs. Library calls

- Division of labor (a.k.a. Separation of Concerns)
- Memory management example
 - Kernel
 - Allocates "pages" (w/HW protection)
 Allocates many "pages" to library
 Big chunks, no "small" allocations
 - Library

 - Provides malloc/free for allocation and deallocation of memory
 Application use malloc/free to manage its own memory at fine granularity
 When no more memory, library asks kernel for a new chunk of pages

User process vs. kernel

- User process -> kernel
 - syscalls
- Kernel -> user process
 - Kernel is all powerful
 - Can write into user memory
 - Can terminate, block and activate user processes