

INF5490 RF MEMS

LN02: MEMS – Fabrication

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Today's lecture

- Micromachining
- Important process steps
 - General
 - Summary: MEMS-specific steps
- Examples of processes
 - MultiMEMS
 - polyMUMPs

MEMS for RF?

- MEMS technology is **attractive for RF** due to
 - Miniaturization: small dimensions ($\sim\mu\text{m}$)
 - Batch processing: parallel processing
 - Many units at low cost
 - Good qualities – high performance
 - High Q, low loss, reduced parasitics
 - Low power consumption
 - Making integrated systems possible
- Essential: **MICROMACHINING!**

Micromachining

- Micromachining, definition:
 - *Accurately, to **define and implement** any microscopic mechanical structure **out of or on** a material*
- **Silicon micromachining is mature**
 - Si processes also used by IC industry
 - "grown out of" IC-processing
 - New *specific* MEMS processes also developed
 - A lot of variants, - **few standards!**

What is needed?

- A proper **substrate**
 - Si, SOI, glass (PSG), quarts
- Methods to
 - **Define** geometries (pattern)
 - **Modify** material properties
 - **Remove** material
 - **Add** new material
 - **Bonding** wafers together

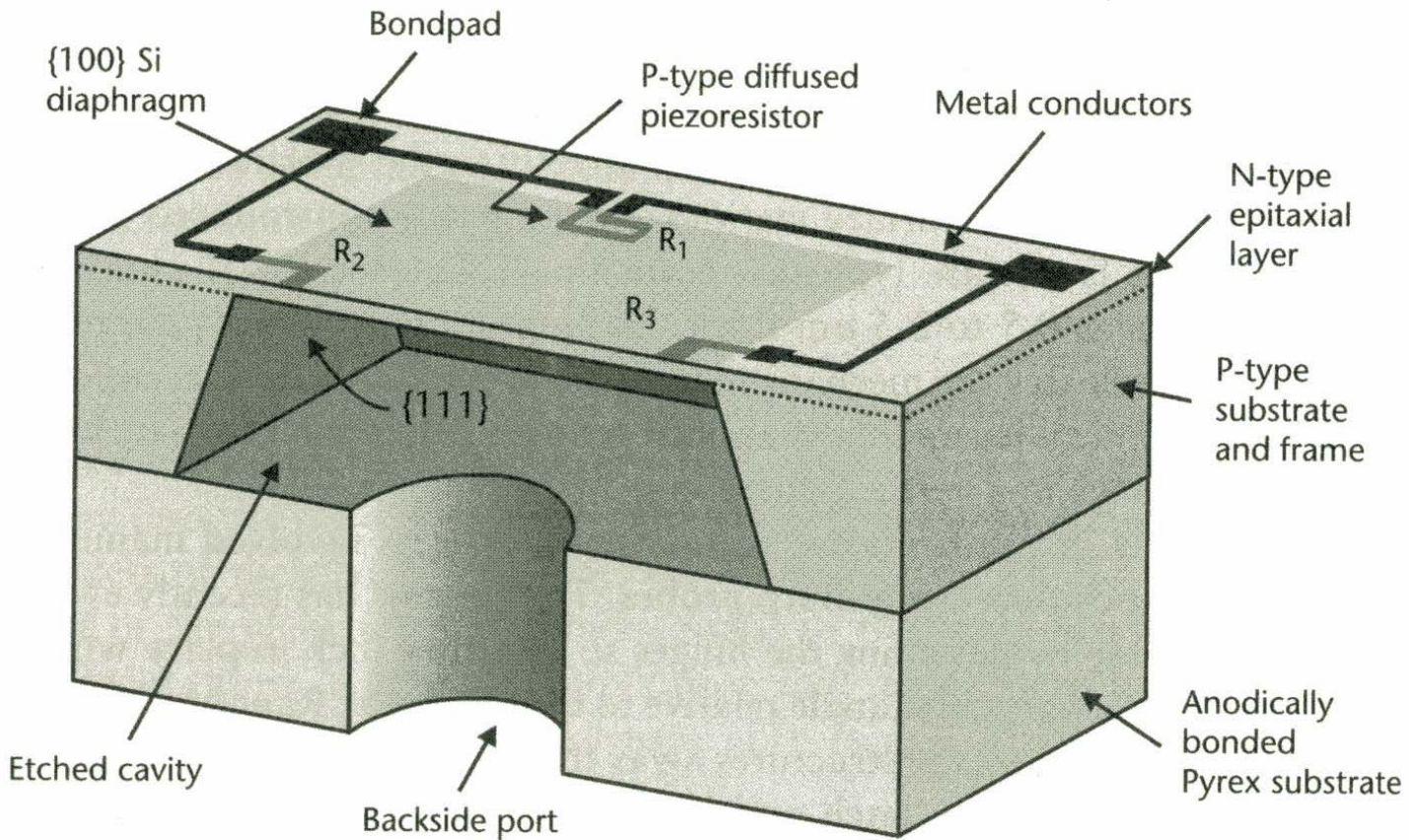
2 main methods

- **”Bulk”** micromachining
- **”Surface”** micromachining
- An **overview** is given in the following
 - Details can be found in literature

Bulk micromachining

- Selective etching and diffusion into well defined areas **of a substrate**
 - Etching of the substrate → membranes
 - Etching from back side (wet etching: liquid is used)
 - Possibly combined with dry etching on the front side
- More mature than surface micromachining
- Typical examples
 - Pressure sensor, accelerometer
- "Wafer-bonding" may be necessary
 - Interconnect whole wafers

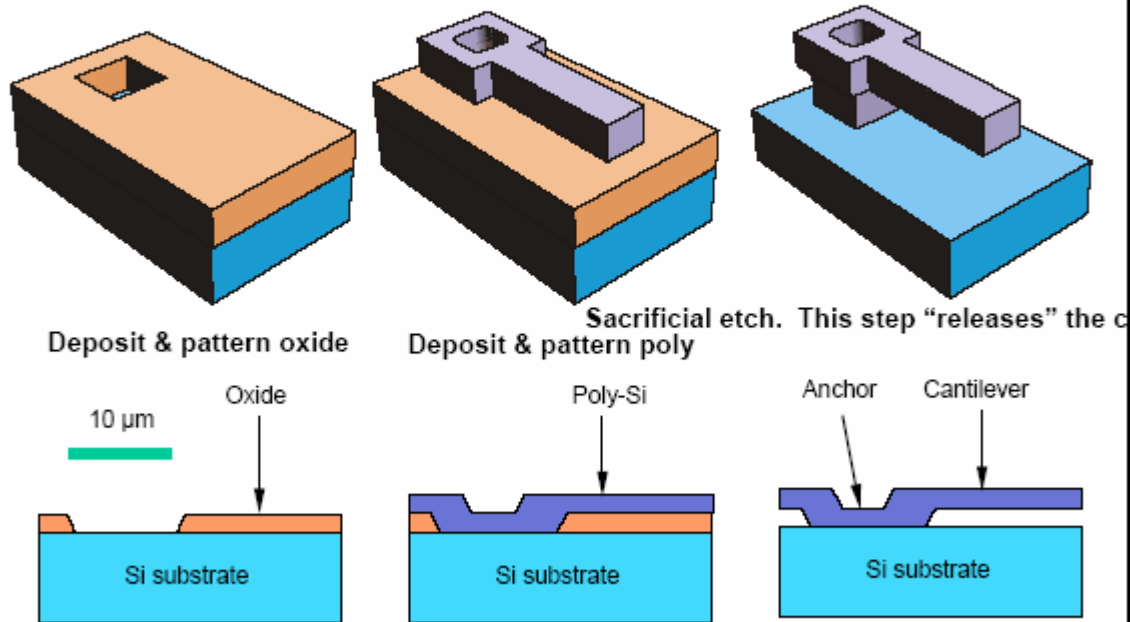
Pressure sensor



Surface micromachining

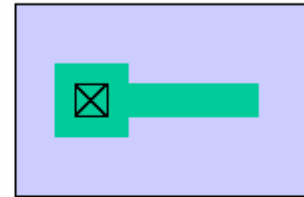
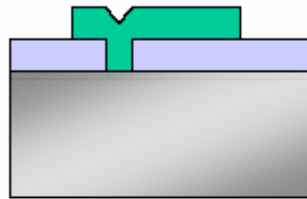
- **"Surface"** micromachining
 - Deposit layers
 - **Structural layer**
 - **Sacrificial layer** = "distance-keeping" layer
 - Selective etching of structural layers
 - Removing sacrificial layers

Micromachining a Cantilever



8

Surface Micromachining



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Surface micromachining

- + Can make structures with smaller dimensions
- ÷ Structures have smaller "mass"
 - Not meeting requirements for some applications
 - accelerometer
- + Possible to integrate IC-components
- **Structural layers** must have
 - Desired **electrical** properties
 - Proper **mechanical** properties
 - Elasticity, density, reliability
 - **Stress**: different stress in interfacing films may be a problem
- **Sacrificial layer**
 - Must be removed effectively by etching
 - Avoid **stiction**
 - Perforating large surfaces may be needed

Residual Stress in Thin Films

- Residual film stress
 - Microstructure
 - Thermal mismatch



- Compressive vs. tensile stress

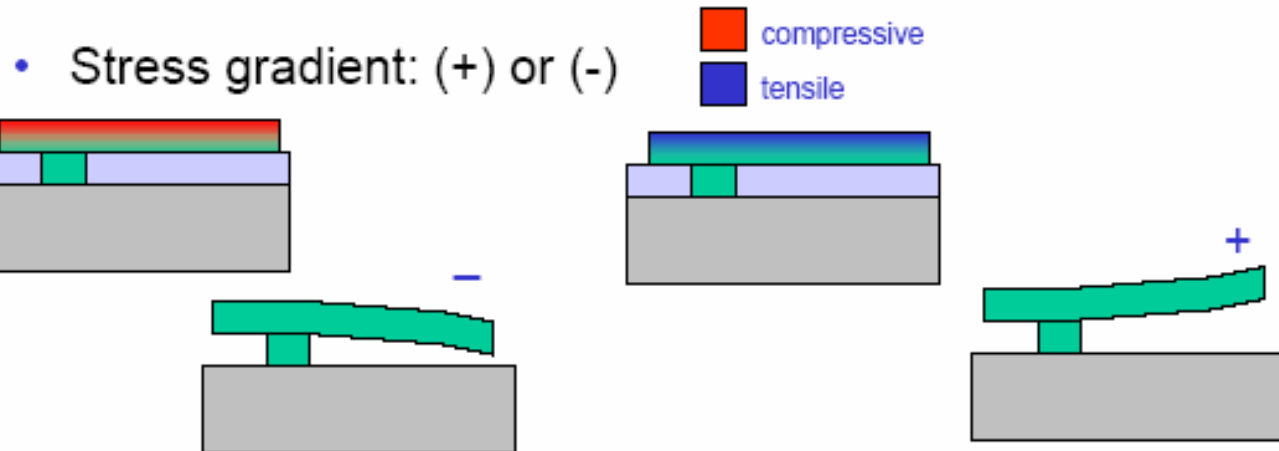


Under **compressive stress**, film wants to expand. Constrained to substrate, bends it in convex way.

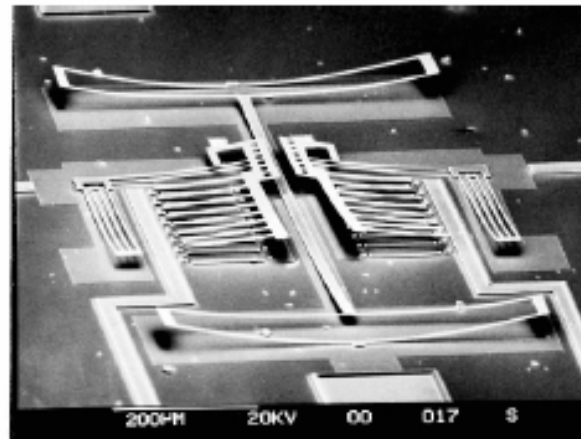
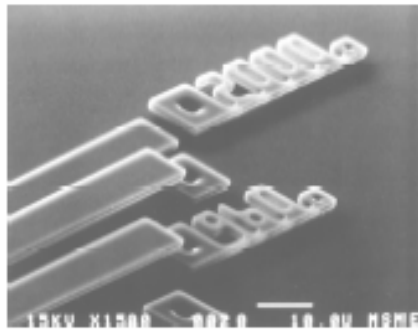


Under **tensile stress**, film wants to shrink. Constrained to substrate, bends it in concave way.

Stress Gradients



"Curling" →



Important process steps

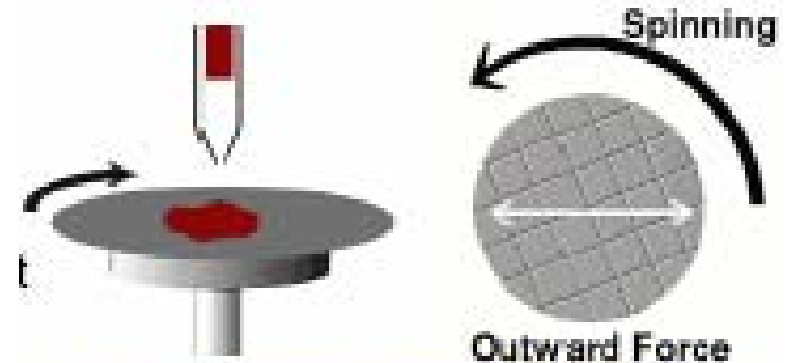
- Define patterns
 - *Photolithography*
- Modify semiconductor material properties
 - *Diffusion*
- Remove material
 - *Ething*
- Adding material – build structures
 - *Deposition*

Photolithography

- **Transfer design pattern → pattern in material**
 - Optical exposure using **photo mask**
 - Using photoresist (organic) – "spin-on"
- **Mask -types**
 - Emulsion mask
 - Chromium mask
 - Direct patterning on wafer
- **Exposure methods**
 - Contact: reduces lifetime of mask
 - "Proximity": 25 – 50 μm distance
 - Projection using complex optics
 - Electron beam (e-beam) writing patterns
- **Exposure → developing of photoresist → "post bake" → "treatment" of material (etching/diffusion)**

Spin-on methods

- Material drop in centre is spinned on
 - For organic materials
 - **Photoresist**, polyimide's, 0.5 – 20 μm
 - SU-8 (epoxy-based), > 200 μm
 - For dielectric isolators
 - Thickness depends of
 - Concentration, viscosity, speed, time



Topographic height variations give problems

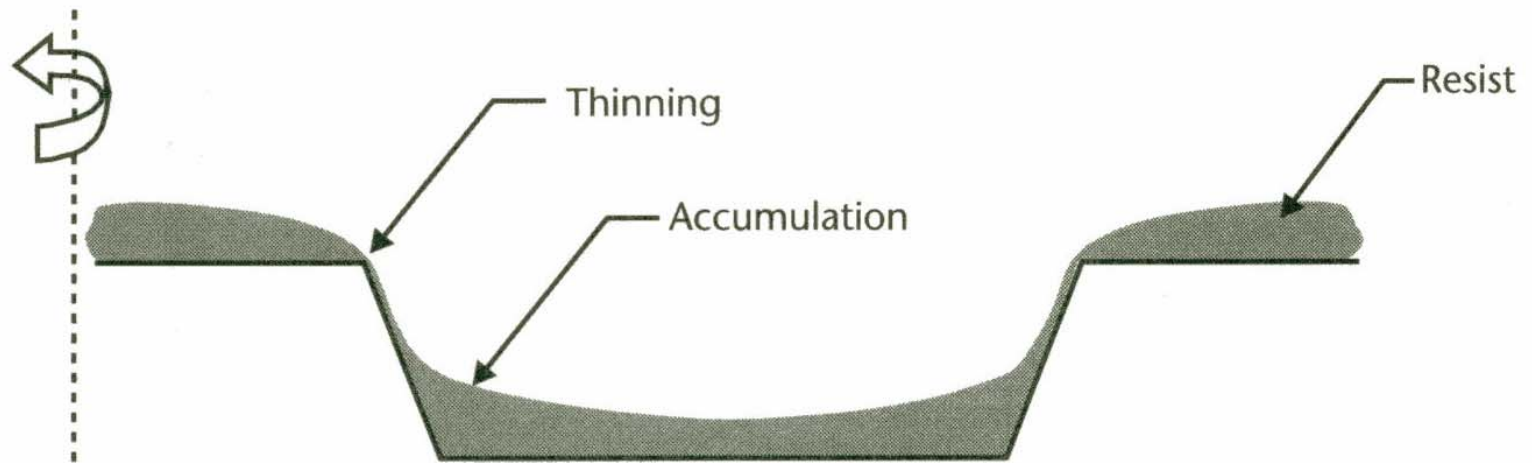
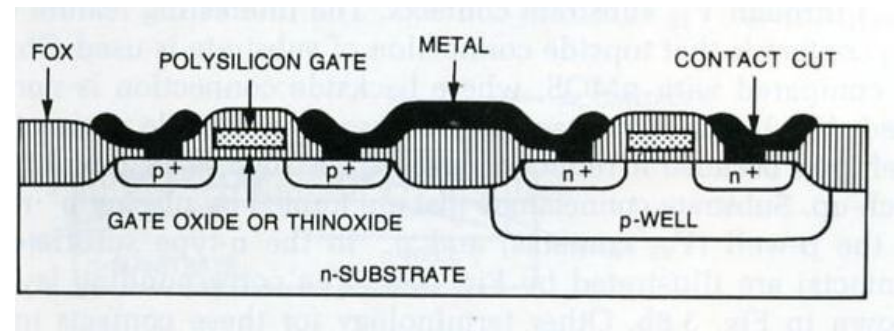


Figure 3.3 Undesirable effects of spin-coating resist on a surface with severe topographical height variations. The resist is thin on corners and accumulates in the cavity.

Maluf

Modify material properties: Diffusion

- Diffusion of impurities in semiconductors
 - Dope materials
 - Phosphorus (n+), Boron (p+)
 - "predeposition",
 - "ion implantation"
 - "drive-in" at high temp



- Type and concentration of dope materials determine electrical properties
 - Two mechanisms
 - **Diffusion current** due to concentration gradients of free charges (n, p)
 - **Drift of charges** due to electric field

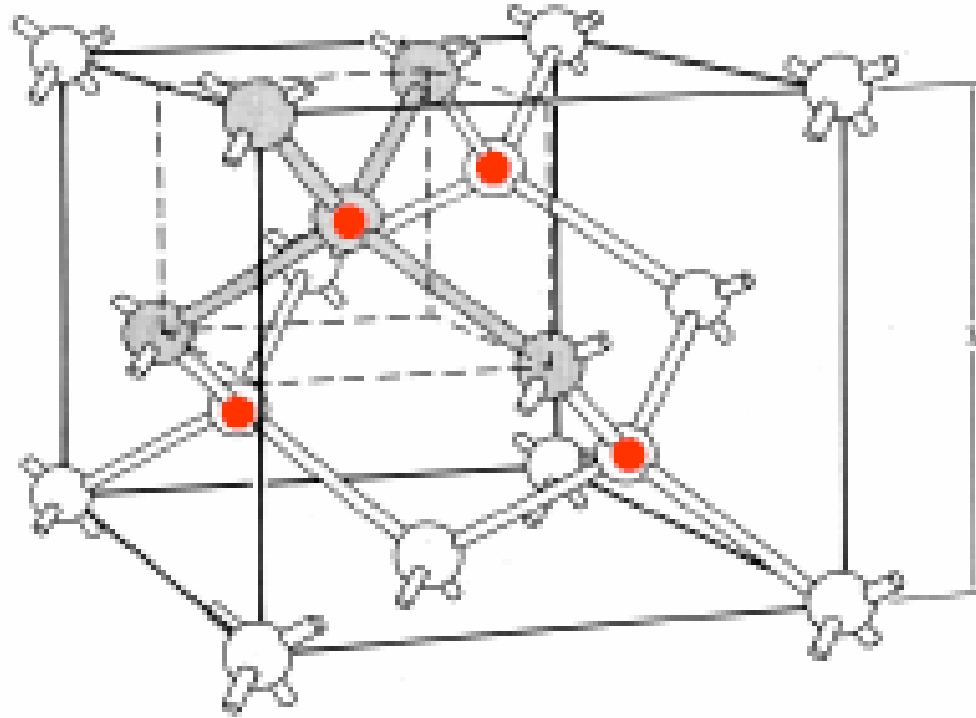
Remove material: Etching

- Wet-etching or dry-etching
- **Wet-etching**
 - Deep etching of Si is essential in micromachining
 - Using liquids
 - Depends on:
 - Concentration of liquid, time, temperature
 - Not precise
 - Low cost batch processing
 - Both **isotropic** or **anisotropic**

Wet-etching

- **Isotropic** = uniform etching in all directions
 - HF or blends are usual
 - 0.1 – 100 $\mu\text{m}/\text{min}$ etch speed
- **Anisotropic** = etching faster along some directions
 - Etch speed depends of **crystal orientation**
 - NaOH, KOH used
 - Silicon nitride used as mask for **KOH**

Crystal orientation in Si

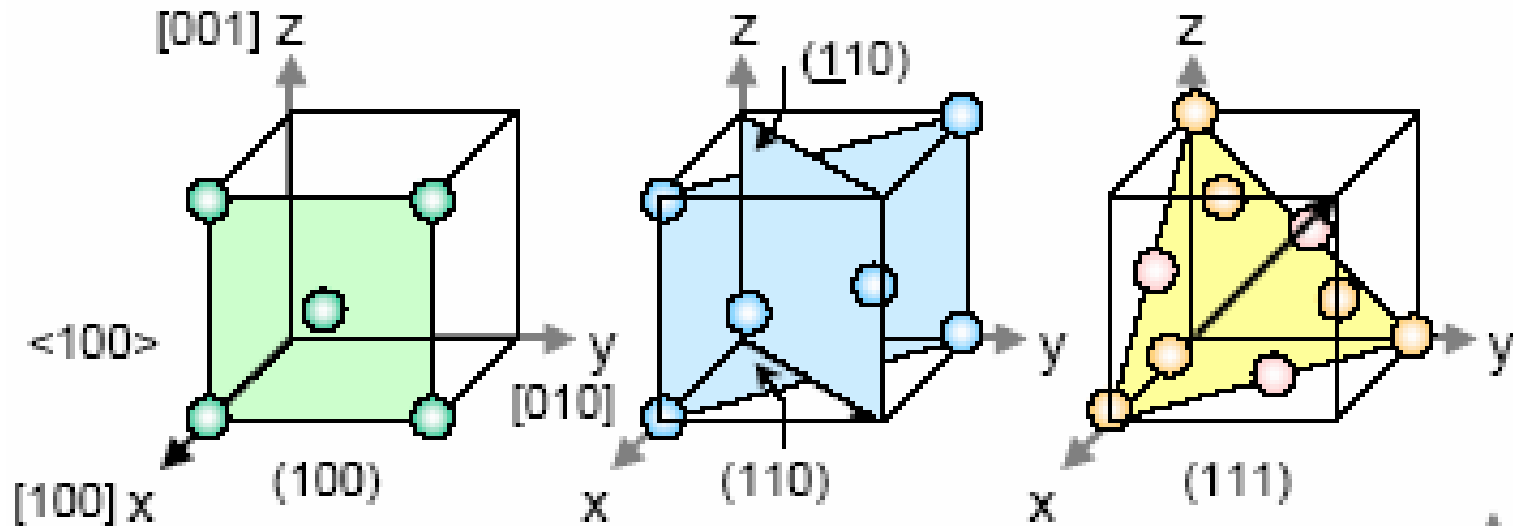


Silicon crystal structure

$$\lambda = 5.43 \text{ \AA}$$

Wolf and Tauber

Crystal directions



Miller indekser: (plan), {familie av plan}, [retning], <familie av retninger>

Different etch methods

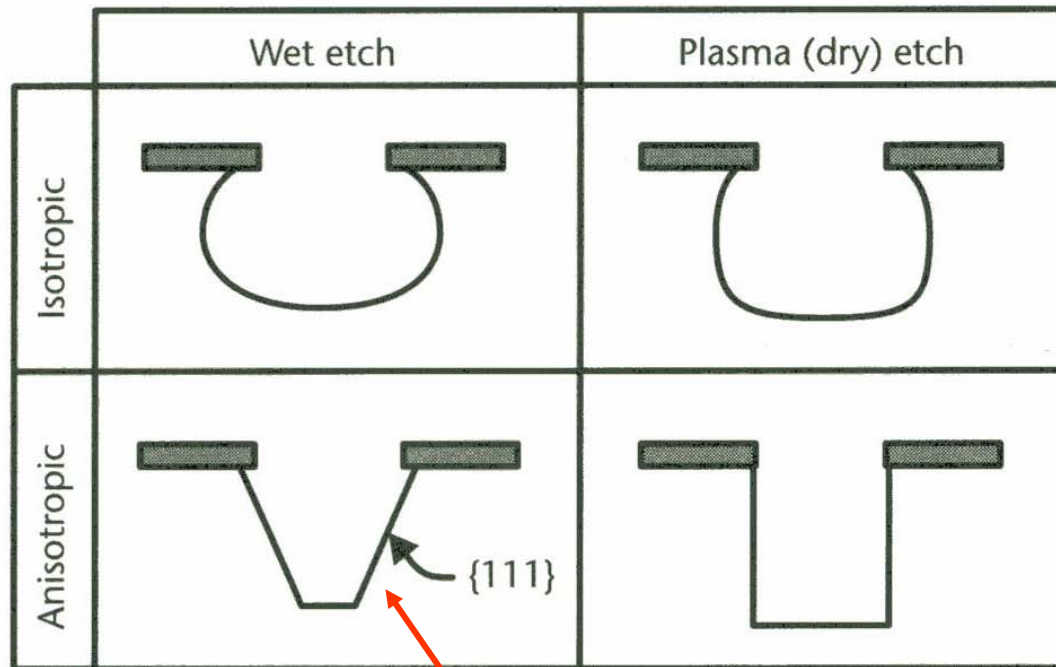


Figure 3.5 Schematic illustration of cross-sectional trench profiles resulting from four different types of etch methods.

54.7°

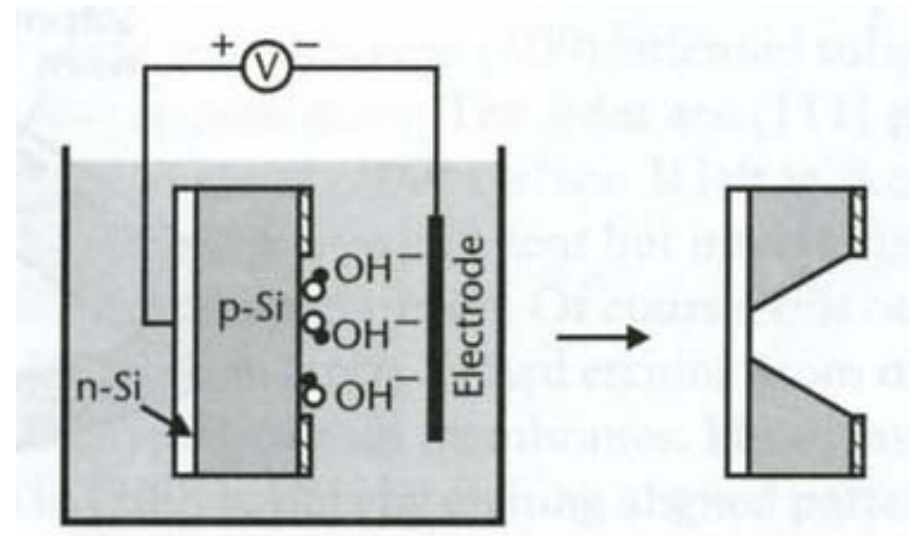
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Anisotropic wet etching

- **KOH**-etching
 - {110} planes are etched 2x the speed of {100}
 - {111} plans are etched 100 x slower than {100}
 - Disagreement on reason: density of energy bands or formation of thin oxide layer?
- Used for making V-grooves
- Other anisotropic etch liquids
 - **TMAH**, ratio (100)/(111) = 10 – 35
 - SiO₂ may then be used as a mask

Controlling etch depth

- Etch depth controlled by **electrochemical etching**
 - Precise growing of epi-layer
 - Ex. n-type on p-wafer
 - Apply electric potential
 - pn-diode reverse biased
 - p-material etched
 - Etching stops at pn-junction
 - Thin SiO₂ layer formed
 - Used to define thickness of membranes



Dry-etching

- 1. Vapor-phase etching
- 2. Plasma-etching
- 3. Reactive Ione-Etching
 - RIE
 - DRIE
- 4. "Ion milling"

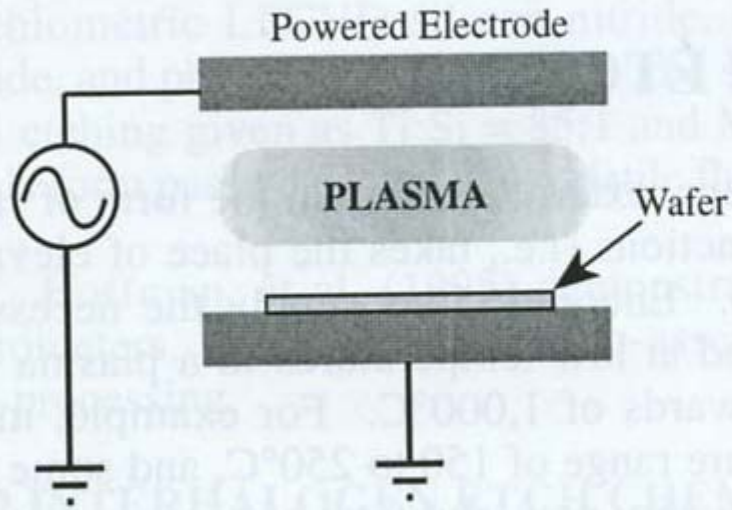
Dry-etching, contd.

- **1. Vapor-phase etching**
 - Use reactive gases ("vapor")
 - Both isotropic and anisotropic etching
- **2. Plasma-etching**
 - *Plasma: "electric neutral, highly ionized gas of ions, electrons and chemical reactive, neutral particles"*
 - Chemical reactive particles and ions are accelerated in an electric field towards the Si substrate ("target")
 - Etching Si, SiO₂, Si₃N₄, polysilicon, metals
 - The **chemical reaction** at the surface is critical for **plasma-etching**
 - **Low temperature etching!**

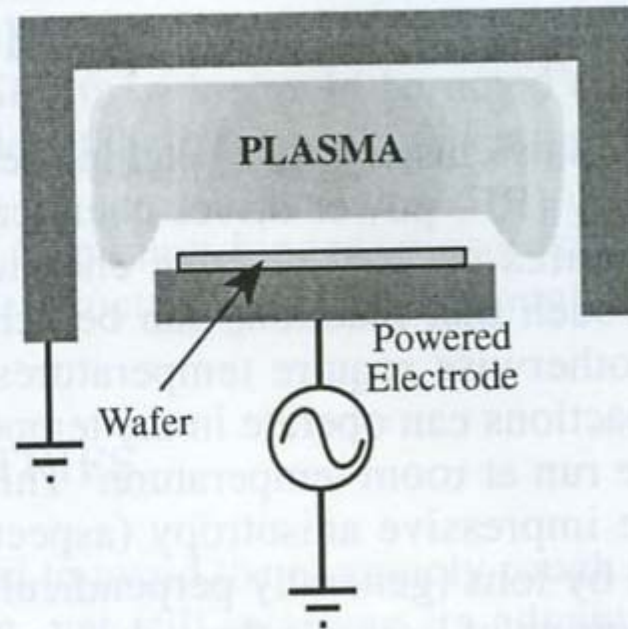
Dry-etching, contd.

- **3. RIE – Reactive Ion Etching**
 - **Bombarding the Si-surface** with reactive particles is important for **RIE**
 - "Synergy effect"
 - Low pressure
 - Larger anisotropy possible
 - Vertical beam : vertical anisotropy
 - Higher etch speed

PLASMA ETCHER



REACTIVE ION ETCHER



Kovacs

DRIE

- **DRIE** – Deep Reactive Ion Etching (1995-)
 - Vertical etching
 - Can etch deep holes ($> 500 \mu\text{m}$) with almost perfect vertical sidewalls
 - **Bosch-method**
 - Figure \rightarrow
 - High "aspect-ratio"
 - Etching and deposition every second step
 - **etch**: SF_6 , mostly at the bottom!
 - **deposit**: polymer

Bosch-process

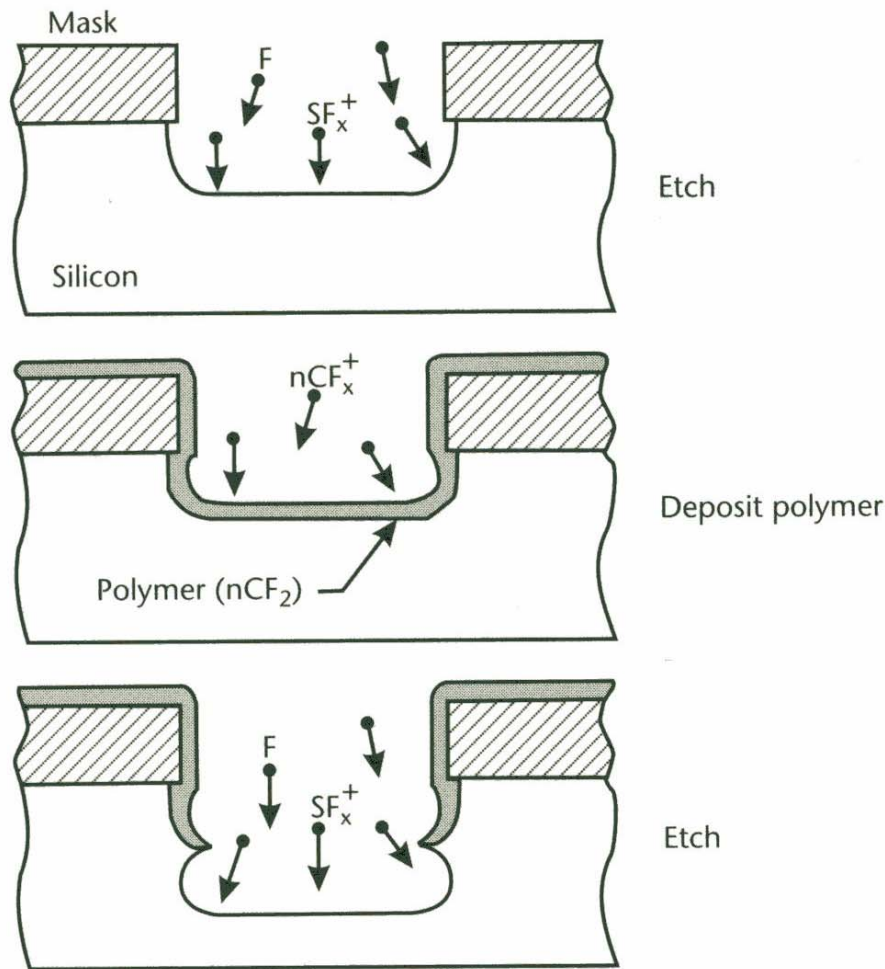
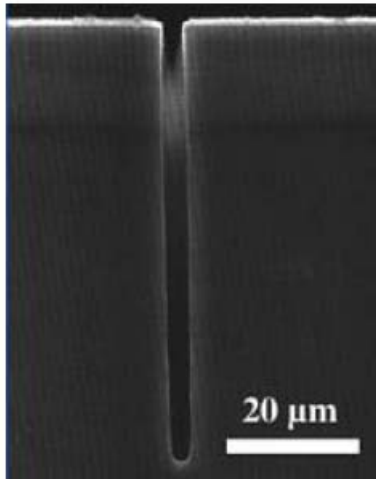
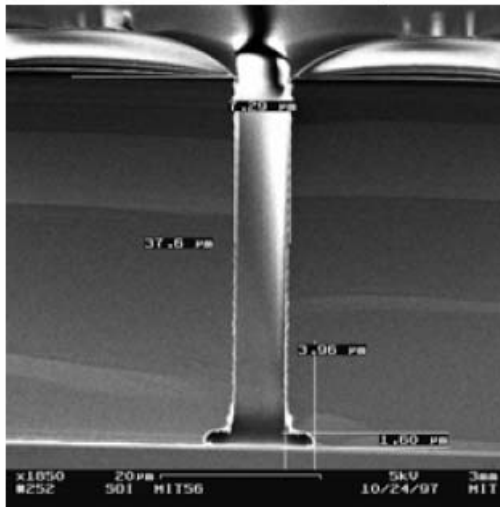
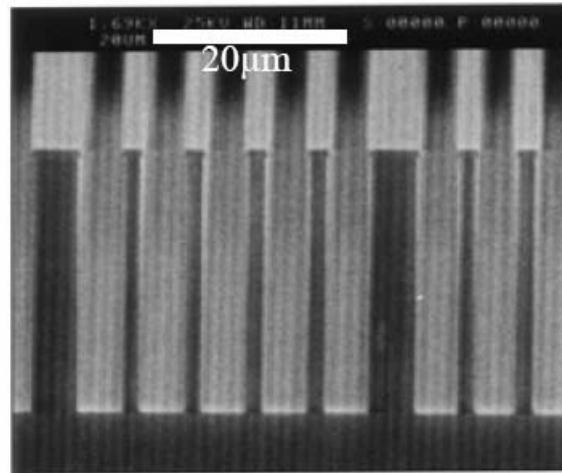


Figure 3.12 Profile of a DRIE trench using the Bosch process. The process cycles between an etch step using SF_6 gas and a polymer deposition step using C_4F_8 . The polymer protects the sidewalls from etching by the reactive fluorine radicals. The scalloping effect of the etch is exaggerated.

Deep RIE Examples

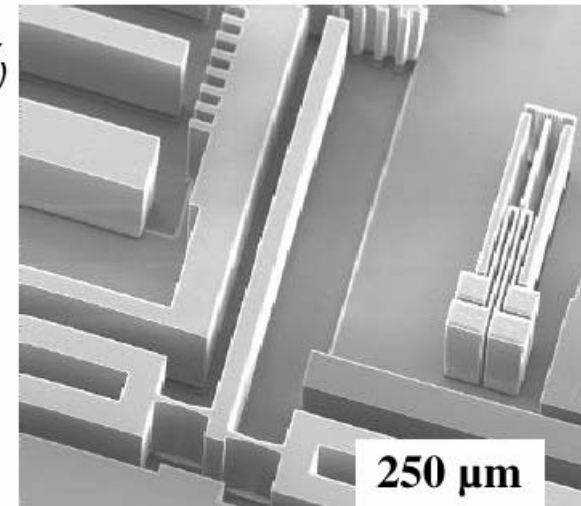


STS 1999



Ayon et al.,
1998 (MIT)

Klaassen et al.,
1995 (Stanford)



4. Ion milling

- **Inert gas** (Ar) accelerated towards substrate
 - ~ 1kV
- No chemical reaction
 - **All materials can be etched by this method**
- Vertical etch profile
- Lower etch speed than RIE

Building of structures

- **Deposition** of thin or thick layers ("films")
 - Conductors: Al, Cu
 - Semiconductors: Si, polySi
 - Isolators: SiO₂, Si₃N₄
 - Polymers (organic)
- **Bonding-techniques**
 - Interconnecting wafers

Additive process steps

- Formation of films on substrate surface
 - **Structural layers**
 - **Sacrificial layers ("spacers")**
- Techniques
 - a. Epitaxial growth
 - b. Oxidation
 - c. Vaporization
 - d. CVD, Chemical Vapor Deposition
 - e. Sputtering
 - f. Moulding

a. Epitaxial growth

- Epitaxial growth

- Used a lot in IC industry

- Growth of **crystalline** Si on a Si-wafer

- Vapor-phase chemical deposition > 800 °C

- Gives the same crystalline orientation as the wafer

- Doped materials used: arsenic, phosphorus, boron

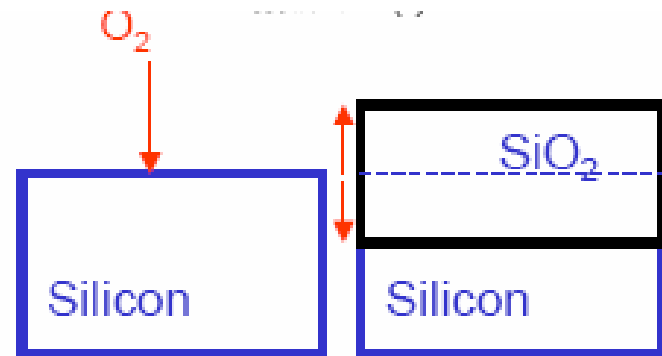
- Thin, 1-20 μm

- Growth of **polycrystalline** material on SiO_2

- Growth of Si on Sapphire (SOS)

b. Oxidation of Si

- Thermal oxidation
 - **High quality** thermal grown oxide
 - Dry O_2 or vapor at **high temp**, 850-1150 °C
 - Thermal oxidation generates compressive **stress** → deflection!
 - Volume of SiO_2 is larger than Si
 - Different thermal coefficients of expansion, TCE



c. Vaporization

- Heating the source to high temp
 - → vapor → condensation → **film deposition** on wafer
 - ~Vacuum
- Vaporization takes place due to thermal heating or e-beam bombardment
- Is a **directive** deposition method
 - The source is relatively small
 - Material deposited at a specific angle
 - Gives bad step coverage (corners, sidewalls)
- Most films get **tensile** stress (stretched)

d. CVD

- **Chemical Vapor Deposition**
 - **Chemical reaction** initiated between vapor and heated surface
 - High temperature process, > 300 °C
 - Gives **high quality** thin film polySi, dielectric and thin metal films
 - Influenced by: temperature, gas-flow, dope material, pressure
- **Categories**
 - **PECVD**, Plasma-enhanced, ~ 300 °C or lower
 - PolySi, SiO₂, SiNitrid (0.2 nm – 2 μm)
 - Plasma excitation using RF
 - Good control of stress
 - **LPCVD**, Low-pressure, 400-800 °C

Deposition of polysilicon

- Poly is an attractive material for surface micromachining
 - Various thicknesses may be fabricated (nm \rightarrow μ m)
- Deposition of polysilicon using LPCVD
 - Crystalline grain structure achieved when > 630 °C
 - Temperature determines **tensile** or **compressive** stress
 - "Annealing" at 900 °C reduces stress

Deposition of isolators

- Deposition of **SiO₂**
 - LPCVD or PECVD may be used
 - < 500 °C, **LTO = low-temp oxide**, amorphous
 - **The quality is not that good as for a thermal grown oxide!**
 - Used as isolator or sacrificial layer
 - Etched using HF
- Deposition of **Si₃N₄**
 - Used for passivation
 - Used as mask for some etchings (KOH)

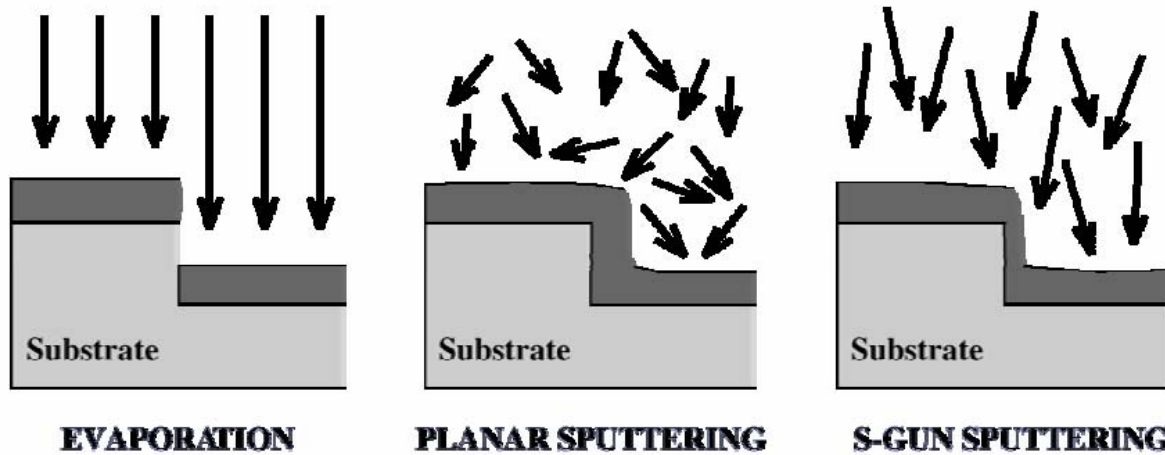
e. Sputter deposition

- **Method:**
 - **Target** material bombarded with a flow of inert gas ions (Ar⁺)
 - ~ vacuum
 - Released atoms deposit on the wafer
- **Low temperature** <150 °C
 - Many applications in MEMS
- **Many types of materials**
 - Both conducting and isolating materials can be sputtered
 - Thin metal films, glass, piezoelectric films (PZT)
- Different classes of sputtering available
 - Ions are accelerated in a **DC** electric field between "target" and "wafer"
 - **RF**-excitation of "target"
 - Ion beam generated in **plasma** and accelerated towards "target"

Sputter deposition, contd.

- Alternative type: **reactive sputtering**
 - Nitrogen or oxygen gas is added, **reacts!**
- Direction "randomness" can be achieved
 - When sputter target is larger than wafer
 - Gives good step coverage
- Good stress control
 - Stress level depends of sputter **power** and **pressure** in chamber
 - *Tensile stress*: low power, high pressure
 - *Compressive stress*: high power, low pressure

Sputtering vs. Evaporation



Geometry of evaporation and sputtering chambers (as well as electromagnetic fields) determine *directionality* of deposition:

Good or bad step coverage (can be advantage or disadvantage)

Figure: G. Kovacs, 1996.

"Adhesion layer"

- Many metals have bad adhesion to Si, SiO₂, Si₃N₄
 - Peeling off
- Add a thin layer to increase **adhesion**
 - Gold, silver, platinum
 - Cr, Ti
 - Should avoid oxidation of the adhesion layer during processing, - will destroy adhesion

f. Moulding

- **LIGA** = a moulding method
 - **Lithographie, Galvanoformung, Abformung**
 - X-ray used for mask exposure
 - Galvanoforming → metal mould is formed
 - Moulding → components formed
 - **Plastic**, metal, ceramic -components
- + Flexible method
- ÷ X-ray used, high fabrication cost
- + Gives high aspect ratio, 3D components!
- ÷ Limited because 3. dimension is limited to vertical
- Thick **photoresist** may also be used to build a mould

Advanced process-steps

- **Anodic bonding**

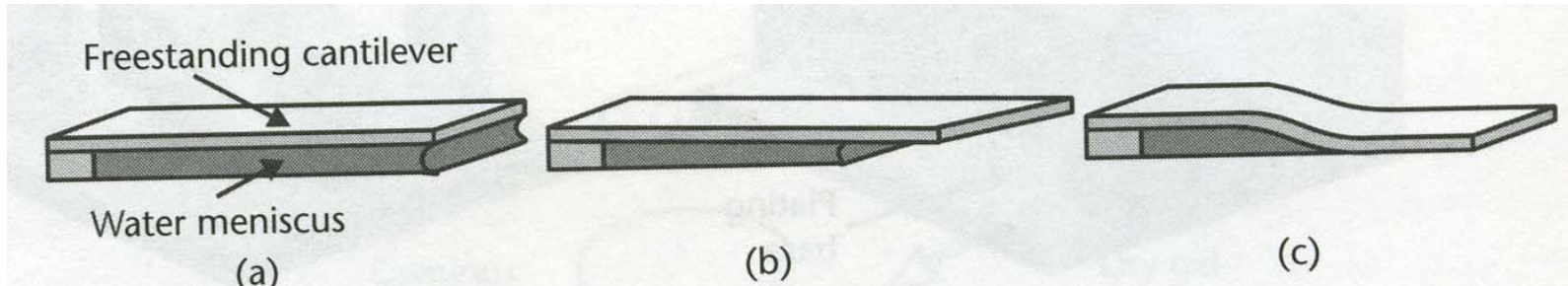
- Si-wafers are bonded together, glass – Si
 - Used for pressure sensors (jmfr. MultiMEMS →)
- 200 – 500 °C, 500 – 1500 V
- Glass has negative ions at the contact interface with Si

- **Electroplating**

- Thin **seed layer** is deposited at the Si substrate
 - “A thin metal layer is **electroplated** on the surface using either chemical or electrolytic plating”
- Plating using gold, copper, nickel etc.
- May give thick layers, 5 – 100 µm
- May be used for **moulding**: - making a **mould**

Supercritical drying

- **Removing sacrificial layer** is problematic
 - HF etches → water rinsing is used
 - The water may stick to the structures due to the surface tension
 - Thin wafer ("meniscus") is formed
 - The volume of the liquid decreases when dried
 - Structure is pulled down → **"stiction"** → **structure must be released!**
- **"Supercritical Point Drying"**: avoids forming of meniscus
 - Wet wafer is placed in a methanol chamber
 - Liquid CO₂ is added → the blend is removed → CO₂ rest is heated to the supercritical region (transition: gas - liquid) → the gas is removed



Structural – sacrificial layers

Structure

polySi

Al

SiO₂

Al

poly-SiGe

Sacrificial

SiO₂, PSG, LTO

photoresist

polySi

Si

poly-Ge

Etchant

HF, BHF

O₂ plasma

XeF₂

EDP, TMAH, XeF₂

H₂O₂, hot H₂O

Srinivasan

Structural – sacrificial layers

- Structural layer – sacrificial layer (Varadan)
 - polySi SiO₂
 - Polyimide aluminum
 - Si₃N₄ polySi
 - Wolfram SiO₂

Summary: MEMS-specific steps

- Methods **especially** developed for MEMS
 - Anisotropic chemical wet-etching
 - Deep reactive ion-etching, RIE, DRIE
 - Etching of sacrificial layer
 - Moulding

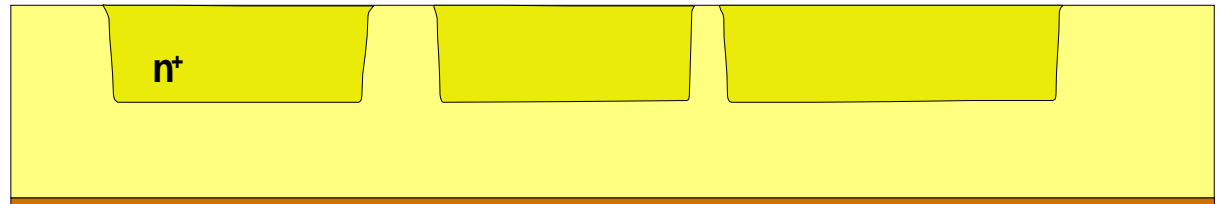
 - "Wafer bonding"
 - Electroplating
 - "Critical-point drying"

Examples of processes

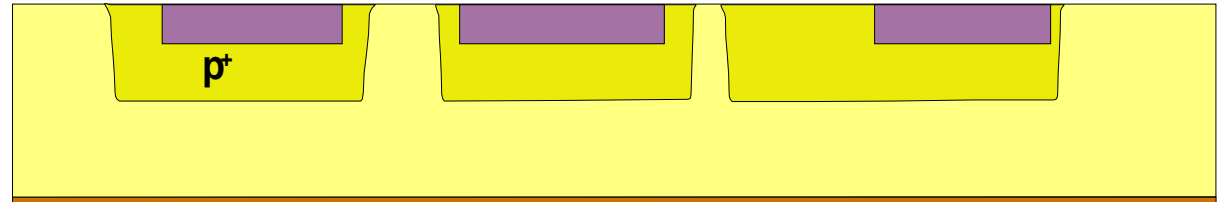
- Bulk micromachining
- **MultiMEMS** from InfineonSensonor →
 - Europractice

MPW Process (1)

- **NOWEL :**
n impl. + diff.



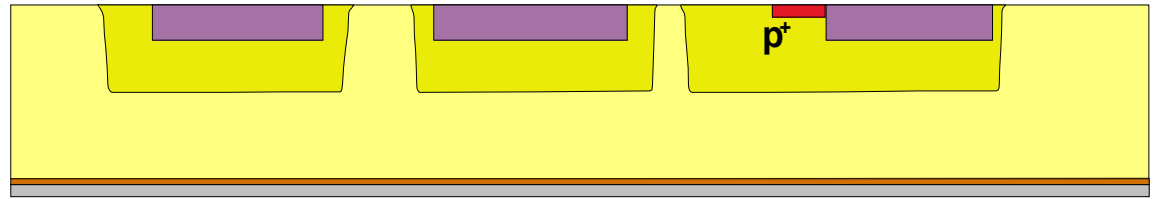
- **BUCON :**
p impl. + diff.



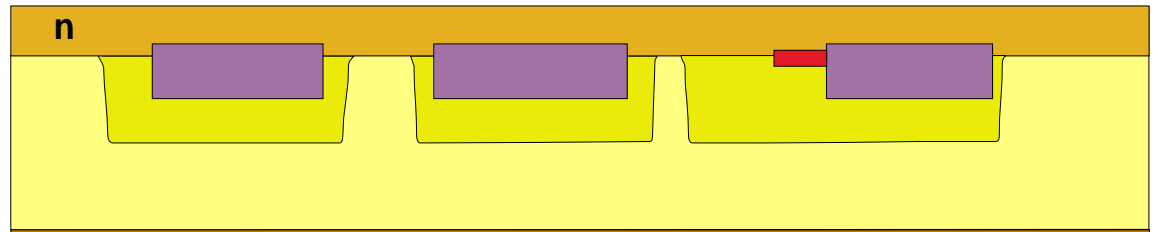
The following slides are from MultiMEMS, SensoNOR/Europractice

MPW Process (2)

- BURES :
p impl. + diff.

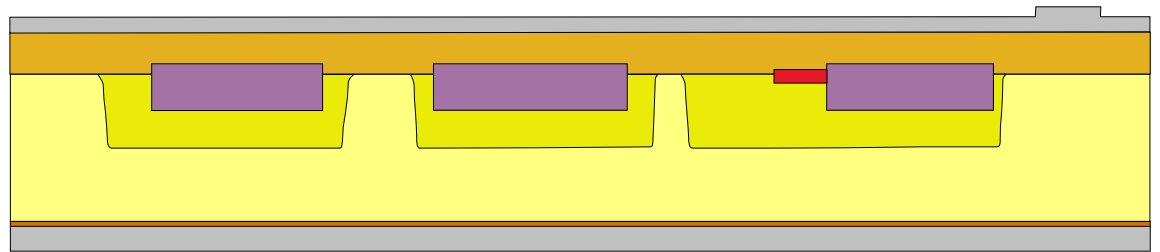


- n epi

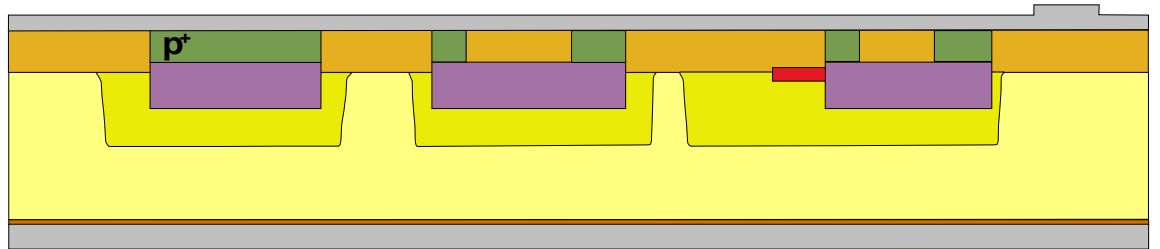


MPW Process (3)

- TIKOX :
2 oxidations

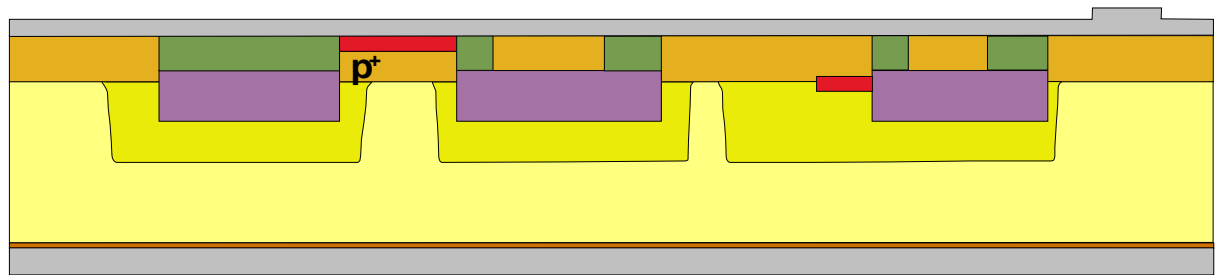


- SUCON :
p impl. +
diff.

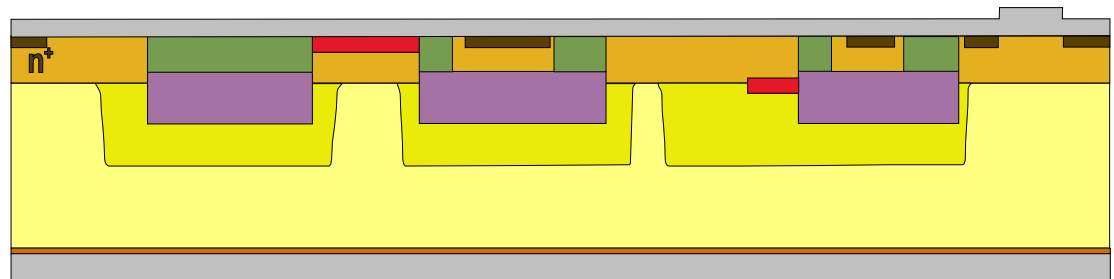


MPW Process (4)

- SURES :
p impl.

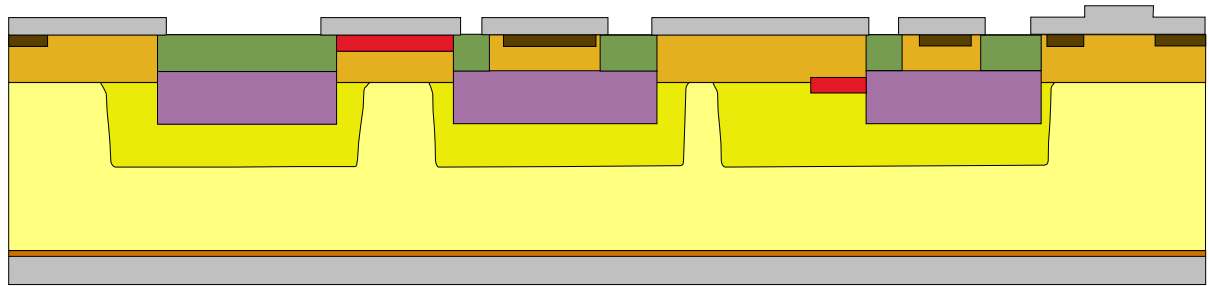


- NOSUR :
n impl. + diff

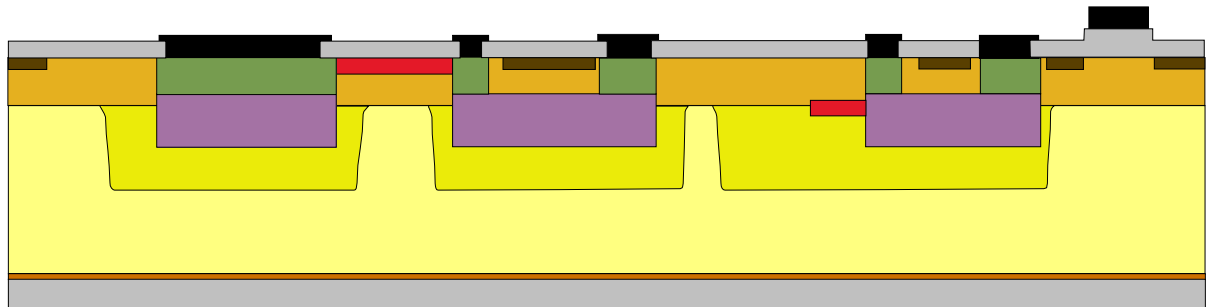


MPW Process (5)

- COHOL :
oxide etch

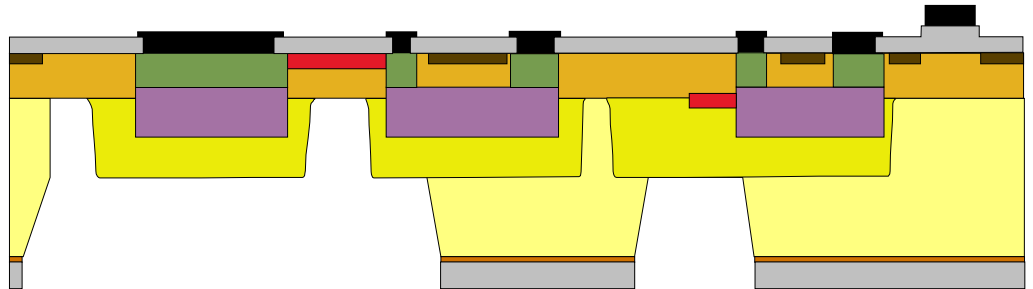


- MCOND :
Al sputter +
pattern

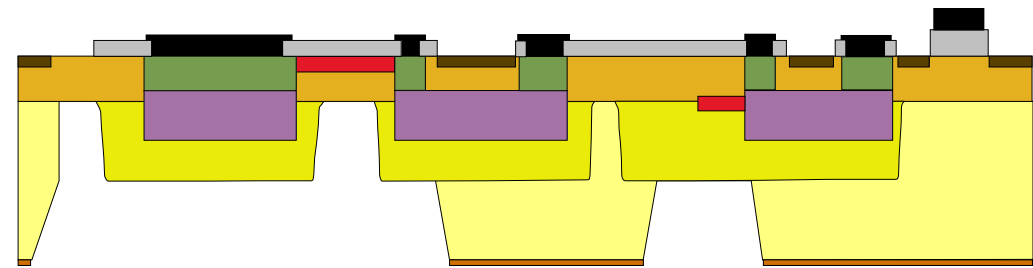


MPW Process (6)

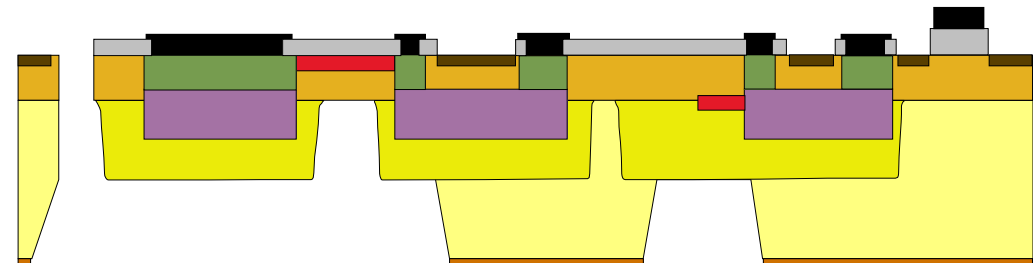
- **BETCH :**
TMAH
etch



- **NOBOA :**
oxide etch

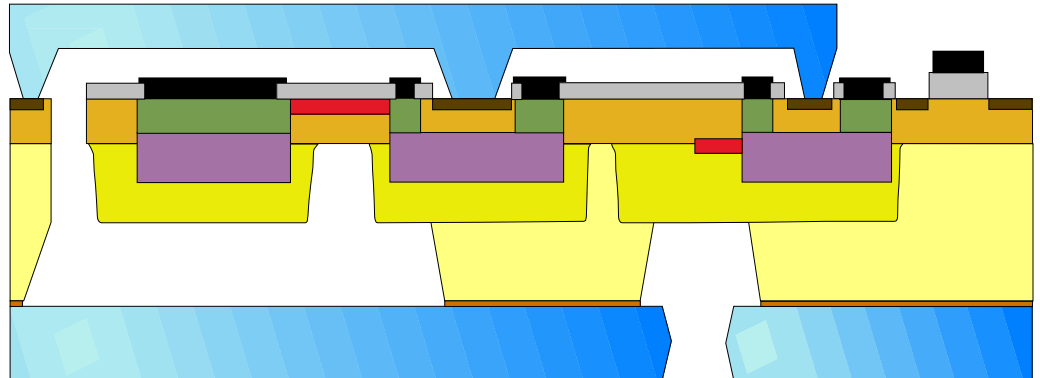
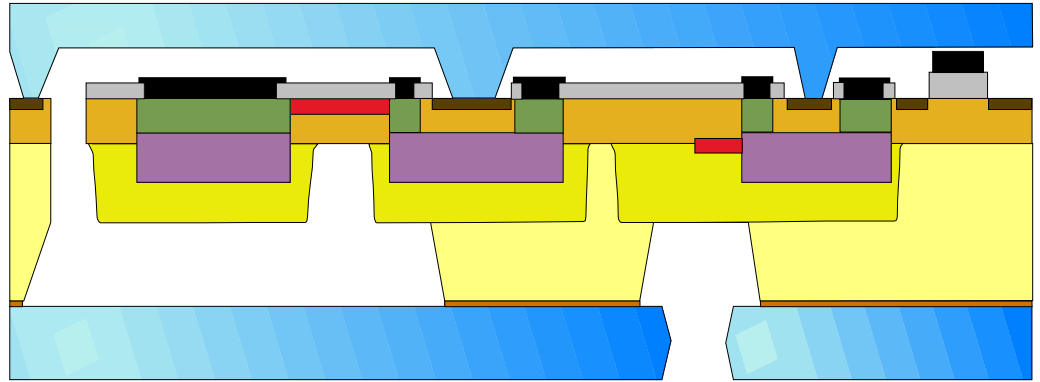


- **RETSCH :**
dry etch



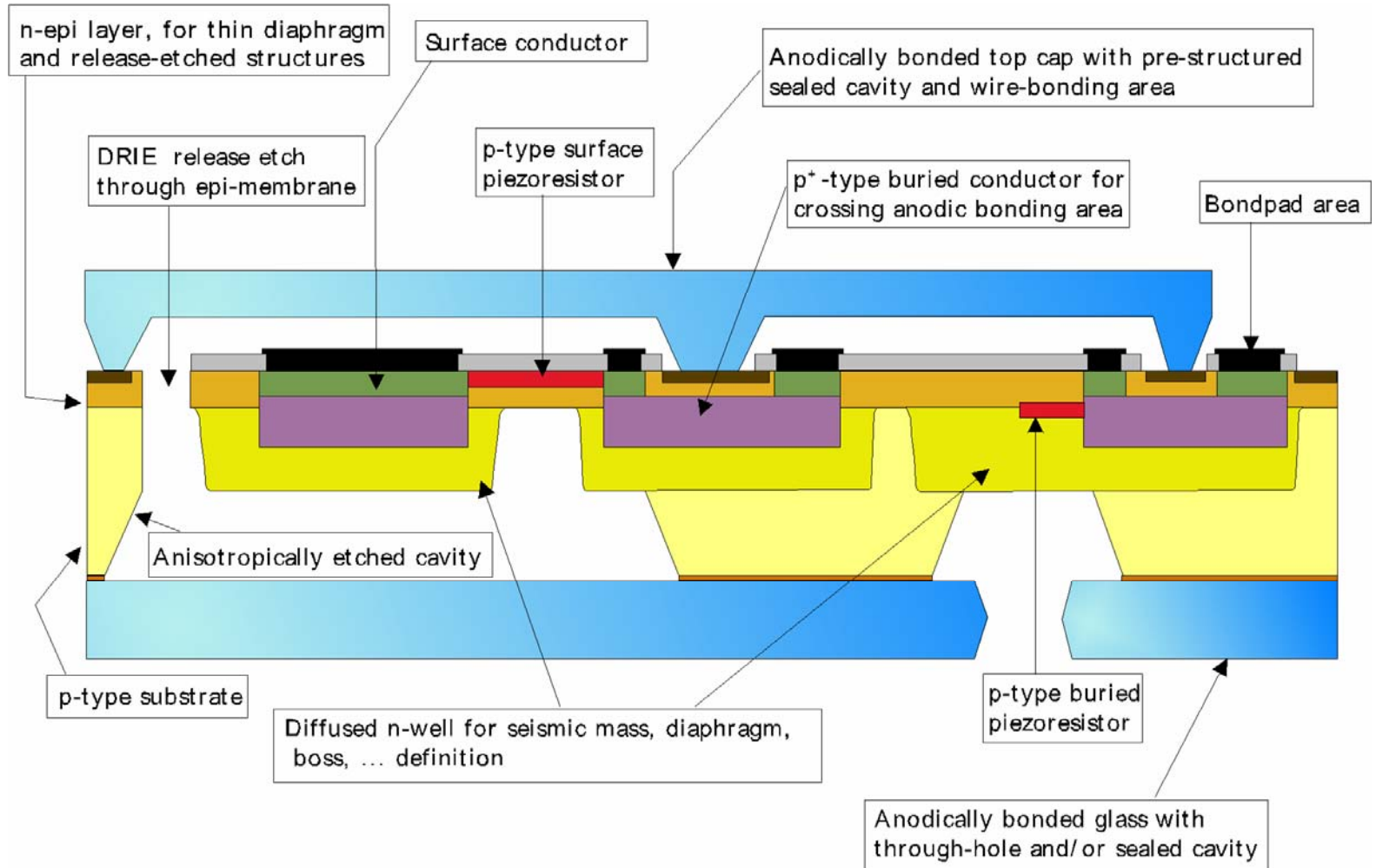
MPW Process (7)

- TOGE;
BOGEF;
BOGEB :
wet etching of
glass +
anodic
bonding



- Dicing

Cross section overview

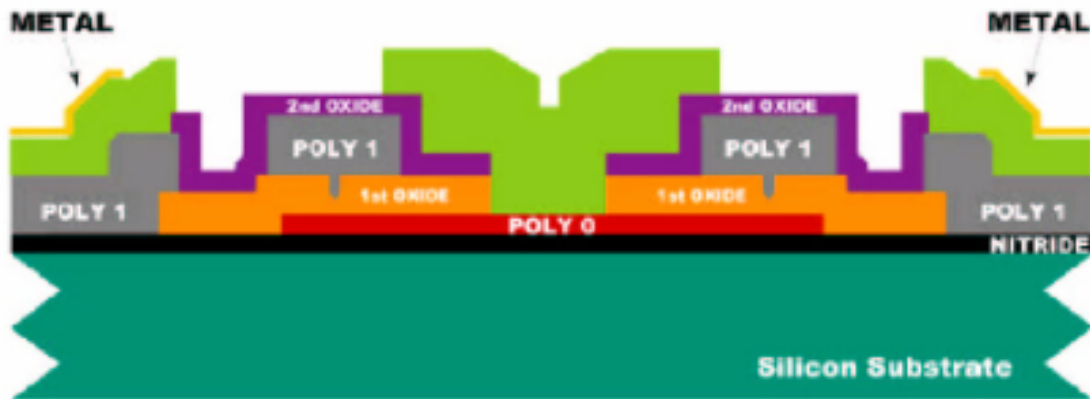
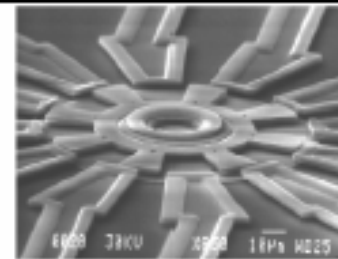


Examples of processes

- Surface micromachining

– **polyMUMPs** from MEMSCAP →

MUMPS Micromotor



EE C245

U. Srinivasan

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Følgende slides fra polyMUMPs:

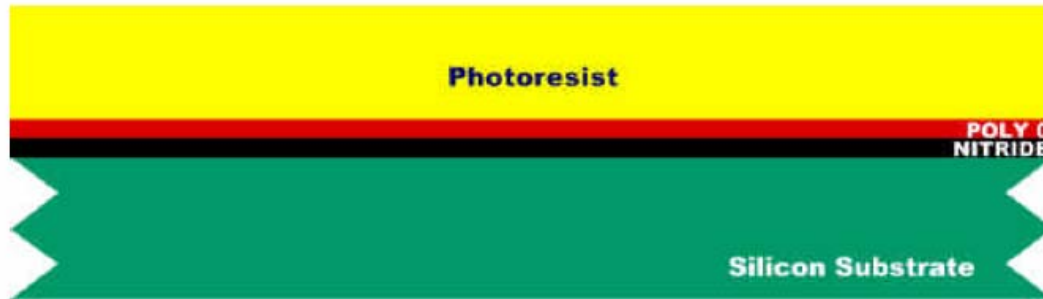


FIGURE 1.2. The surface of the starting n-type (100) wafers are heavily doped with phosphorus in a standard diffusion furnace using POCl_3 as the dopant source. A 600 nm blanket layer of low stress silicon nitride (Nitride) is deposited followed by a blanket layer of 500 nm polysilicon (Poly 0). The wafers are then coated with UV-sensitive photoresist.

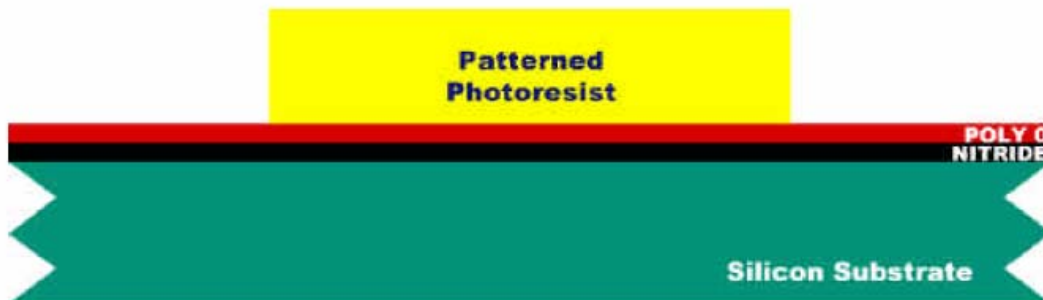


FIGURE 1.3. The photoresist is lithographically patterned by exposing it to UV light through the first level mask (POLY0) and then developing it. The photoresist in exposed areas is removed leaving behind a patterned photoresist mask for etching.

3-LAYER POLYSILICON SURFACE MICROMACHINING PROCESS



FIGURE 1.4. Reactive ion etching (RIE) is used to remove the unwanted polysilicon. After the etch, the photoresist is chemically stripped in a solvent bath. This method of patterning the wafers with photoresist, etching and stripping the remaining photoresist is used repeatedly in the PolyMUMPs process.



FIGURE 1.5. A $2.0\ \mu\text{m}$ layer of PSG is deposited on the wafers by low pressure chemical vapor deposition (LPCVD). This is the first sacrificial layer.



FIGURE 1.6. The wafers are coated with photoresist and the second level (DIMPLE) is lithographically patterned. The dimples, 750 nm deep, are reactive ion etched into the first oxide layer. After the etch, the photoresist is stripped.

CHAPTER 1

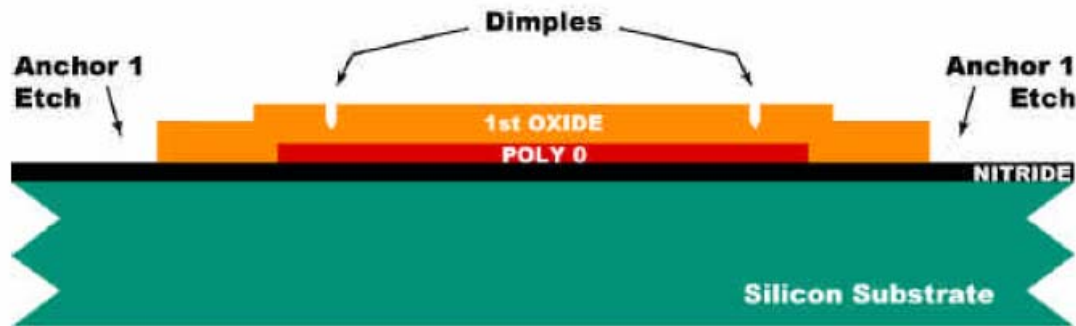


FIGURE 1.7. The wafers are re-coated with photoresist and the third level (ANCHOR1) is lithographically patterned. The unwanted oxide is removed in an RIE etch and the photoresist is stripped.

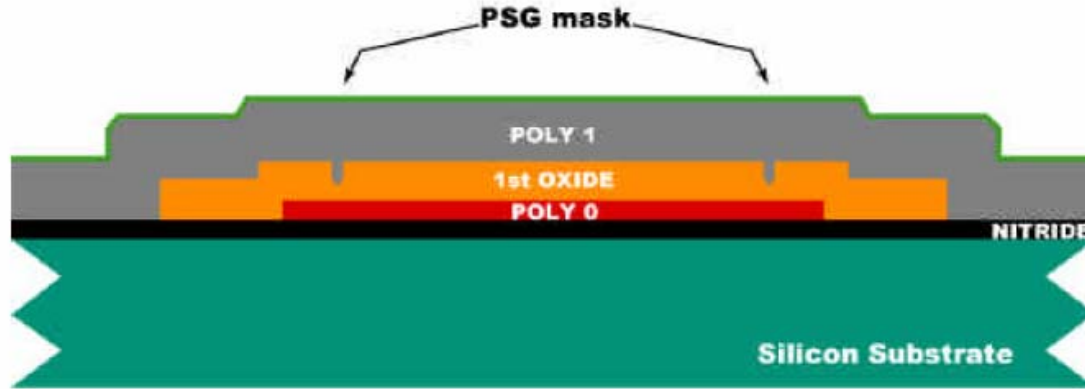


FIGURE 1.8. A blanket 2.0 μm layer of un-doped polysilicon is deposited by LPCVD followed by the deposition of 200 nm PSG and a 1050°C/1 hour anneal. The anneal serves to both dope the polysilicon and reduce its residual stress.



FIGURE 1.9. The wafer is coated with photoresist and the fourth level (POLY1) is lithographically patterned. The PSG is first etched to create a hard mask and then Poly 1 is etched by RIE. After the etch is completed, the photoresist and PSG hard mask are removed.

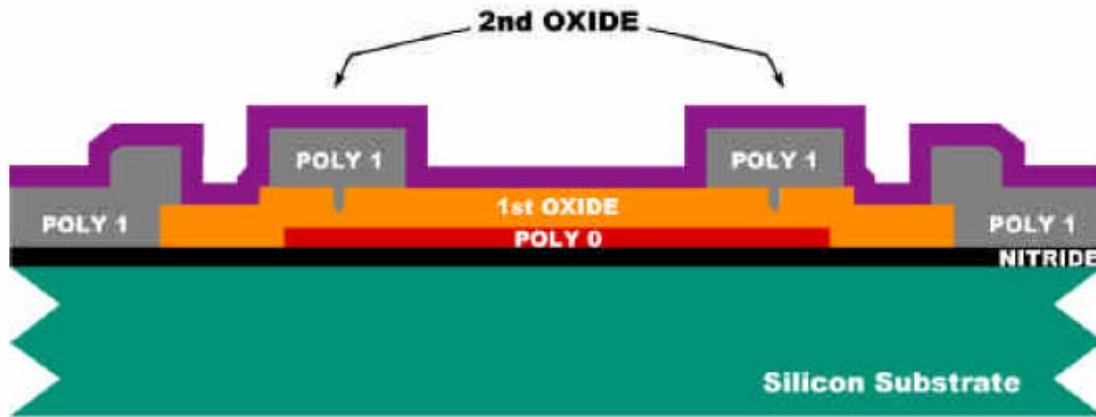


FIGURE 1.10. The Second Oxide layer, 0.75 μm of PSG, is deposited on the wafer. This layer is patterned twice to allow contact to both Poly 1 and substrate layers.



FIGURE 1.11. The wafer is coated with photoresist and the fifth level (POLY1_POLY2_VIA) is lithographically patterned. The unwanted Second Oxide is RIE etched, stopping on Poly 1, and the photoresist is stripped.

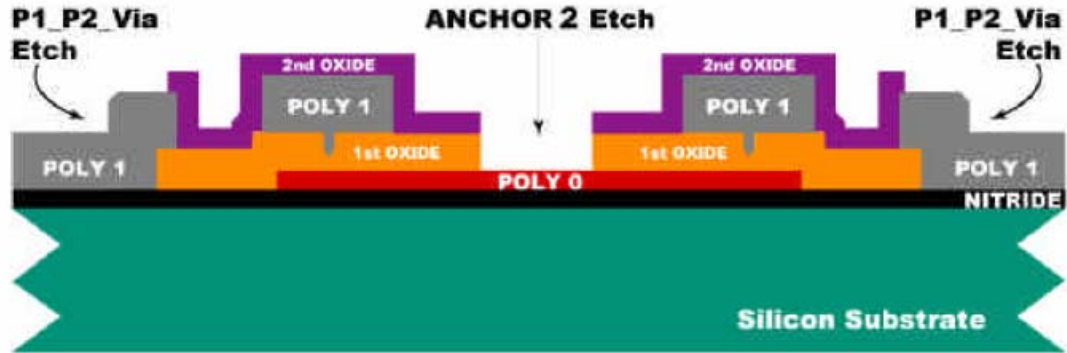


FIGURE 1.12. The wafer is re-coated with photoresist and the sixth level (ANCHOR2) is lithographically patterned. The Second and First Oxides are RIE etched, stopping on either Nitride or Poly 0, and the photoresist is stripped. The ANCHOR2 level provides openings for Poly 2 to contact with Nitride or Poly 0.

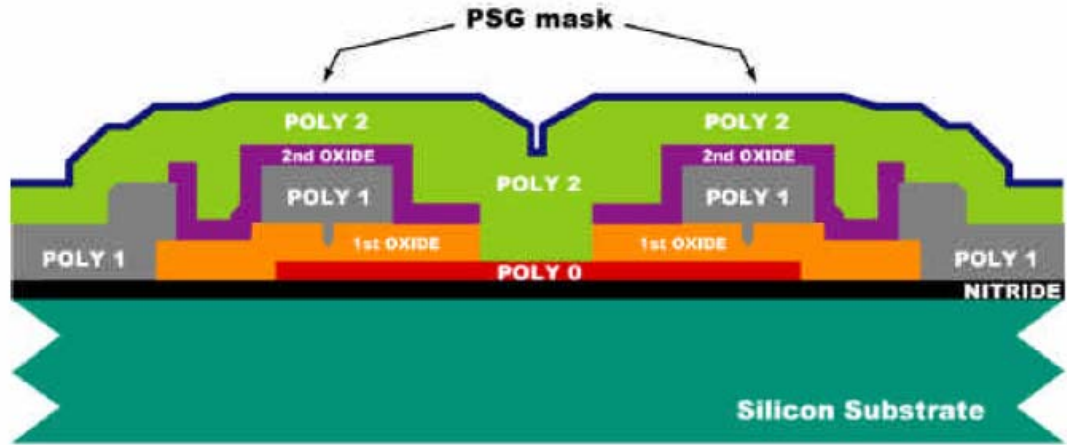


FIGURE 1.13. A 1.5 μm un-doped polysilicon layer is deposited followed by a 200 nm PSG hardmask layer. The wafers are annealed at 1050°C for one hour to dope the polysilicon and reduce residual stress.

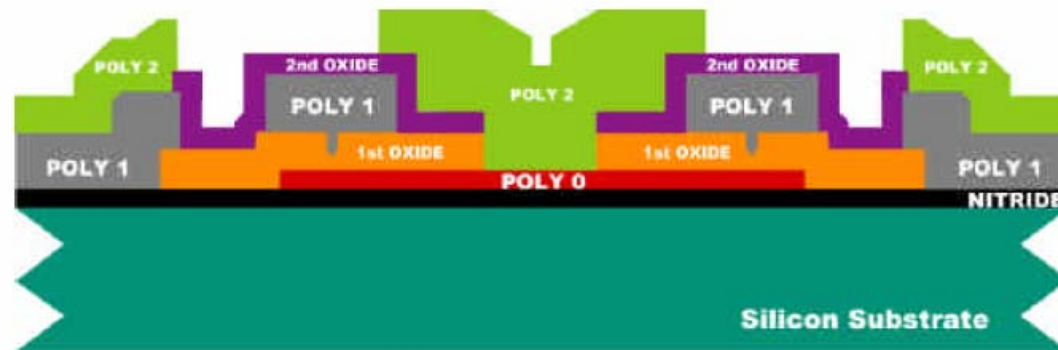


FIGURE 1.14. The wafer is coated with photoresist and the seventh level (POLY2) is lithographically patterned. The PSG hard mask and Poly 2 layers are RIE etched and the photoresist and hard mask are removed. All mechanical structures have now been fabricated. The remaining steps are to deposit the metal layer and remove the sacrificial oxides.

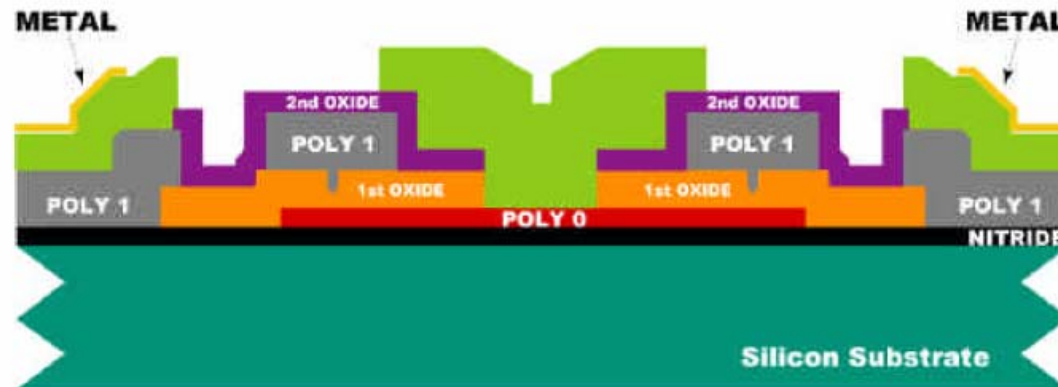


FIGURE 1.15. The wafer is coated with photoresist and the eighth level (METAL) is lithographically patterned. The metal (gold with a thin adhesion layer) is deposited by lift-off patterning which does not require etching. The side wall of the photoresist is sloped at a reentrant angle, which allows the metal to be deposited on the surfaces of the wafer and the photoresist, but provides breaks in the continuity of the metal over the reentrant photoresist step. The photoresist and unwanted metal (atop the photoresist) are then removed in a solvent bath. The process is now complete and the wafers can be coated with a protective layer of photoresist and diced. The chips are sorted and shipped.

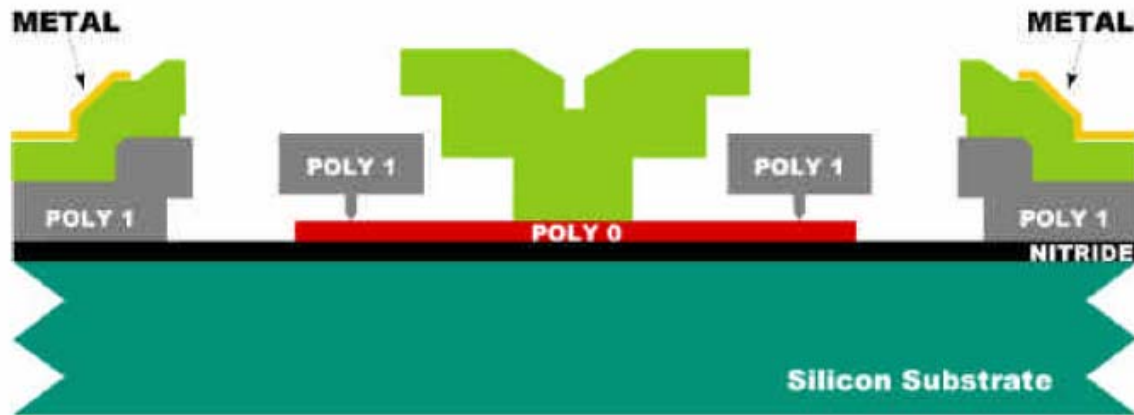
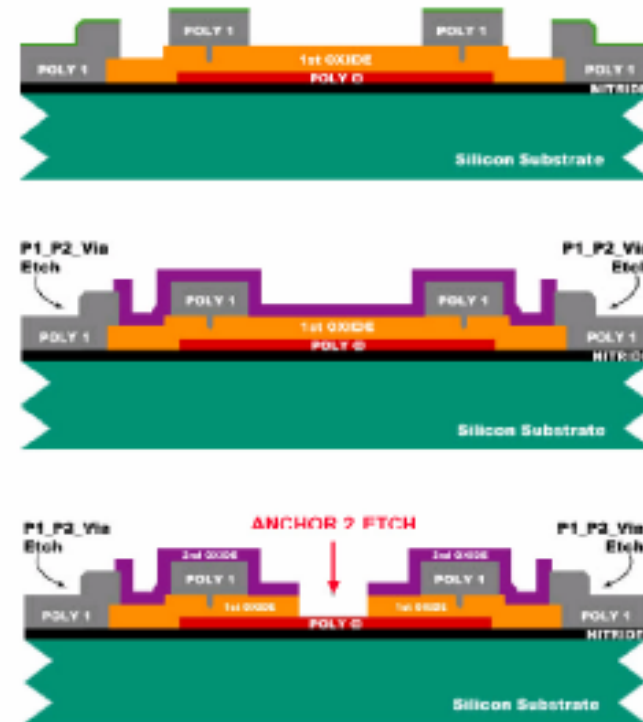
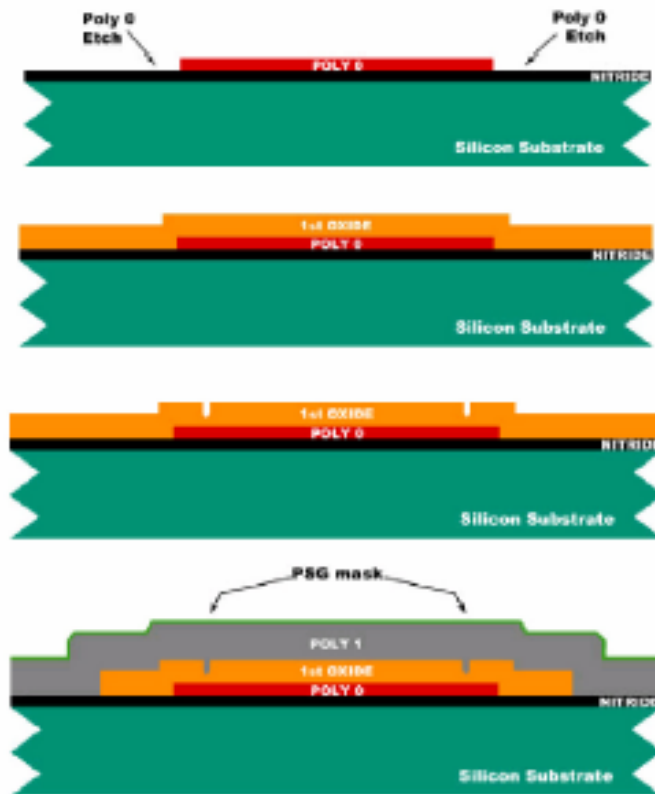


FIGURE 1.16. The structures are released by immersing the chips in a 49% HF solution. The Poly 1 “rotor” can be seen around the fixed Poly 2 hub. The stacks of Poly 1, Poly 2 and Metal on the sides represent the stators used to drive the motor electrostatically.

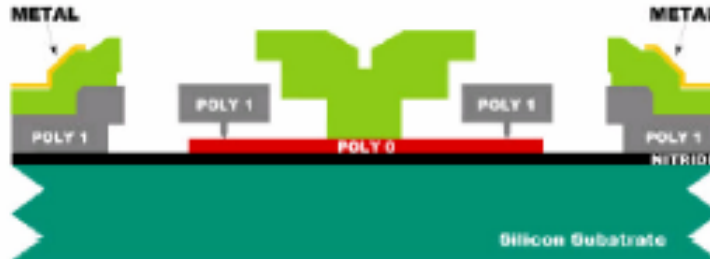
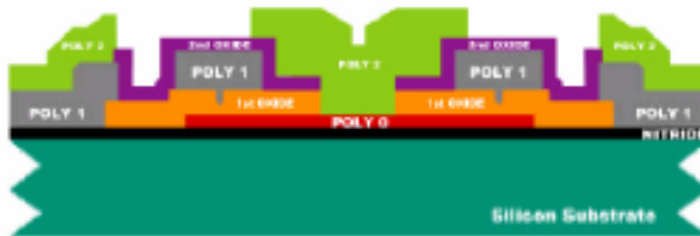
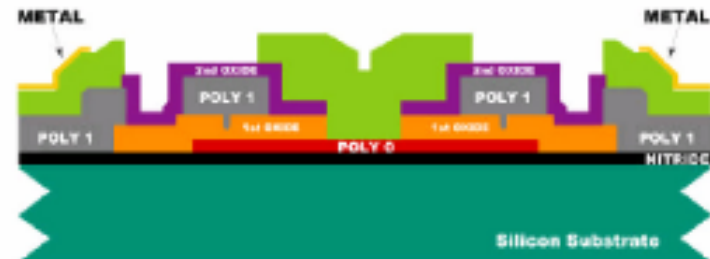
MUMPS Process Flow I



EE C245

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MUMPS Process Flow II



EE C245

Process highlights

- "Full MEMS" processing capabilities
- 100 & 150mm wafer diameter
- Automatic lithography lines
- PECVD deposition of Si_3N_4 and SiO_2
- Dry etching of Al, Poly-Si, Si_3N_4 and SiO_2
- Deep Reactive Ion Etching of silicon
- Wet etching of silicon
- Advanced wafer bonding technologies
- Deposition of Au, Al, Ni, NiCr, Ti, etc
- Automatic visual inspection
- Full automatic electric wafer test
- Wafer dicing



Processing equipment



■ Diffusion / oxidation furnaces

- Diffusion
- Annealing
- Oxidation
- LPCVD poly-Si
- LPCVD Si₃N₄
- POCl₃
- SiC tube for growth of extra thick oxide

Processing equipment



■ Automatic resist coaters

- Double sided coating
- fully automated



■ Mask aligners

- Contact / proximity printing
- Front to back-side alignment
- Throughput of 170 wafers / hour

Processing equipment

■ PECVD deposition

- Si_3N_4
- SiO_2
- Amorphous silicon

■ RIE etching

- Silicon (Bosch / Cryo)
- SiO_2
- Si_3N_4
- Poly - silicon
- Aluminum
- polyimide

