INF 5490 RF MEMS

LN12: RF MEMS inductors

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Today's lecture

- What is an inductor?
- MEMS -implemented inductors
- Modeling
- Different types of RF MEMS inductors
  - **Horizontal plane** inductors
  - Real **solenoids**
- How to increase performance
  - Q-value, Inductance (L), Self resonance frequency (f_max)
- Elevated inductors
- Inductor banks

What is an inductor?

- Inductor = a component with interaction between magnetic and electric flux
  - Magnetic field ←→ current

- Two basic laws
  - Faraday´s law
    - Varying **magnetic field** induces **current**
  - Ampere´s law
    - **Current** flowing sets up a **magnetic field**

Faraday´s law

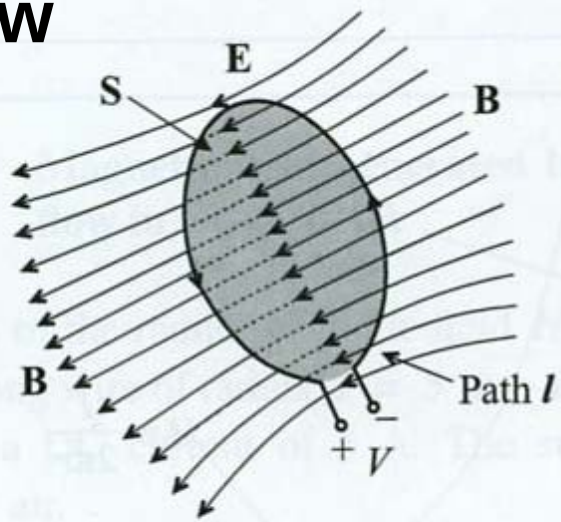


Figure 2-15 The time rate of change of the magnetic flux density induces a voltage.

$$\oint \bar{E} \cdot d\bar{l} = -\frac{d}{dt} \iint \bar{B} \cdot d\bar{S}$$

$\bar{B}$ = magnetisk fluks-tetthet — **magnetic flux density**

$$\bar{B} = \mu \cdot \bar{H}$$

μ = permeabilitet $= \mu_0 \cdot \mu_r$ — **permeability**

$\bar{H}$ = magnetfelt — **magnetic field**

Ampere´s law

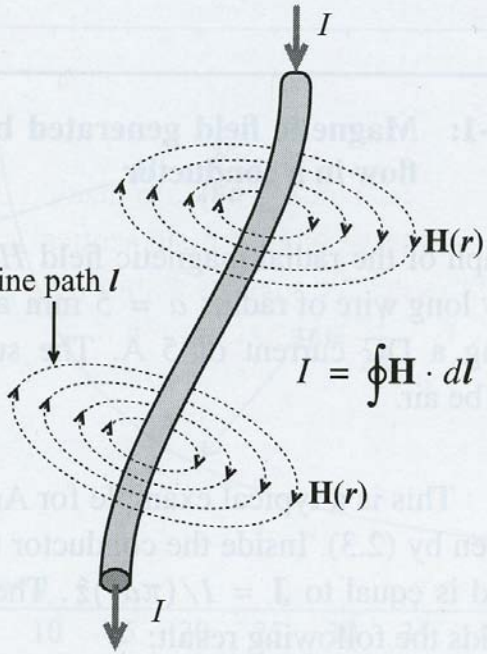


Figure 2-13 Ampère's law linking the current flow to the magnetic field.

$$I = \oint \bar{H} \cdot d\bar{l} = \iint \bar{J} \cdot d\bar{S}$$

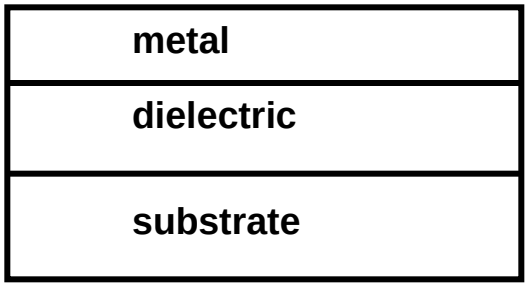
Inductors follow **Faraday´s/Ampere´s laws**

- Change of current in inductor →
- Change of magnetic field (Ampere´s law) →
- Electric field induced (Faraday´s law) →
- The induced electric field opposes further change in current (Lenz law)
  - **Inertia** with respect to variation: **”reactance”**
  - Mechanical analogy: **mass!**

Inductors

- Generally implemented as **solenoids**
  - 2D (in plane) or 3D
  - Several turns used to increase magnetic flux density
    - May give large inductance, L, for a small area/volume

- Basic equations
  - V = L dI/dt
  - V = Ls * I (Laplace)



- Solenoids in **plane** are typical for IC and MEMS

Competition from IC

- Standard **CMOS, SiGe-technology** has given good results!
  - F.ex. Q = 12–18 @ 2 GHz, 16–22 @ 6 GHz (2003)

- Reasons for the increased IC-component performance which has been obtained
  - Optimized **inductor geometry** due to good CAD tools
  - Using **thick metal layers** of gold (3 µm)
  - Using **thick dielectric** (3-6 µm oxide over substrate)
  - Using **high resistivity substrate,** 10-2000 ohm-cm
    - Reducing ”eddy currents” = magnetic induced currents
    - Thereby reducing substrate loss underneath the inductor

Any reason for RF MEMS inductors?

- Micromachined inductors should have better performance than todays CMOS inductors
  - MEMS may give **higher Q-values!**
    - **Q>30**
  - MEMS may give higher **L** and self resonance-frequency

L → L, C, R -circuit

- Should be CMOS compatible
  - F.ex. post processing CMOS

- Micromachined inductances not yet a commercial product

Applications of (RF MEMS) inductors

- Replacement components in
  - Low noise oscillators
  - Integrated LC-filters
  - Amplifiers
  - On-chip ”matching” networks
  - Impedance transformers
  - Phase shifters

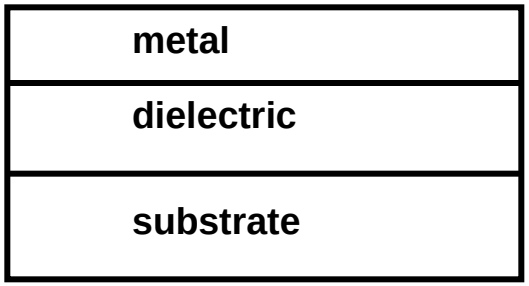
RF MEMS inductors

- Two-dimensional (planar) inductors
- Three-dimensional inductors, solenoids

- Only fixed-value inductors can be implemented
  - No practical implementation of tunable inductors exist
- Variable inductance values: implemented as an **inductor bank**
  - Many inductors with fixed, high Q-values
  - In combination with MEMS contact switches

Planar inductors, in general

- Implemented in a single plane
- One **metal layer** patterned by etching
- Inductor rests on a **substrate** covered by a **dielectric**
- **Loss** in inductor due to:
  - Finite metal conductivity
  - Loss in dielectric
  - Loss in substrate
- Area limitations for RF
  - Total length of an inductor has to be significantly shorter than the wavelength
    - This will give negligible phase shift of signal



Different planar geometries

- Simple **line sections**
  - Each one has a low inductance value, nH
- **Meander**
  - Coupling by negative mutual inductances
- **Spiral inductors**
  - Increasing inductance, L
  - **Problem**: connecting to the inner winding
    - Wire bonding
    - Separate structure layer
    - Flip-chip bonding methods

Contribution to inductance

- **Self inductance** from its own winding
- **Mutual inductance** from neighbouring windings
  - Mutual coupling between neighbour lines
- Total inductance is the sum of self inductance and mutual inductance
  - In some elements current flows in the same direction, in others opposite

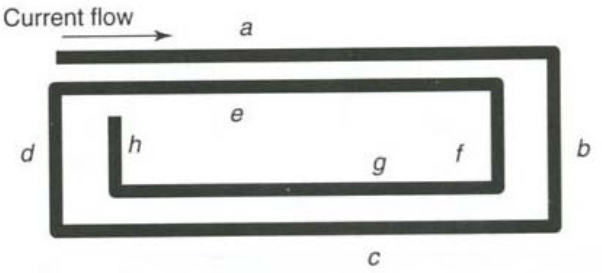


Figure 4.2 Spiral inductor and the effect of current flow in nearby segments

Different planar geometries

- Distance between lines is critical
- Circular spiral has a shorter length than a quadratic spiral
  - → Lower R
  - Q is about 10% higher with same ”diameter”, d_0
- Higher Q achieved by increasing number of turns per area
  - Self resonance frequency decreases due to the increase in capacitance → limits the region of use

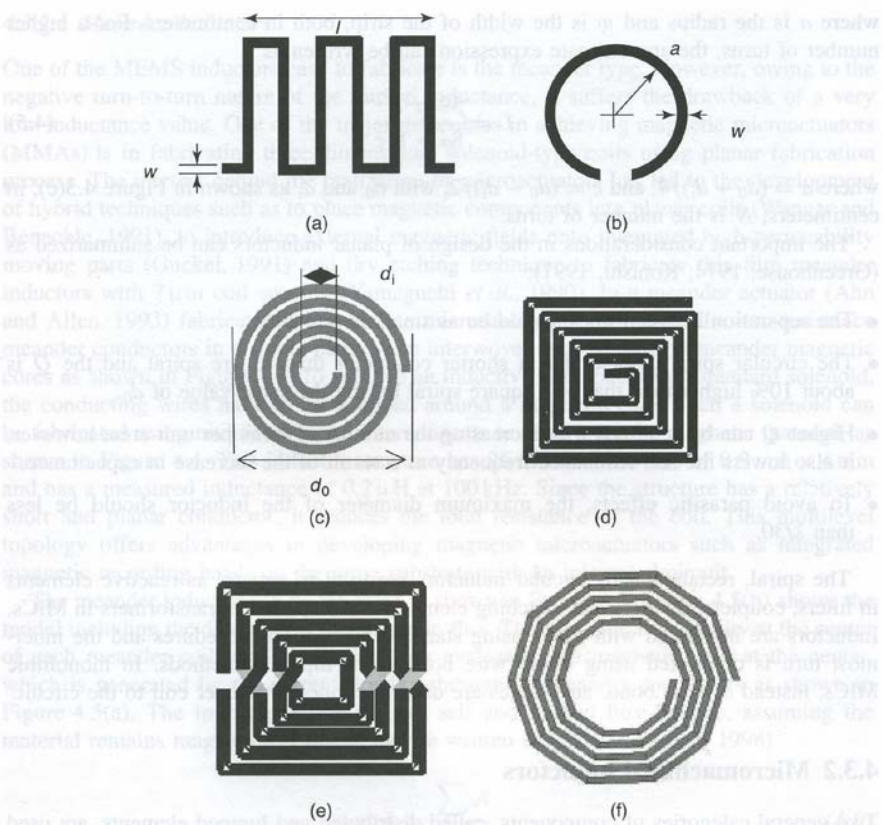


Figure 4.3 Schematic diagram of common planar inductors: (a) meander; (b) loop; (c) circular spiral; (d) square spiral; (e) symmetric spiral; (f) polygon spiral

Inductor is a non-ideal component

- Changes its value versus frequency
  - Becomes capacitive at high frequencies

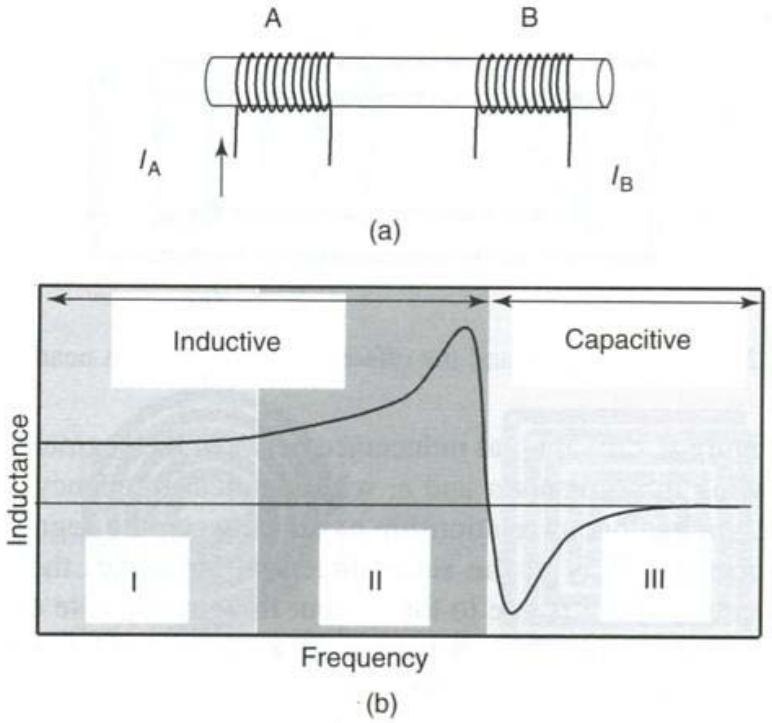


Figure 4.1 (a) Self-inductance and mutual inductance due to a change in current; (b) typical operational regions of an inductor. Note: I_A and I_B, current in coils A and B, respectively

General model for a planar inductor

Ls is low frequency inductance

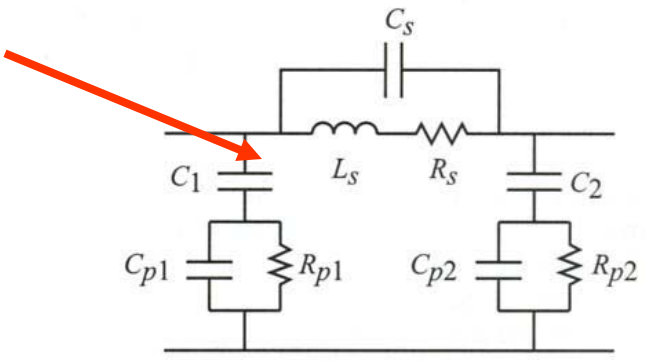
Rs is series resistance

Cs is capacitance between windings

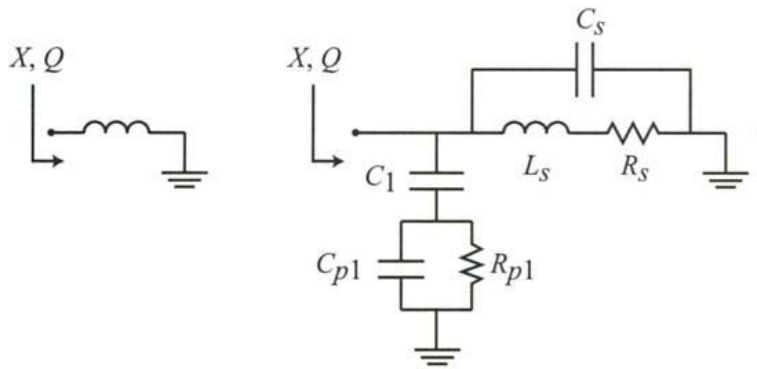
C1 is capacitance in oxide layer between inductor and substrate

Cp is capacitance to ground through substrate

Rp is **"eddy current"** loss in substrate



(a)



(b)

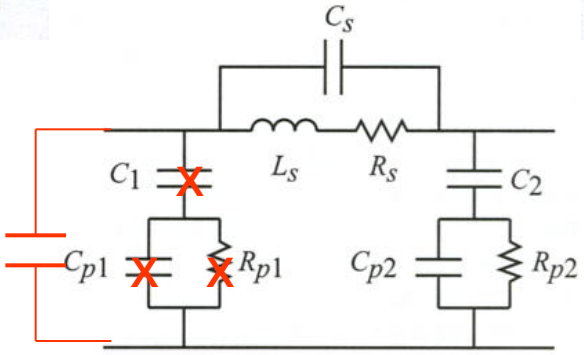
Figure 12.1. (a) The equivalent LRC model of a planar inductor. (b) A short-circuited inductor model typically used in *S*-parameter and *Q* measurements. C_{p1} and C_{p2} are often assumed identical and equal to C_p.

Frequency response for a planar inductor

- At low frequencies we have

$$Z = R_s + j\omega L_s \qquad (12.1)$$

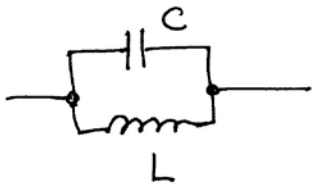
- At high frequencies:
  - Rp1 is negligible
  - C1 and Cp1 combined → Cp



$$Z = (R_s + j\omega L_s) \left\| \left(\frac{1}{\omega C_s}\right) \right\| \left\{ \frac{1}{\omega C_1} + \left(\frac{1}{\omega C_{p1}} \| R_{p1} \right) \right\} \qquad (12.2)$$

Parallel resonator

Parallell resonans



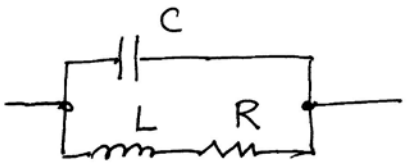
$$Z = \frac{\frac{1}{j\omega C} \cdot j\omega L}{\frac{1}{j\omega C} + j\omega L}$$

Resonans när $\frac{1}{\omega C} = \omega L$

$$\frac{1}{j\omega C} + j\omega L = 0$$

$$Z = \infty$$

Due to parasitic capacitances a specific self resonance frequency is obtained



$$Z = \frac{\frac{1}{j\omega C} \cdot (R + j\omega L)}{\frac{1}{j\omega C} + R + j\omega L} = \frac{-j\omega L\,(R + j\omega L)}{R}$$

$$\Downarrow -j\omega L$$

Q_ind = ωL/R

At resonance:

$$Z = \frac{\omega^2 L^2}{R} - j\omega L \approx \frac{\omega^2 L^2}{R}$$

Ex.: Inductor reactance

Resistance is here defined at 2 GHz

R is supposed to vary as **sqrt (f)** above 2 GHz due to the skin effect

Parallel-type resonance at 8 GHz, phase also changes

At resonance the input impedance of a parallel resonator is real and given by:

$$Z_{res} = \frac{(\omega L_s)^2}{R_s} \qquad (12.3)$$

Figure shows that simple L, R – model is valid to 0.5 f_resonance

Phase properties show that the component is inductive also for higher frequencies →

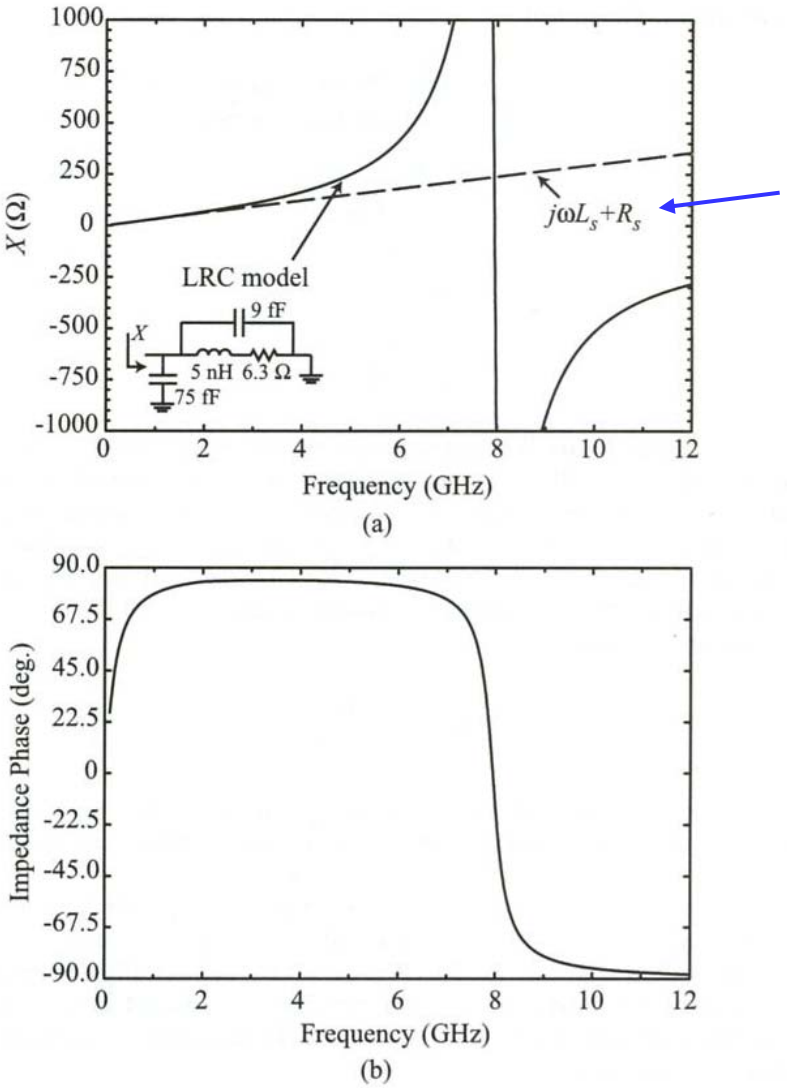


Figure 12.2. The calculated X (a) and phase (b) of a planar 5-nH inductor. The resonant frequency is 8 GHz and the resistance is assumed constant up to 2 GHz and then increases as $\sqrt{f}$.

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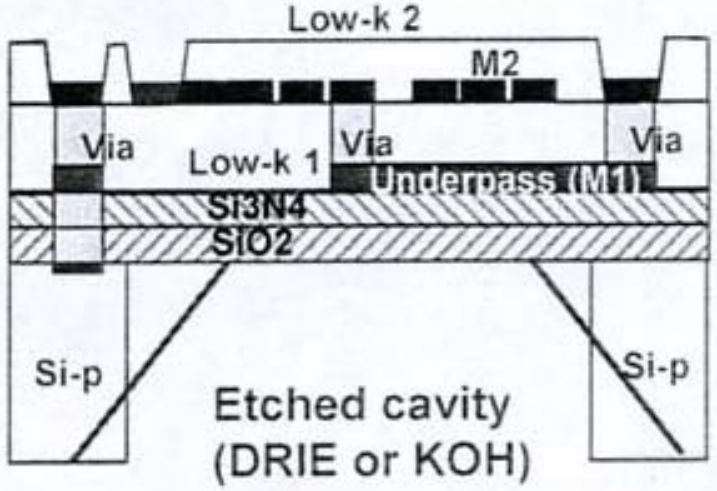
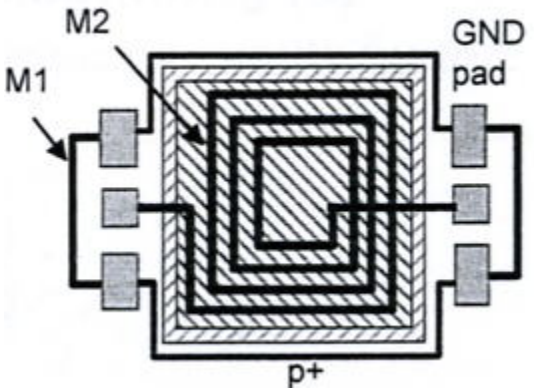
Example: Thick copper/polyimide horizontal-plane inductor

Process (EPF Lausanne, WIDE-RF):

- 4-8μm electroplated Cu in polyimide mold using Ta barriers





”Form” (”mold”) of organic material

Ex. CMOS – MEMS inductor

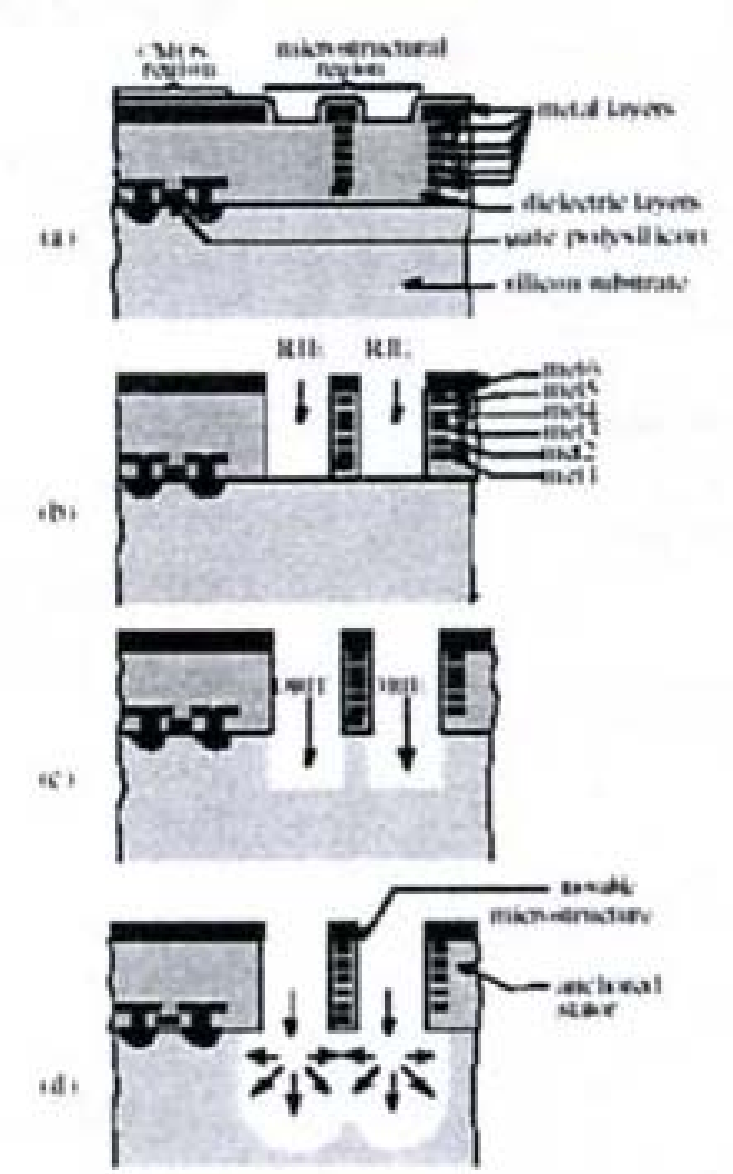
- High Q, 6 Cu layers
- Low-ε dielectric
- Post-CMOS processing
  - Standard CMOS + RIE post processing + isotropic etch

- X. Zhu et al

Carnegie Mellon University
Ex. from Transducers 2001

Anisotropic etching followed by isotropic etching

Top metal layer is mask



Ex. Spiral inductor (Ahn & Allen)

- Two solenoids
- **Magnetic core** used for trapping magnetic flux
  - Must be a high permeability material
  - Ex. Varadan fig. 4.7 (Ahn & Allen) →
- Conductor from centre needed!

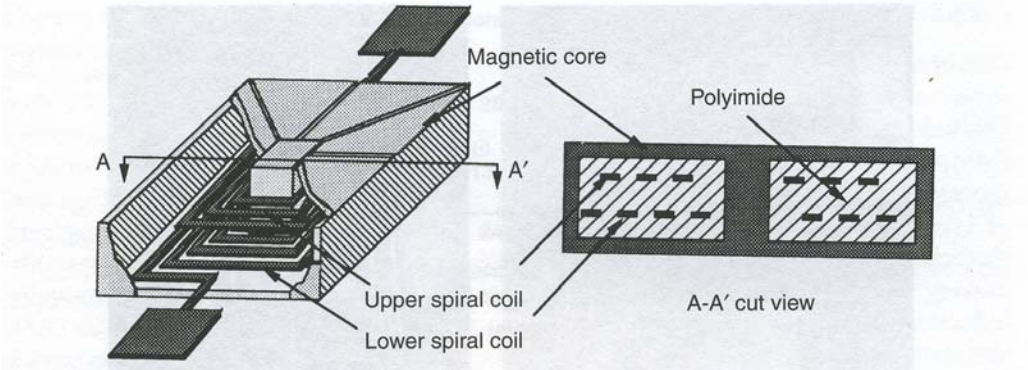
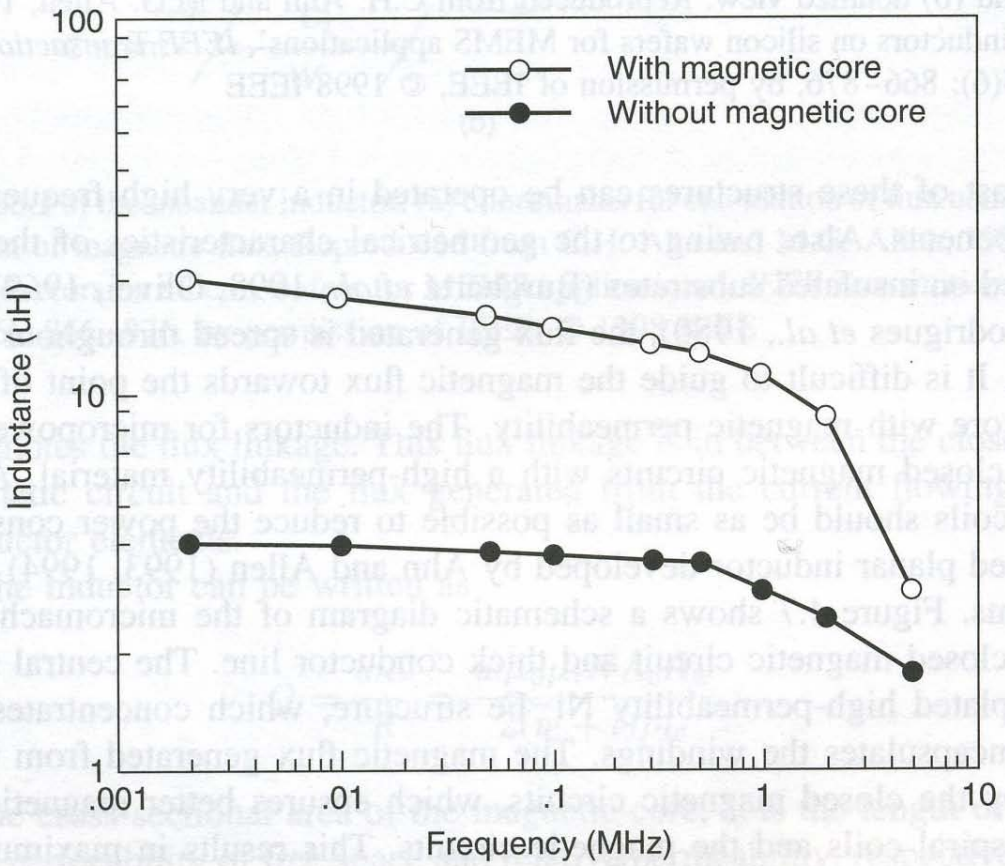


Figure 4.7 Schematic diagram of a micromachined spiral inductor. Reproduced from C.H. Ahn and M.G. Allen, 1993, 'A planar micromachined spiral inductor for integrated magnetic microactuator applications', *Journal of Micromechanics Microengineering* **3**: 37–44, by permission of the Institute of Physics

Effect of magnetic core



Magnetic core increases inductance

Figure 4.8 Measured inductance with and without magnetic core. Reproduced from C.H. Ahn and M.G. Allen, 1993, 'A planar micromachined spiral inductor for integrated magnetic microactuator applications', *Journal of Micromechanics Microengineering* **3**: 37–44, by permission of the Institute of Physics

Meander inductors

- Meander has lower inductance than spiral inductor
- Meander fabricated by surface processing
  - a) Metal conductor in one layer
    - Penetrated by multilevel magnetic core
  - b) Schematic of principle →
    - Ala magnetic core in one layer surrounded by metal turns

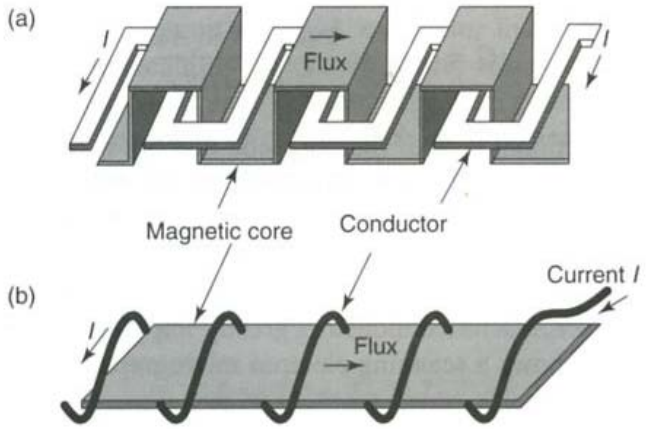


Figure 4.4 Schematic diagram of the micromachined multilevel meander inductor. Reproduced from C.H. Ahn and M.G. Allen, 1998, 'A fully integrated surface micromachined microactuator with a multilevel meander magnetic core', *Journal of Microelectromechanical Systems* **2**(1): 15–22, by permission of IEEE, © 1998 IEEE

Meander fabricated (SEM picture)

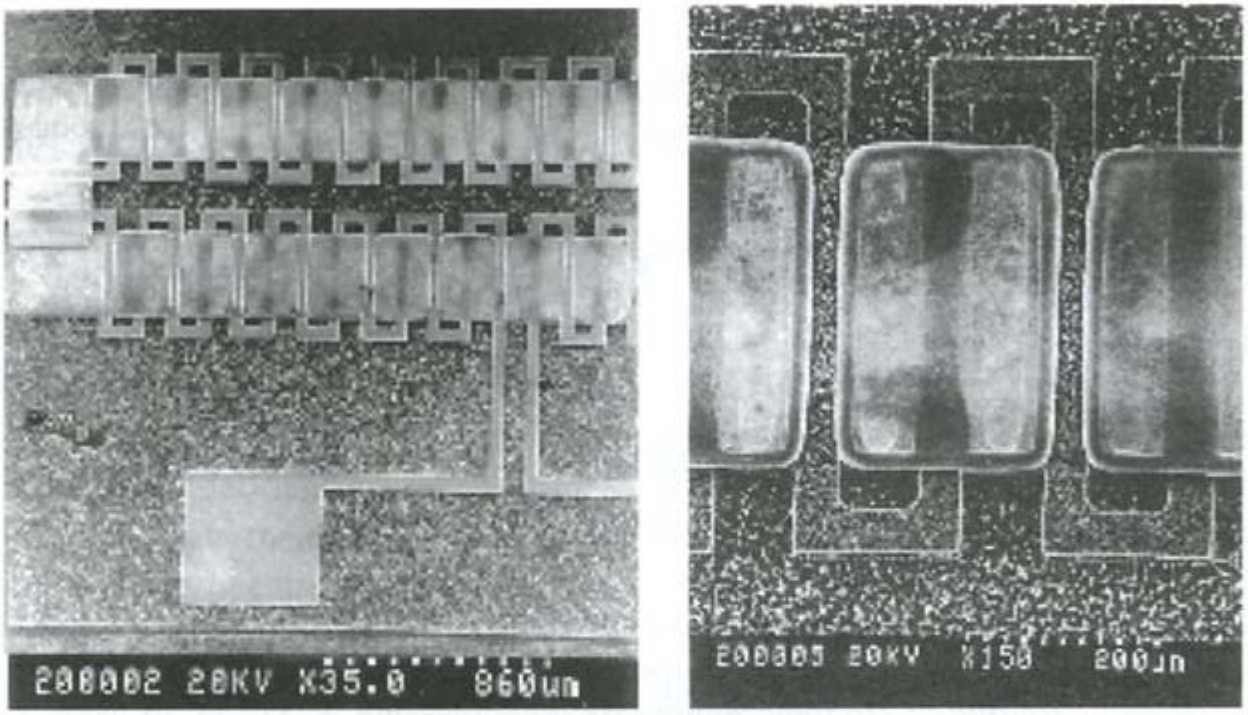


Figure 4.6 Scanning electron micrograph of the fabricated toroidal-meander inductor: (a) half of the inductor and (b) detailed view. Reproduced from C.H. Ahn and M.G. Allen, 1998, 'Micromachined planar inductors on silicon wafers for MEMS applications', *IEEE Transactions on Industrial Electronics* **45**(6): 866–876, by permission of IEEE, © 1998 IEEE

Meander: effect of different line widths

- Influence of the line width (C vs width)
  - ”sheet resistance” is inversely proportional to w → decreases!
  - Resistance decreases if w increases, but the capacitance increases

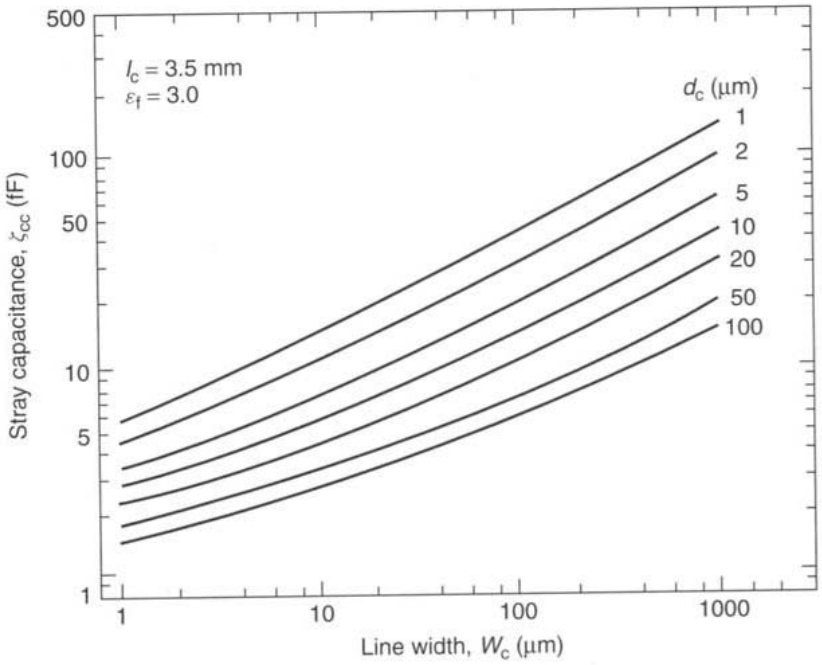
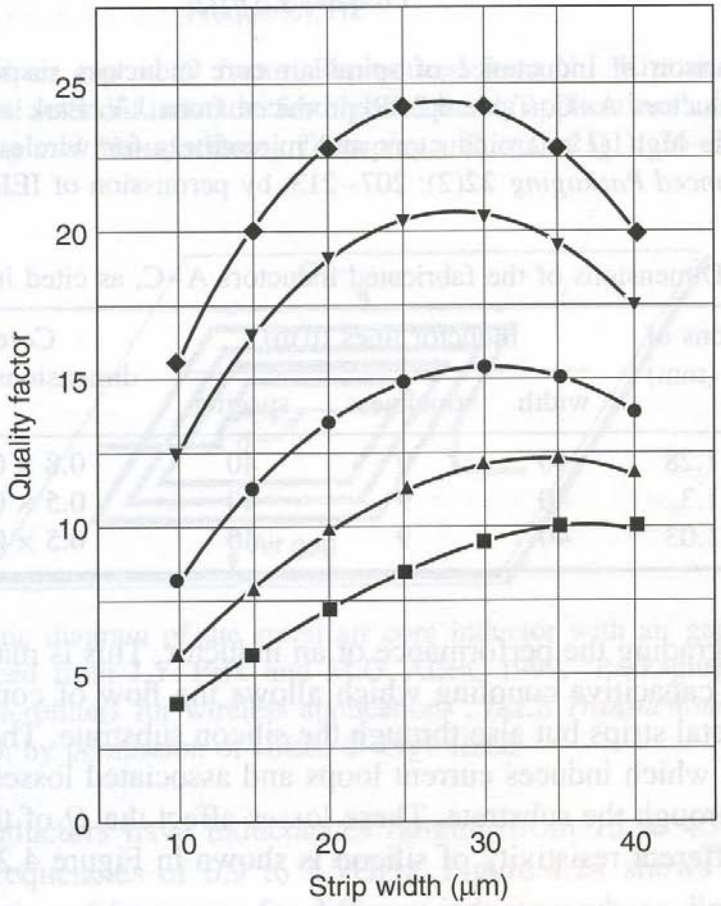


Figure 4.11 Computed stray capacitance due to change in line width W_c. Reproduced from M. Yamaguchi, M. Mastumo, H. Ohzeki and K.I. Arai, 1991, ‘Analysis of the inductance and the stray capacitance of the dry-etched micro inductors’, *IEEE Transactions on Magnetics* **27**(6): 5274–5276, by permission of IEEE, © 1991 IEEE

dc = distance between conductors (line spacing)

Effect of stripe width w on Q-factor



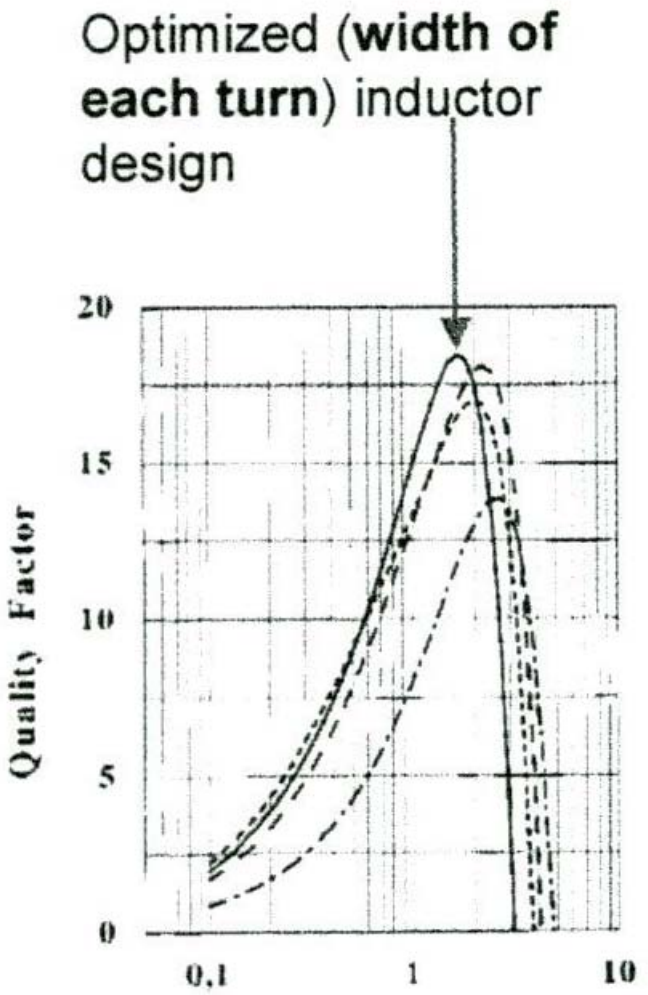
Different frequencies

Optimal values of w exist for minimizing series resistance and maximizing Q

Figure 4.26 Change in Q due to change in strip width for 20-nH inductors for different frequencies: ■, 7 GHz; ▲, 1 GHz; ●, 1.5 GHz; ▼, 2.5 GHz; and ◆, 3.5 GHz. Reproduced from I.J. Bahl, 1999, 'Improved quality factor spiral inductors on GaAs substrates', *IEEE Microwave and Guided Wave Letters* **9**(10): 398–400, by permission of IEEE, © 1999 IEEE

Optimization

- Width of each turn can be optimized
  - Each turn has a constant resistance



Effect of different implementations

- How **line spacing** influences L

Line spacing has different effect for spiral and meander: constructive versus destructive mutual inductance

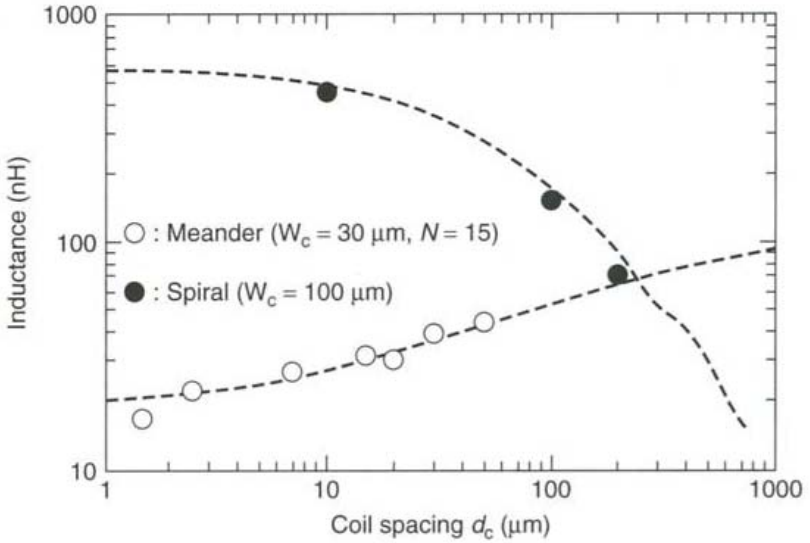


Figure 4.10 Change in inductance arising from changes in spacing between the conductors for meander and spiral inductors. Reproduced from M. Yamaguchi, M. Mastumo, H. Ohzeki and K.I. Arai, 1991, 'Analysis of the inductance and the stray capacitance of the dry-etched micro inductors', *IEEE Transactions on Magnetics* **27**(6): 5274–5276, by permission of IEEE, © 1991 IEEE

- Effect of number of turns on L and Q
- **Spiral** inductors with same dimensions

- n: 3 → 8:
  - L increases
  - Q decreases (due to increase in C)
  - f_max decreases

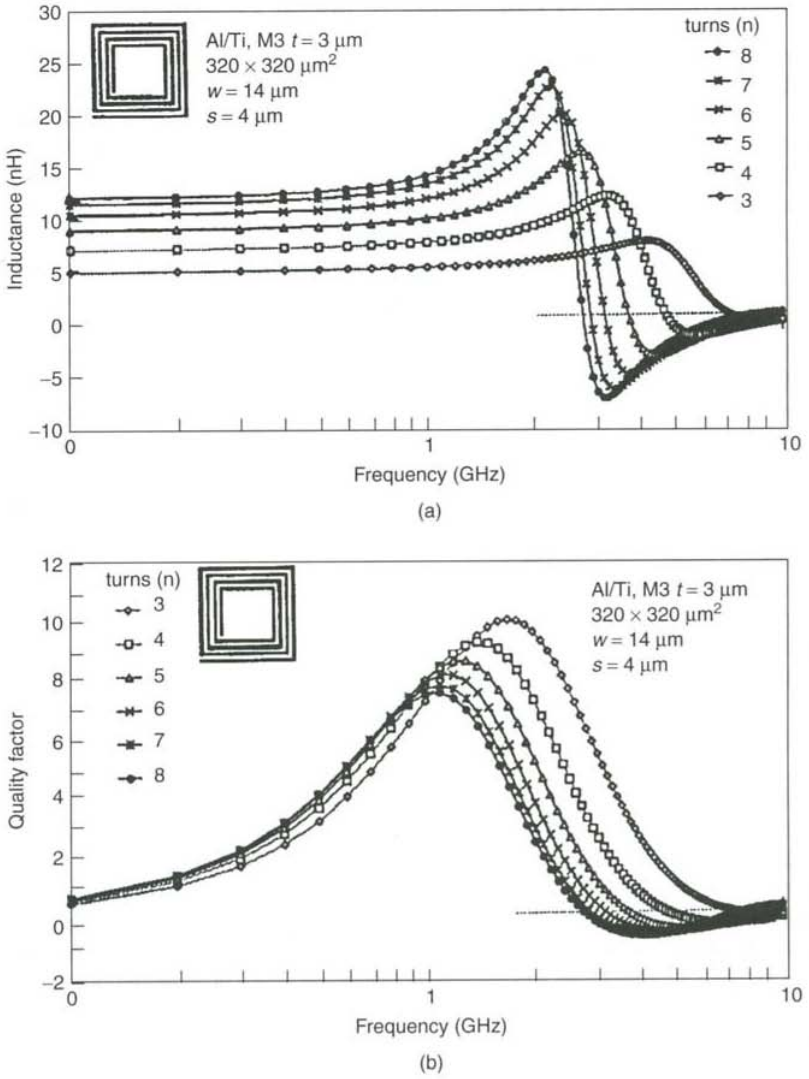
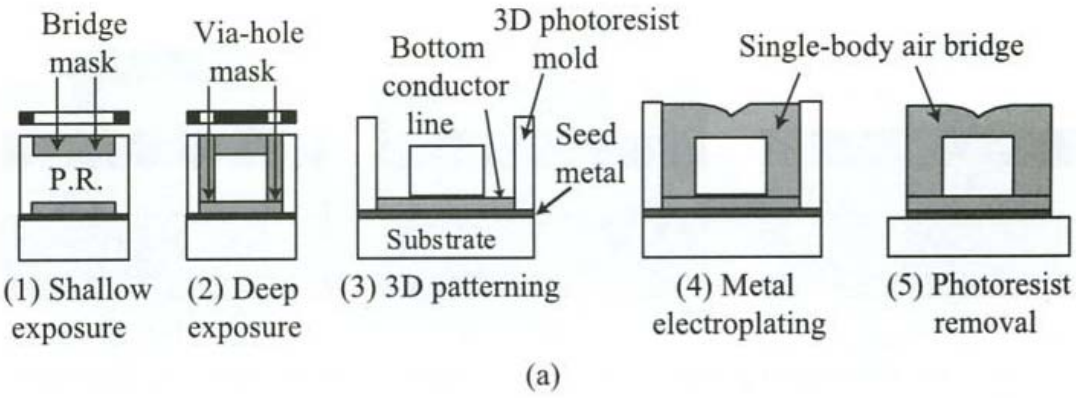
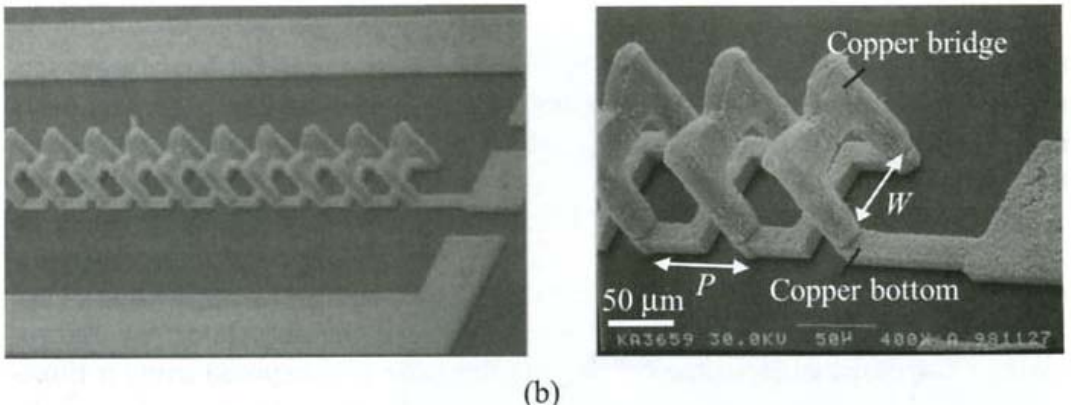


Figure 4.12 Effect of number of turns on (a) the inductance value and (b) Q factor. Reproduced from Y.K. Koutsoyannopoulos and Y. Papananos, 2000, 'Systematic analysis and modeling of integrated inductors and transformers in RF IC design', *IEEE Transactions on Circuits and Systems II* **47**(8): 699–713, by permission of IEEE, © 2000 IEEE

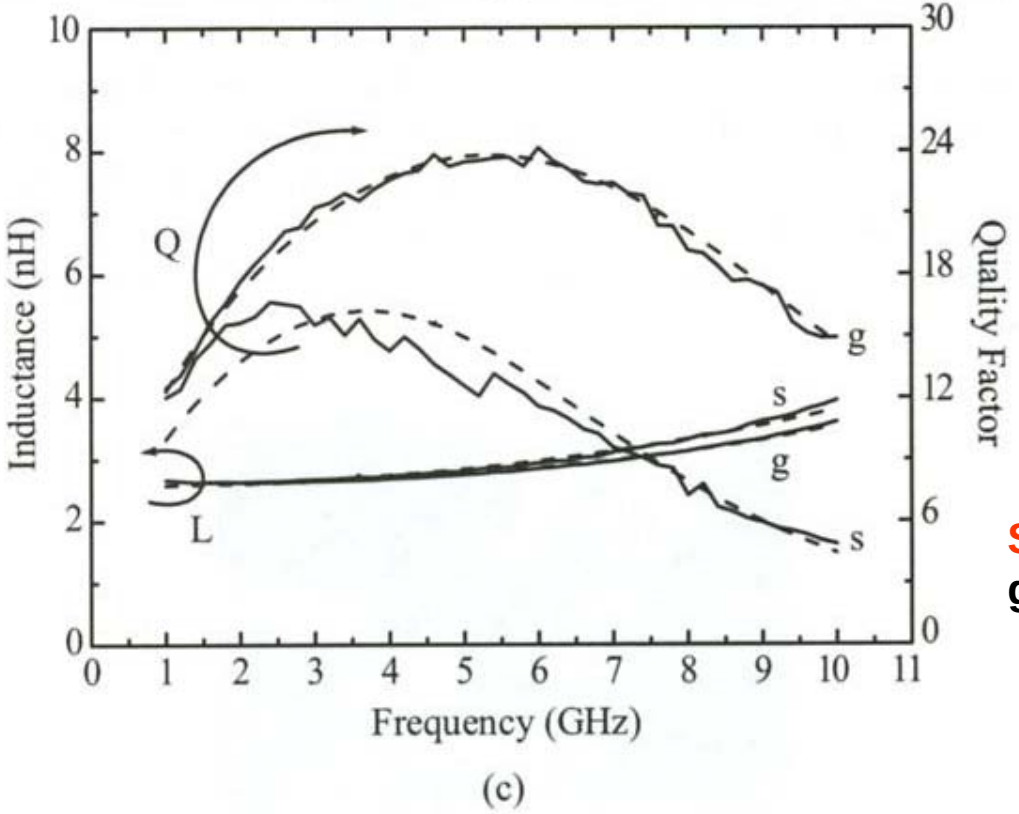
Solenoid-type inductors

- Classical example
- Process using thick **photoresist mold**
  - 45 – 60 μm deep
- Top fabricated using copper: **electroplating**
  - seed + 20 – 30 μm copper layer plated on top
- Result: ”loops” formed





Solenoid-type copper inductors



(c)

Figure 12.14. Fabrication process (a), picture (b), and measured performance (c) of a 2.4-nH all-copper solenoid inductor on silicon and glass substrates [24, 25] (Copyright IEEE).

Si or glass substrate give different values

Results from Yoon et al.

Extreme type

- Solenoid-type inductor with large alumina core
  - Placed **manually** on a Si-substrate, fig. →
    - Cross section 650 x 500 µm2
  - Photo resist on alumina core
  - Direct write laser, 3D
  - Electroplating
    - 5-10 µm copper
  - **Not practical!**

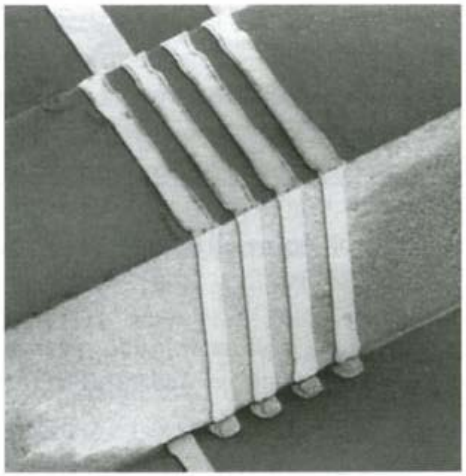


Figure 12.16. A solenoid-type four-turn inductor using a large alumina core [28] (Copyright IEEE).

Young et al., 1997

Example of 3-D structure

- Difficult to produce
  - Nickel-iron (permalloy) magnetic core
  - Multilevel copper + via-contacts
  - Contacts have high contact resistance
  - Need of many turns to get high L
    - More contacts → higher resistance
    - Electroplating of metal lines and via holes may reduce resistance and increase performance

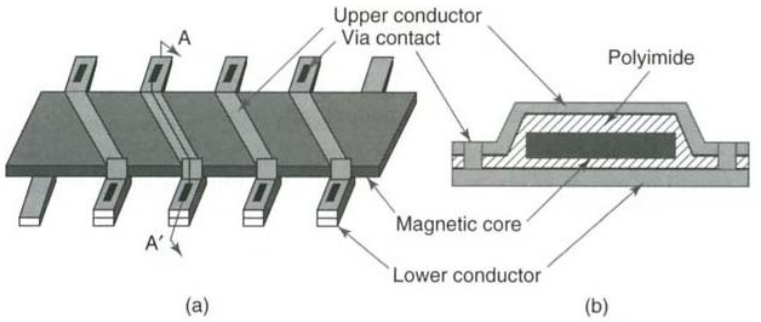


Figure 4.9 Schematic diagram of a solenoid-type inductor: (a) schematic view; (b) cross-sectional view at AA′. Reproduced from C.H. Ahn and M.G. Allen, 1998, 'Micromachined planar inductors on silicon wafers for MEMS applications', *IEEE Transactions on Industrial Electronics* **45**(6): 866–876, by permission of IEEE, © 1998 IEEE

Ahn & Allen, 1998

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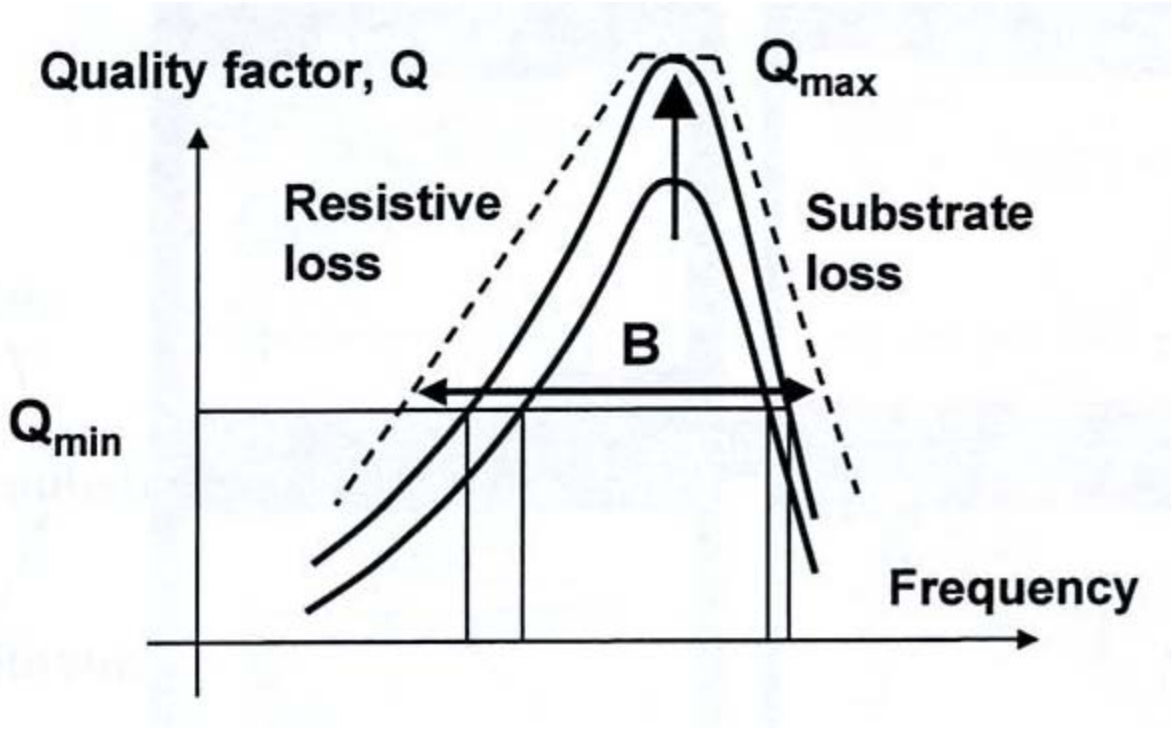
  - Real **solenoids**
- How to increase performance
  - Q-value, Inductance (L), Self resonance frequency (f_max)
- Elevated inductors
- Inductor banks

Q-factor depends on resistive loss and substrate loss



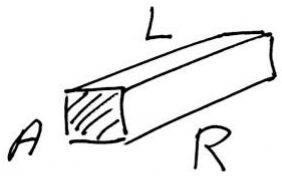
For low frequencies: resistive loss limits Q
For high frequencies: substrate loss limits Q

Improving Q-factor

- Metallization is important
  - Reduction of resistive loss!
  - Use metals with higher conductivity
    - Use copper, Cu, instead of Al
  - Use thicker structures

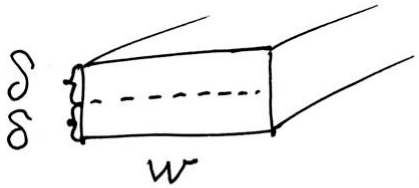
Effect of metal thickness

- Series resistance limits performance
- Simulations show that minimum thickness of **2 x ”skin depth”** is needed to obtain minimum resistance



ρ = **resistivity**

$$R = \frac{\rho \cdot L}{A}$$



Resistance per length

$$\frac{R}{L} = \frac{\rho}{A} = \frac{\rho}{2\delta \cdot w}$$

skin depth = δ

$$\delta = \sqrt{\frac{\rho}{\pi \mu \cdot f}} \sim \frac{1}{\sqrt{f}}$$

μ = permeability
ρ = resistivity

$$\frac{R}{L} \sim \frac{1}{\delta} \sim \sqrt{f}$$

Thick conductors needed

- For copper at 1 GHz: skin depth is about 2 μm
- One should have conductors of min 2 x skin depth thickness
  - E.g. about 4 - 5 μm for Cu
  - Thick layer!
  - Typically obtained by **electroplating**

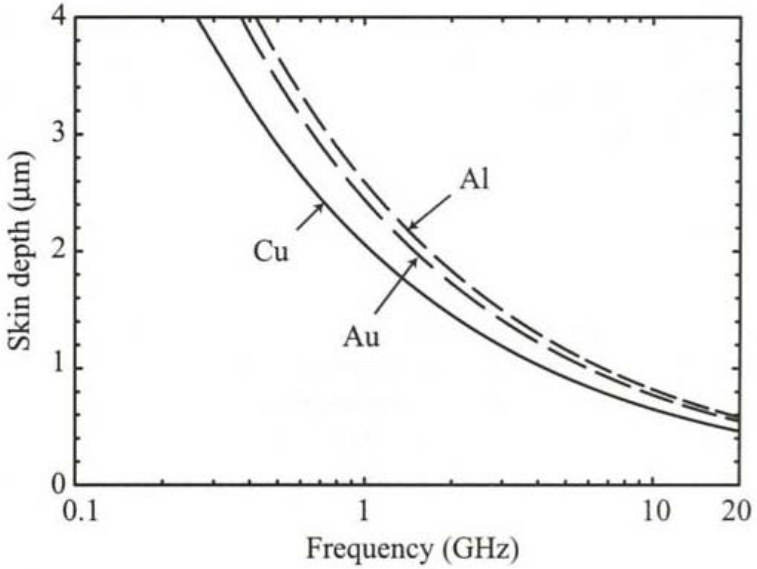


Figure 12.4. Skin depth versus frequency for copper, gold, and aluminum metal layer (bulk values of resistivities are assumed).

Change of Q versus metal thickness

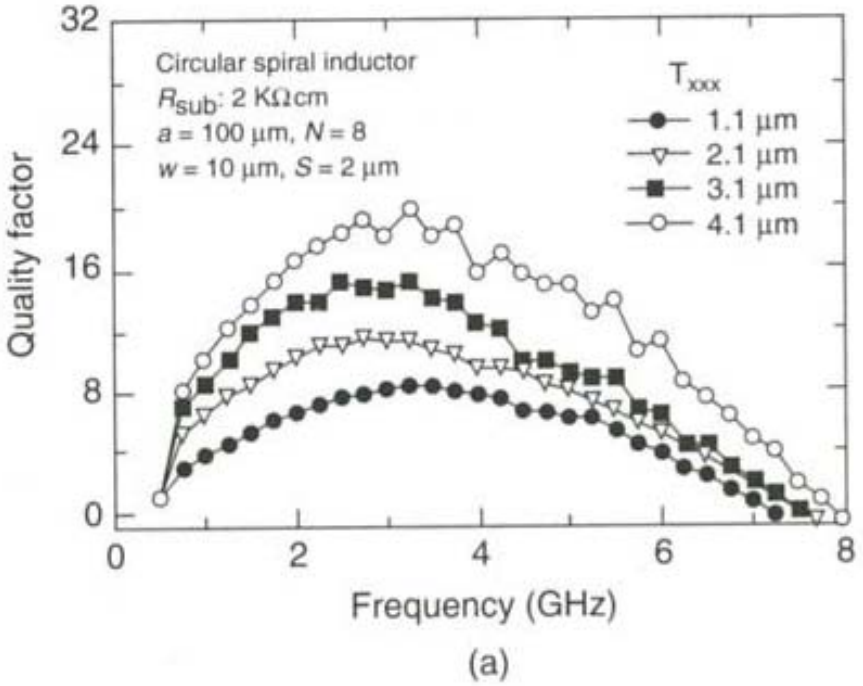


Figure 4.29 Change in Q of an inductor for (a) different metal thickness; (b) for substrates with different resistivity. Reproduced from M. Park, C.S. Kin, J.M. Park, H.K. Yu and K.S. Nam, 1997b, 'High Q microwave inductors in CMOS double metal technology and its substrate bias effects for 2 GHz RF IC application', in *Proceedings of IEDM 97*, IEEE, Washington, DC: 59–62, by permission of IEEE, © 1997 IEEE

Double level metallization

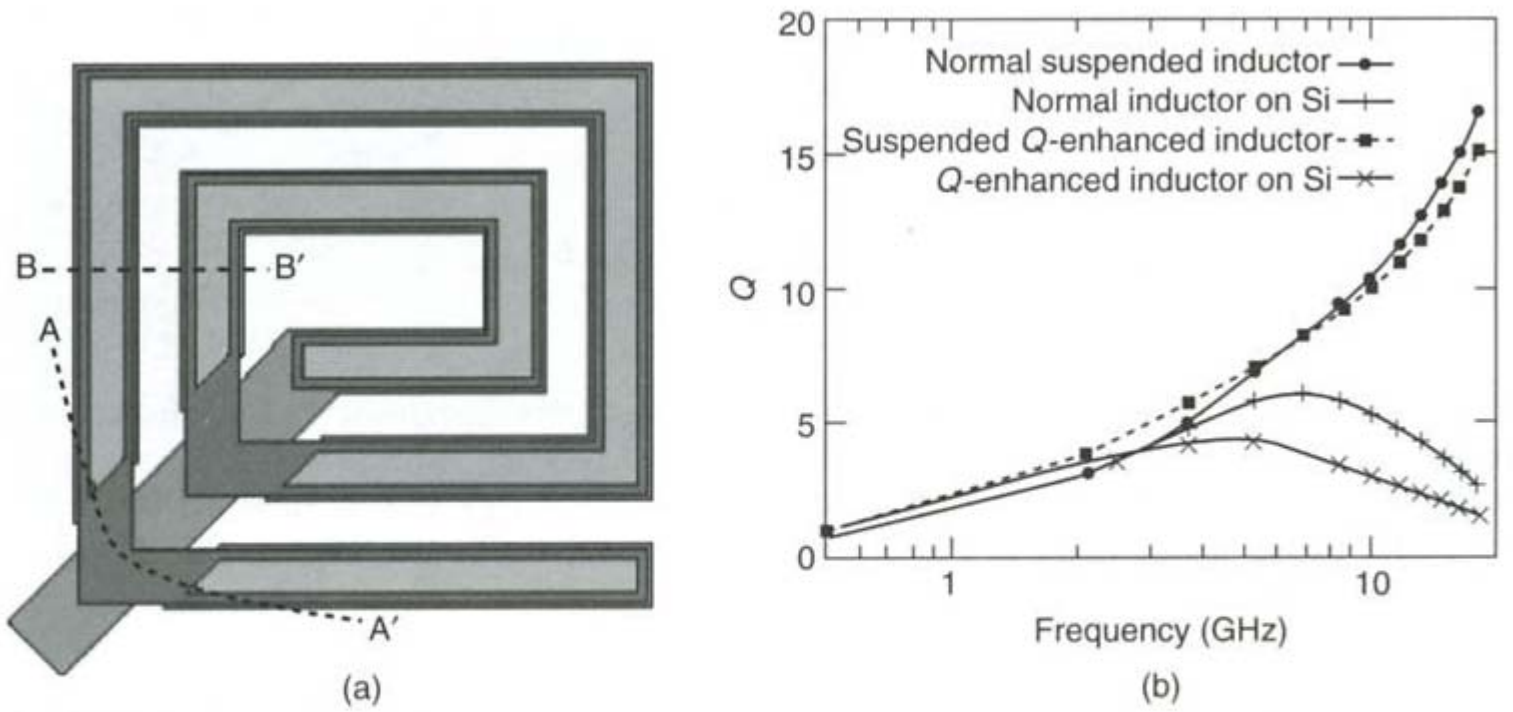


Figure 4.27 (a) Schematic diagram of a Q-enhance inductor; (b) measured results of normal and Q-enhanced inductors. Reproduced from Y. Sun, J.L. Tauritz and R.G.F. Baets, 1999, 'Micromachined RF passive components and their applications in MMICs', *International Journal of RF and Microwave CAE* **9**: 310–25, © Wiley (1999), by permission of Wiley

4.5 µm → 9 µm ("normal/Q-enhanced")
with/without 10 µm polyimide layer ("suspended/on Si")

Example:

Micromachining using **thick metal layers**

Thick **BCB layer** (Benzocyclobutene, low ε dielectric, polymer)
10 μm thick copper-layer

Post-CMOS, low-temperature processing

The thick copper layer is beneficial relative to the skin depth value

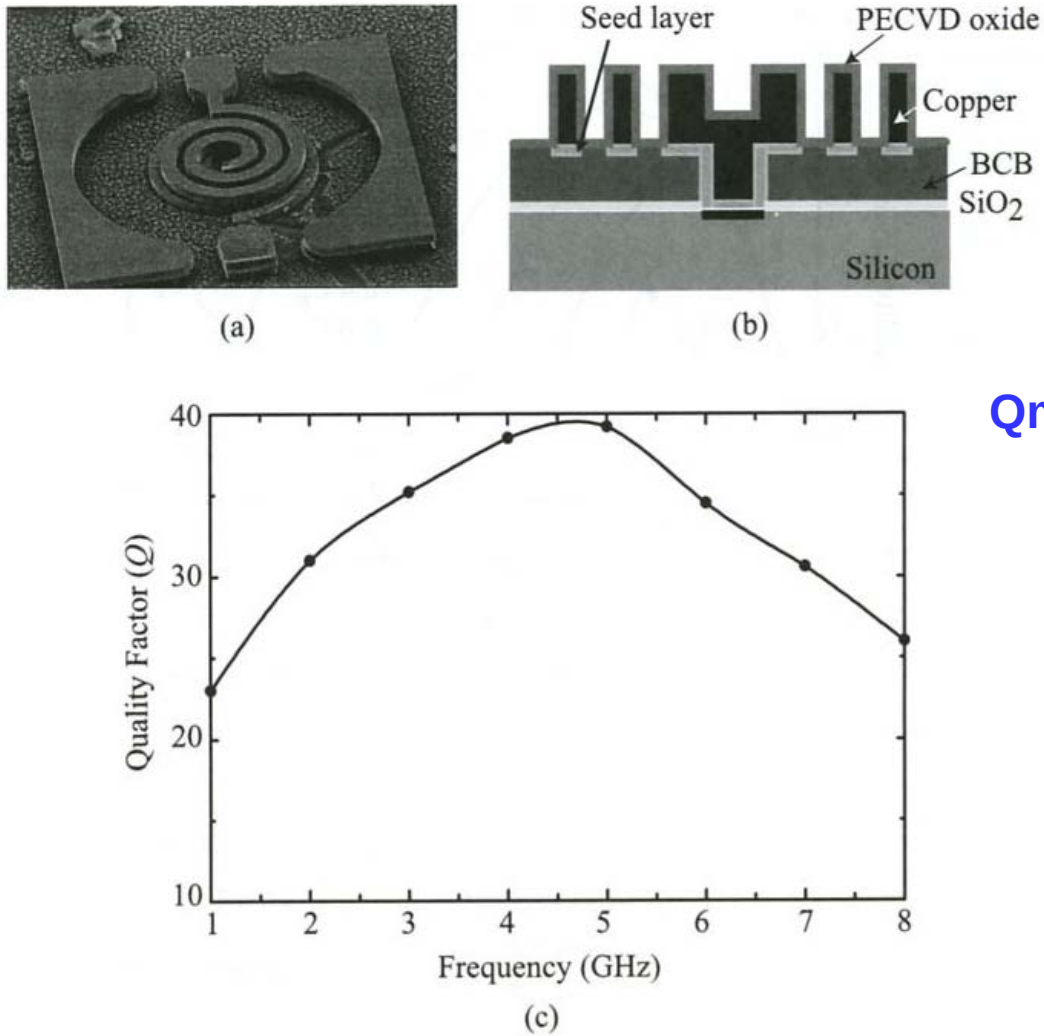


Figure 12.7. The electroplated copper MEMSCAP inductor (a), cross-sectional view (b), and the measured Q of a 1.5-nH inductor [12] (Copyright IEEE).

Qmax = 40!

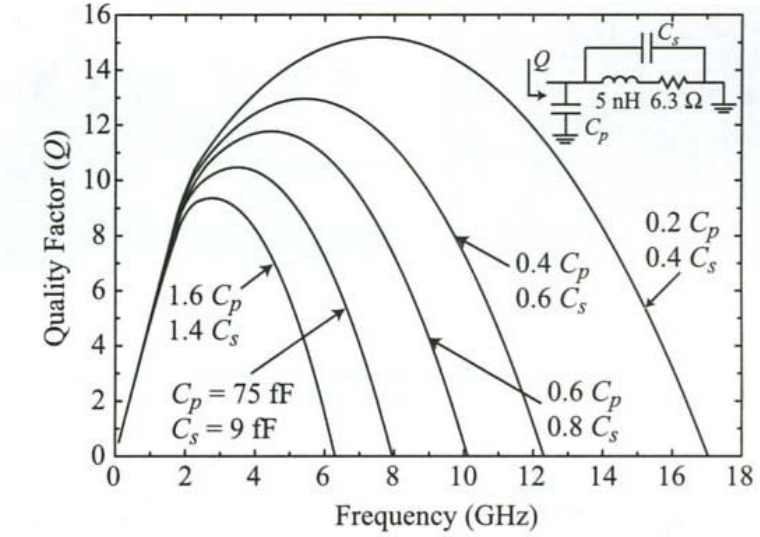
Substrate etching

- Parasitic capacitance between inductor and ground plane is a problem
  - Depends on type and thickness of dielectric
  - Depends on type and thickness of substrate
- Solution: **etching of the underlying substrate**
  - Reduction of parasitic capacitance
  - Q increases
  - Resonance frequency is shifted to higher frequency
    - Increases the useful bandwidth of the inductor
  - High L can be implemented at the same time as avoiding a too low f_max
- Alternative: elevation/suspension

Substrate capacitance effect on Q and reactance X

At 1 – 4 GHz series resitance limits

Figure shows that higher Q also gives a higher self resonance frequency



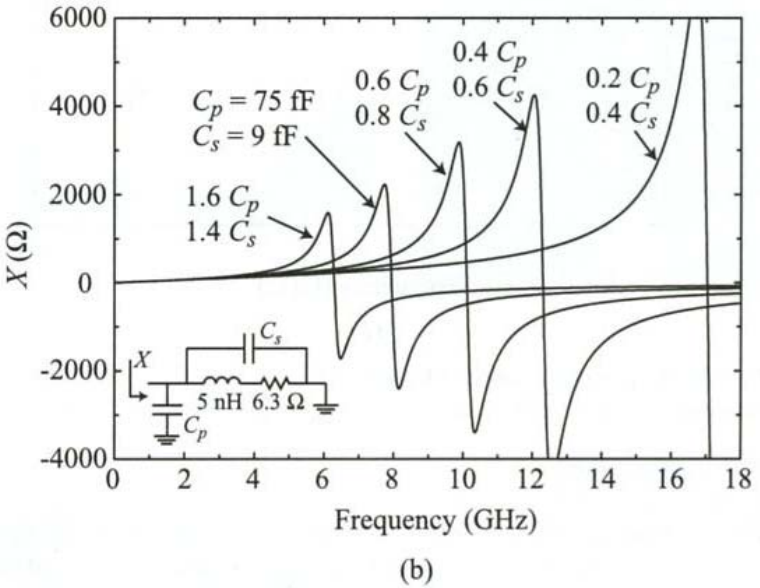
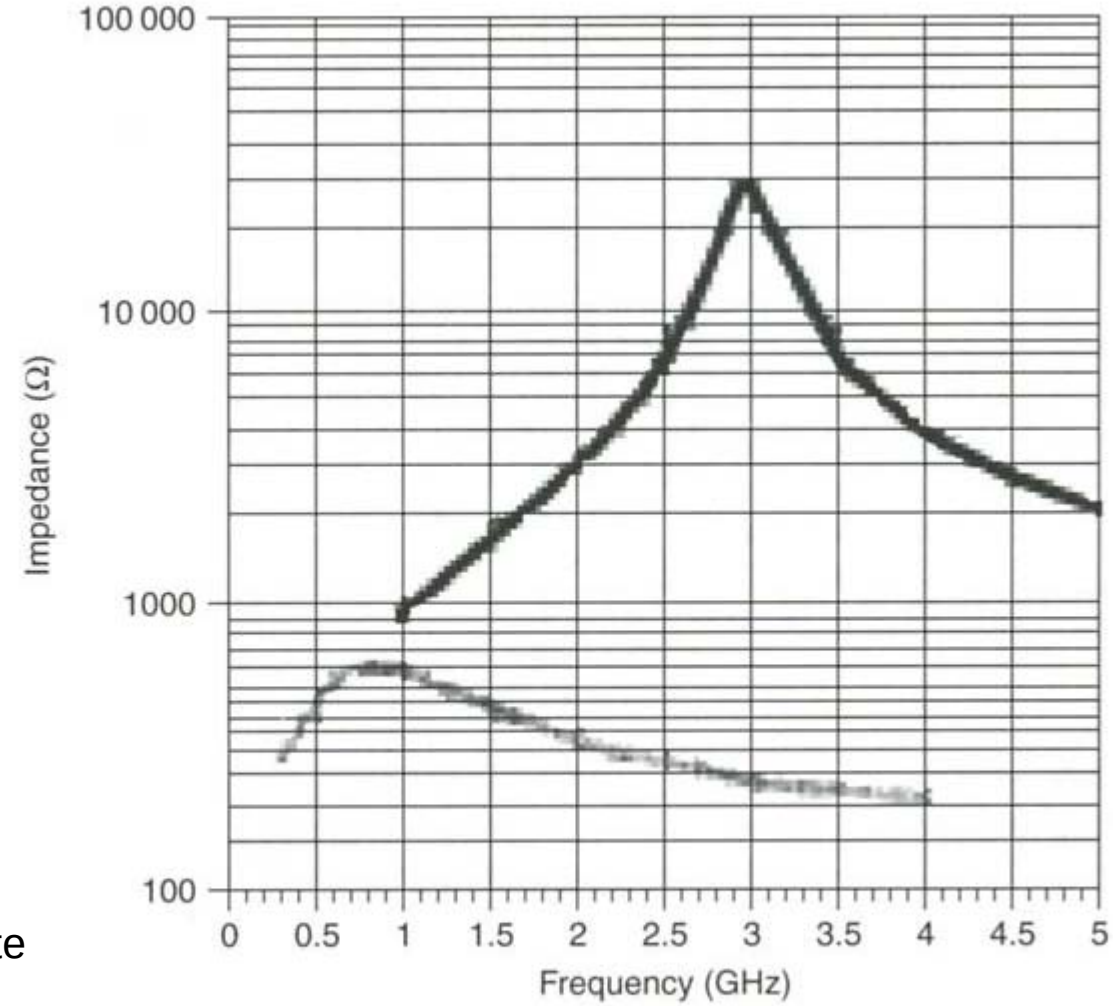


Figure 12.6. The effect of the substrate capacitance on the Q (a) and X (b) of a 5-nH inductor. The resistance is assumed constant up to 2 GHz and then increases as $\sqrt{f}$.

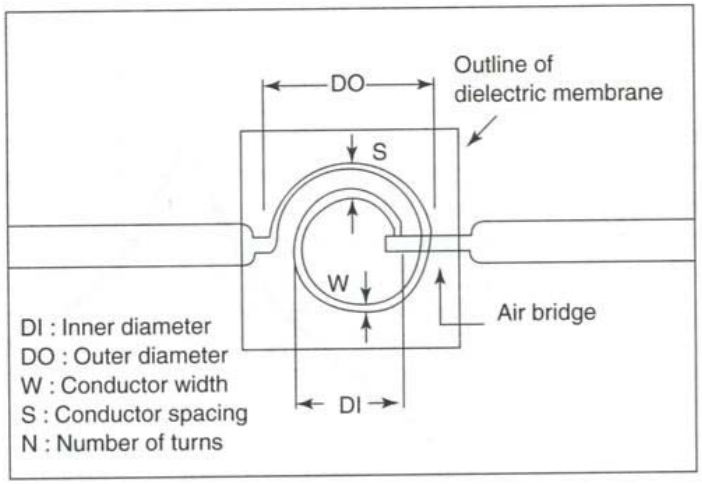


With and **without** underlying substrate

Figure 4.13 Simulated change in resonant frequency of 100 nH inductor with (gray) and without (black) underlying substrate. Reproduced from J.Y.-C. Chang, A.A. Abidi and M. Gaitan, 1993, 'Large suspended inductors on silicon and their use in a 2 mm CMOS RF amplifier', *IEEE Electron Device Letters* **14**(5): 246–248, by permission of IEEE, © 1993 IEEE

Test system

- Example system for testing the effect of having a solenoid on a **membrane** or directly on **Si**



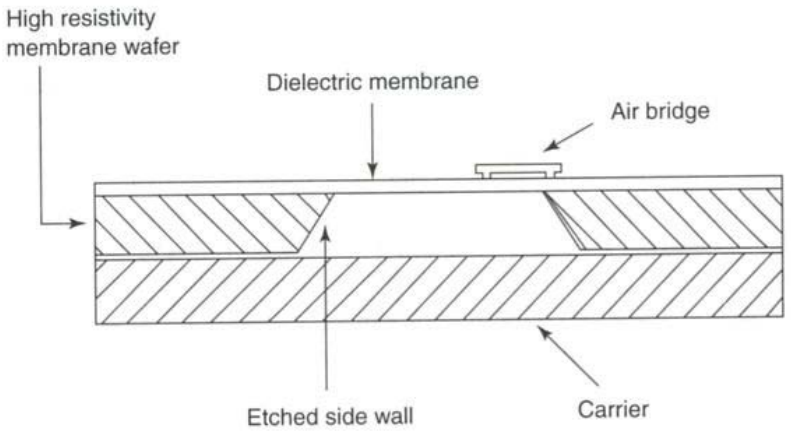


Figure 4.14 Schematic diagrams of the planar inductor and the membrane outline. Reproduced from C.-Y. Chi and G.M. Rebeiz, 1995, 'Planar microwave and millimeter wave lumped elements and coupled line filters using micromachining technique', *IEEE Transactions on Microwave Theory and Techniques* **43**(4): 730–738, by permission of IEEE, © 1995 IEEE

Achieved L on Si and membrane

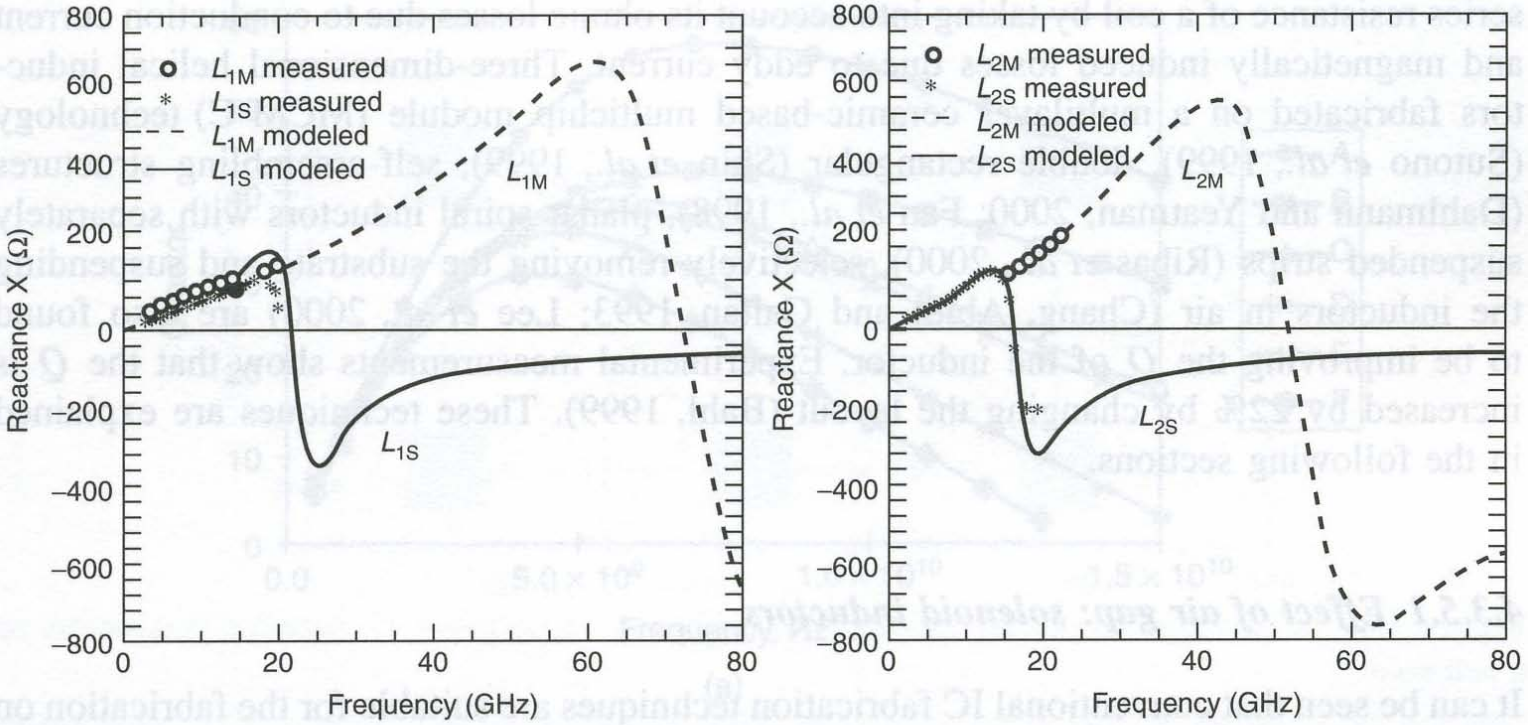


Figure 4.15 Measured and modeled reactance for inductors on silicon (L_{1S}, L_{2S}) and on membrane (L_{1M}, L_{2M}). Reproduced from R. Rodrigues, J.M. Dishman, F.D. Dickens and E.W. Whelan, 1980, 'Modeling of two-dimensional spiral inductors', *IEEE Transactions Components, Hybrids, Manufacturing Technology* **5**: 535–541, by permission of IEEE, © 1980 IEEE

M = membrane, S = Si

Ex.: Q for different etch depths

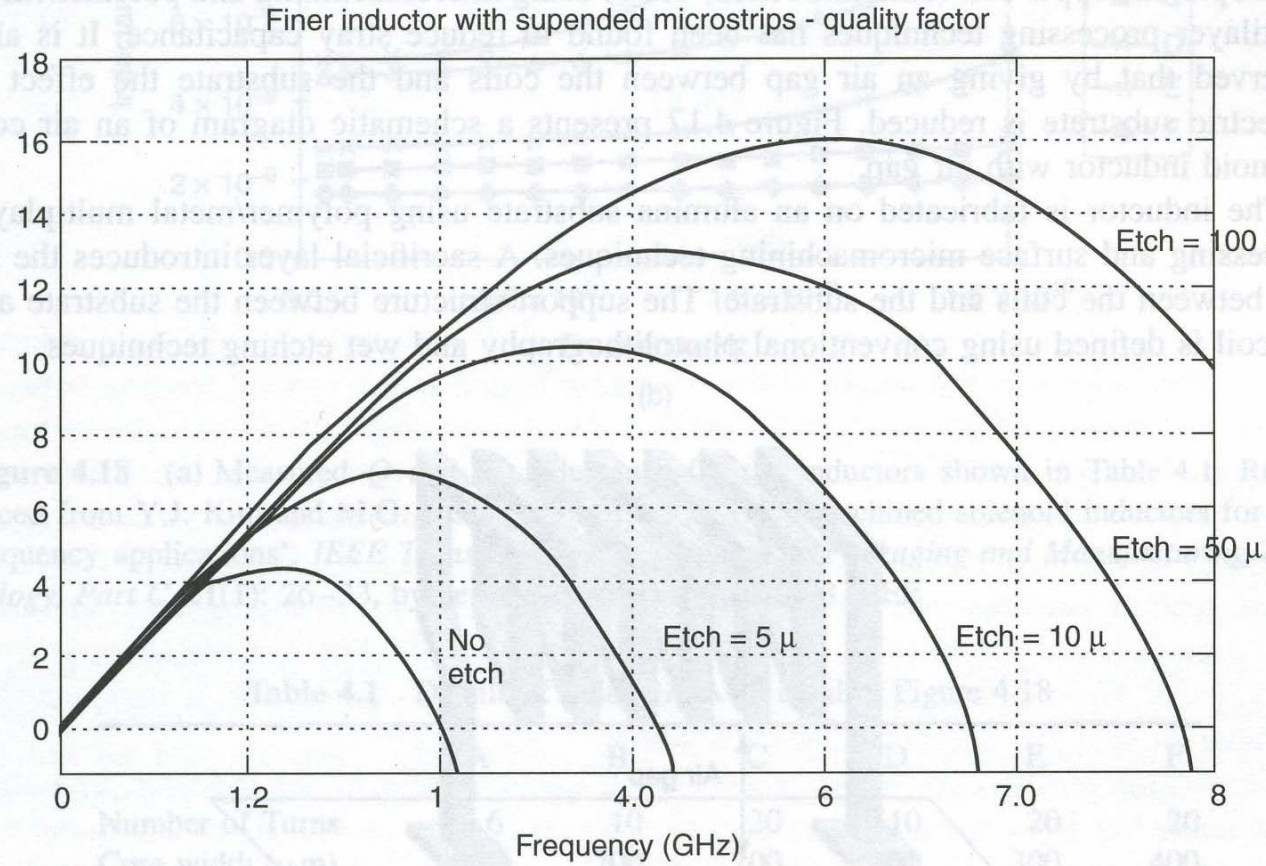


Figure 4.16 The change in Q for a suspended planar inductor for different etch depth. Reproduced from R.P. Ribas, N. Bennouri, J.M. Karam and B. Courtois, 1997, 'GaAs MEMS design using 0.2 μm HEMT MMIC technology', in *Proceedings of the 19th Annual IEEE Gallium Arsenide Integrated Circuit Symposium*, IEEE, Piscataway, NJ, USA: 127–130, by permission of IEEE, © 1997 IEEE

Different substrate materials

- Substrate etching has no effect on Q for low frequencies
  - Rs is the limitation
  - Rs is prop with sqrt(f)

- Look at the effect of different substrate materials →
  - Different resistivity

Q-factor for substrates with different resistivities

”Eddy current”-effects are present at high frequency

High resistivity substrate increases performance

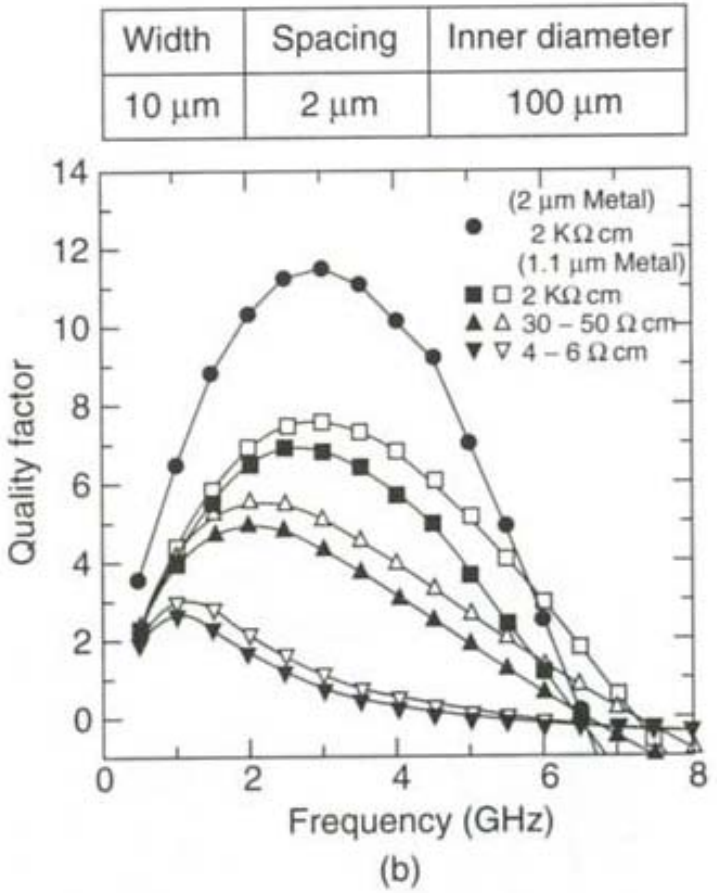
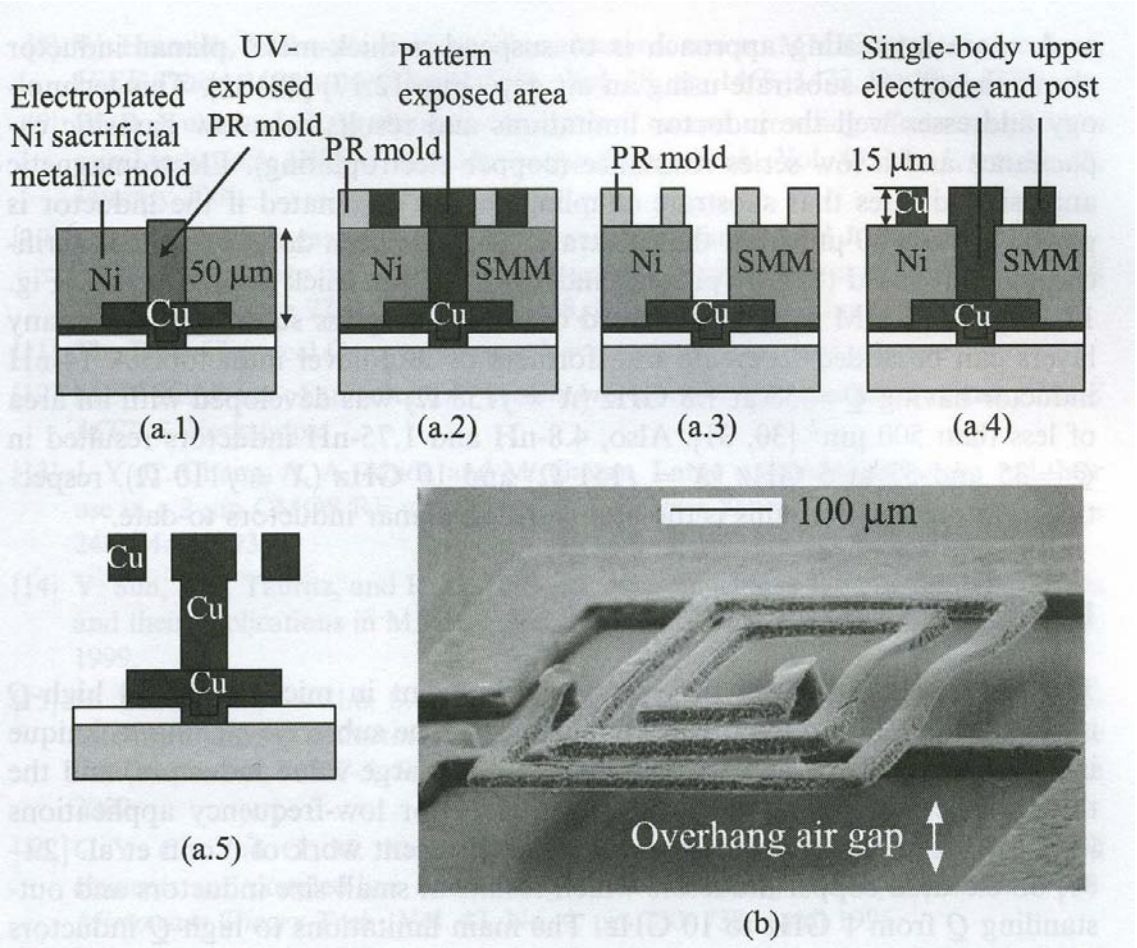


Figure 4.29 Change in Q of an inductor for (a) different metal thickness; (b) for substrates with different resistivity. Reproduced from M. Park, C.S. Kin, J.M. Park, H.K. Yu and K.S. Nam, 1997b, ‘High Q microwave inductors in CMOS double metal technology and its substrate bias effects for 2 GHz RF IC application’, in *Proceedings of IEDM 97*, IEEE, Washington, DC: 59–62, by permission of IEEE, © 1997 IEEE

Both rectangular and spiral inductors are shown

”Air gap” - inductor

- Thick metal planar inductor over substrate with an air gap in-between
  - Elimination of substrate coupling: 30 μm elevation
  - ”Sacrificial metallic mold” (SMM) process used + 10-15 μm copper layer



Performance to inductor above air gap

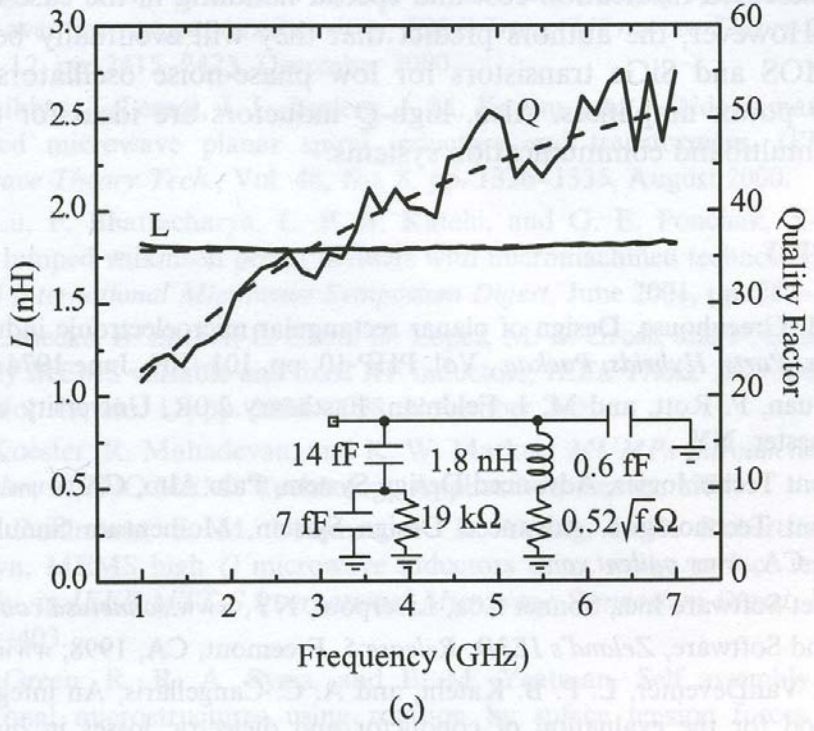


Figure 12.17. Fabrication process (a), picture (b), and measured performance (c) of an overhang inductor using 15-μm-thick copper layers [29, 30] (Copyright IEEE).

- Ex. from the first known work, fig 12.8 a: anisotropic etching
- Fig 12.8 b: suspended inductor
  - One anchor: sensitive to mechanical vibrations
  - Q = 17 at 8.6 GHz

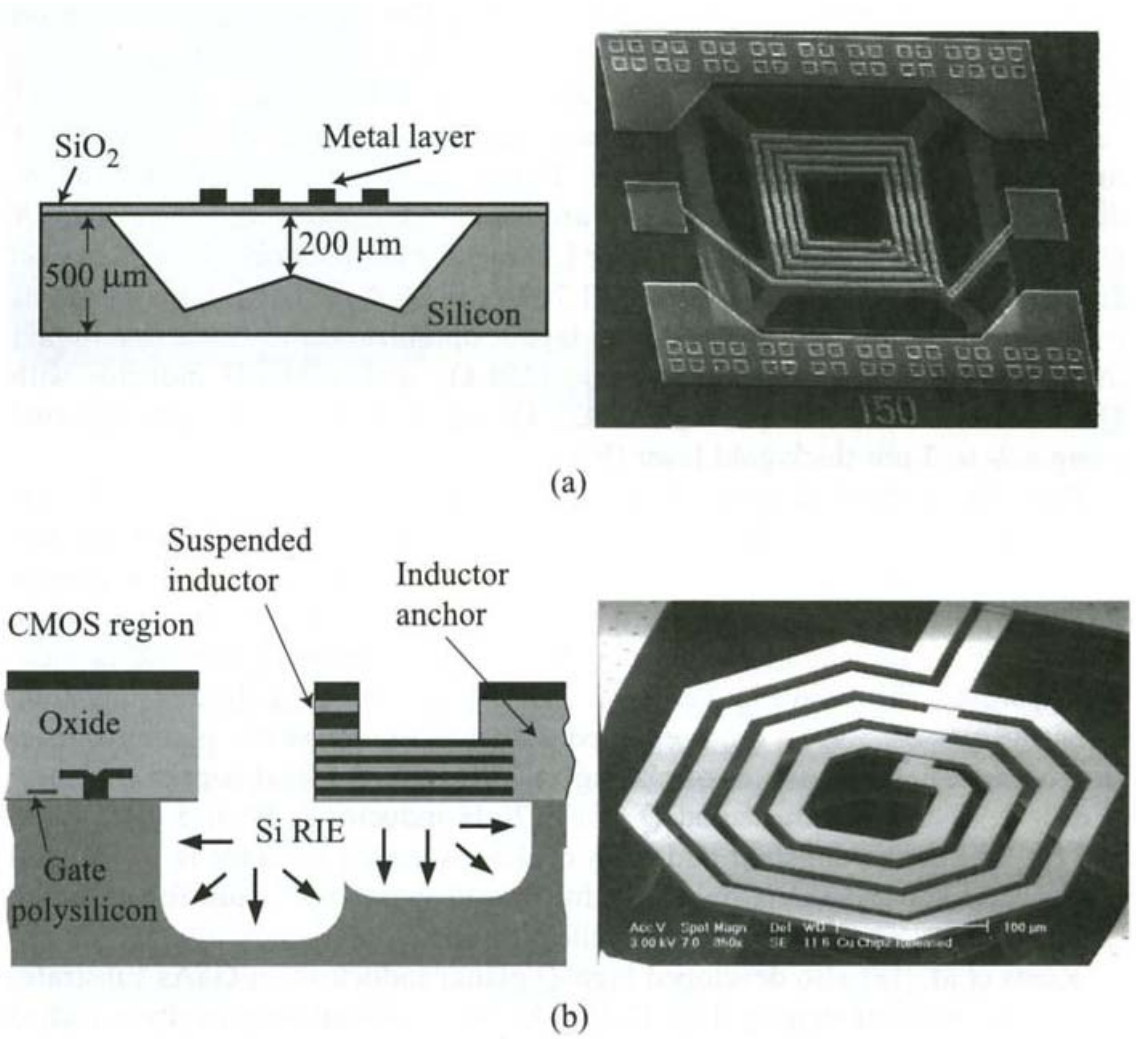
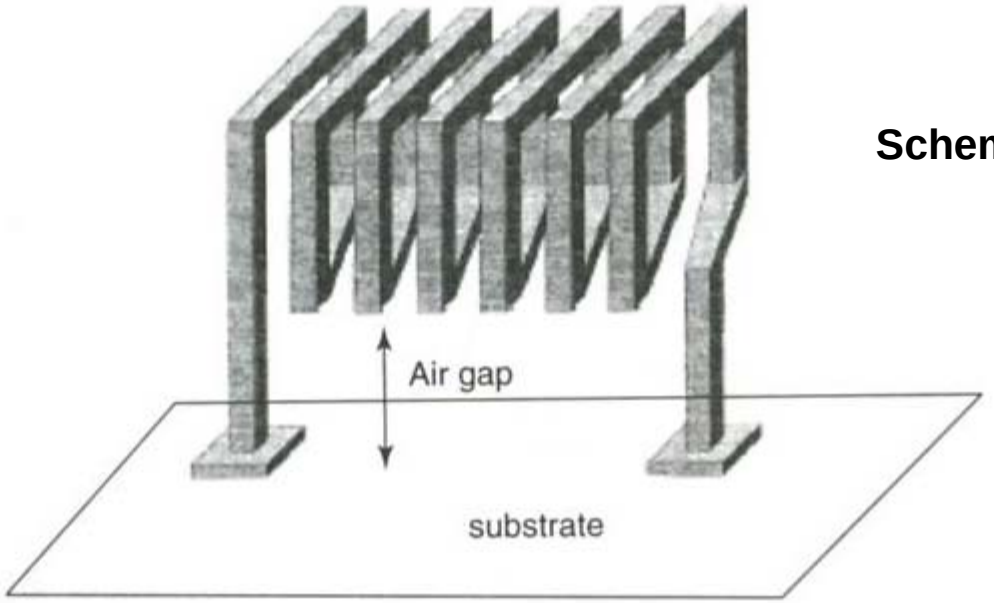


Figure 12.8. Suspended inductors using front-etching techniques and compatible with CMOS processing: UCLA and Delft [13, 14] (a), Carnegie Mellon (b), effort [15] (Copyright IEEE).

Air-gap for solenoids



Schematic figure!

Figure 4.17 Schematic diagram of a solenoid inductor with an air gap. Reproduced from Y.J. Kim and M.G. Allen, 1998, 'Surface micromachined solenoid inductors for high frequency applications', *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part C* **21**(1): 26–33, by permission of IEEE, © 1998 IEEE

Effect of air-gap for spiral inductors

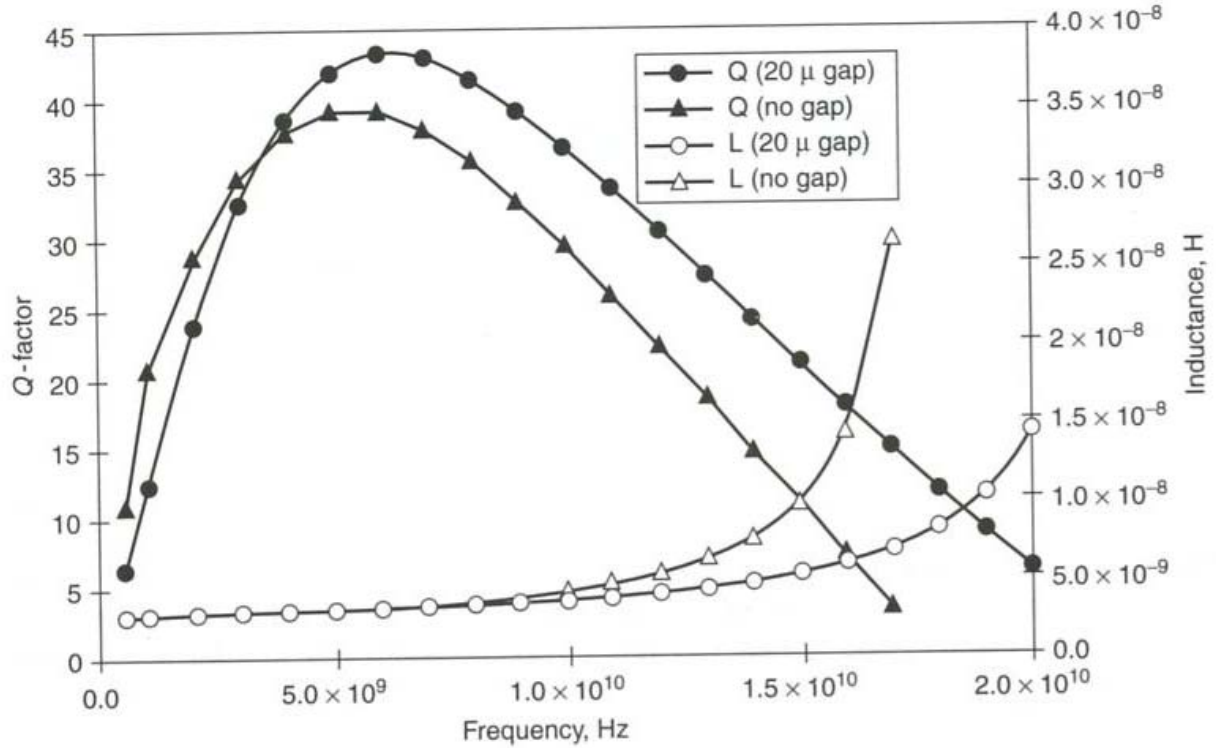


Figure 4.22 Effect of air gap on *Q* factor. Reproduced from Y.J. Kim and M.G. Allen, 1998, 'Surface micromachined solenoid inductors for high frequency applications', *IEEE Transactions on Components, Packaging and Manufacturing Technology, Part C* **21**(1): 26–33, by permission of IEEE, © 1998 IEEE

L benefits from ”no-gap” (between inductor and substrate), Q benefits from air-gap

Summary: How to increase performance?

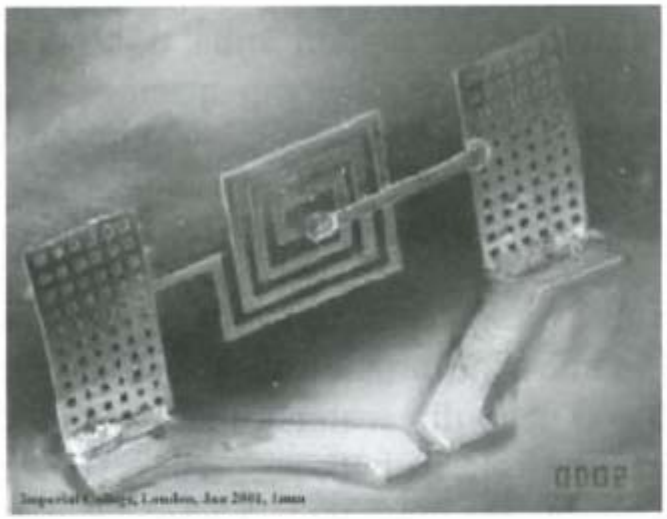
- Have **thick metal layer** with good conductivity
  - To reduce series resistance
- Use **substrate etching**
  - Reduce substrate parasitic capacitance
- Use **3-D** structures
  - For “vertical plane” solenoids the L-value may increase
- Use of **core material**

Basic implementation technologies

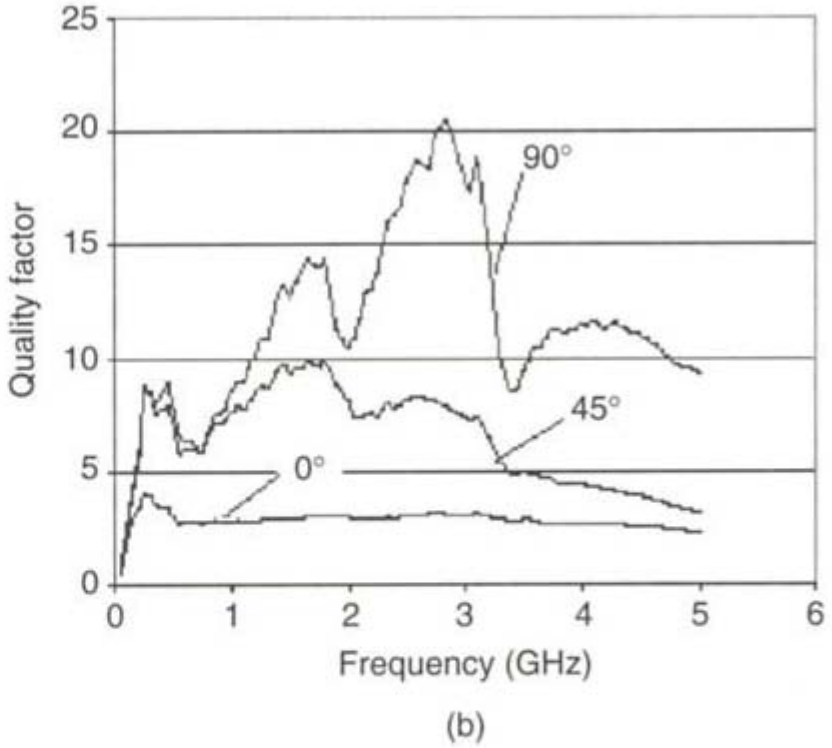
- Thick metal electroplating
  - 0.2 – 6 GHz
- Substrate etching
  - 1 – 100 GHz
- Three-dimensional solenoid type inductors
  - 0.2 – 6 GHz

- ”Self-assembly” (elevation) of inductor →
  - Elevate inductor **above substrate** to reduce parasitic capacitance to substrate, 1 – 100 GHz

Folded and elevated inductors



(a)



(b)

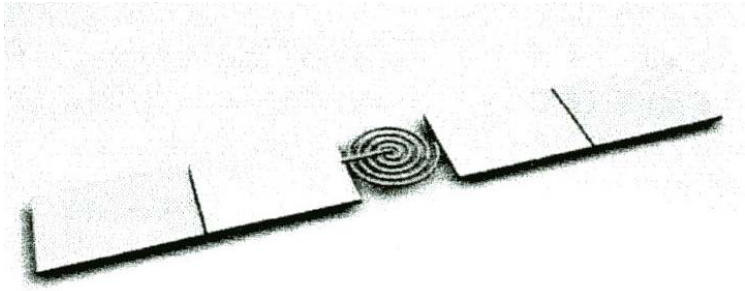
Solder surface tension

Figure 4.30 (a) Three-turn spiral folded inductor after self-assembly; and (b) change in Q against frequency for different angles between coil and substrate. All devices are $4\frac{1}{2}$-turn meander inductors ($L = 2$ nH). Reproduced from G.W. Dahlmann and E.M. Yeatman, 2000, 'High Q microwave inductors on silicon by surface tension self-assembly', *Electronics Letters* **36**(20): 1707–1708, by permission of IEEE, © IEEE 2000

Eric. Yeatman, Imperial College, London

Out of plane inductors

- Inductor can be **elevated** by ”scratch actuators”
  - L. Fan et al, MEMS 1998
  - Elevated 250 μm over Si substrate
  - Resonance at 1.8 – 6.6 GHz after elevation of solenoid



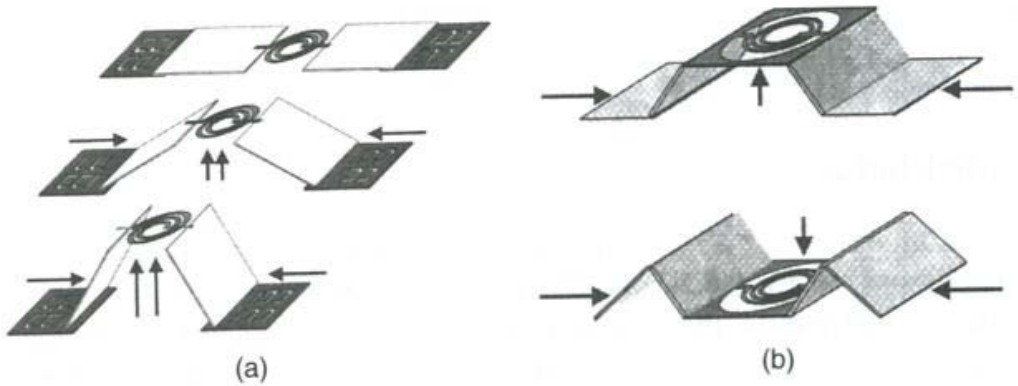


Figure 4.31 (a) Schematic diagram of the MESA micro-elevator by self-assembly structure; (b) the center platform can move upward or downward. Reproduced from L. Fan, R.T. Chen, A. Nepolsa and M.C. Wu, 1998, ‘Universal MEMS platforms for passive RF components: suspended inductors and variable capacitors’, in *Proceedings of 11th Annual International Workshop on MEMS ’98*, IEEE, Washington, DC: 29–33, by permission of IEEE, © 1998 IEEE

Micromachining using self-assembly

Elevate inductor above substrate to reduce parasitic capacitance

Cr-Au layer over poly-layer

Different residual **stress** in materials make the inductor **"curl"** above substrate

Anchor causes a significant parasitic capacitance

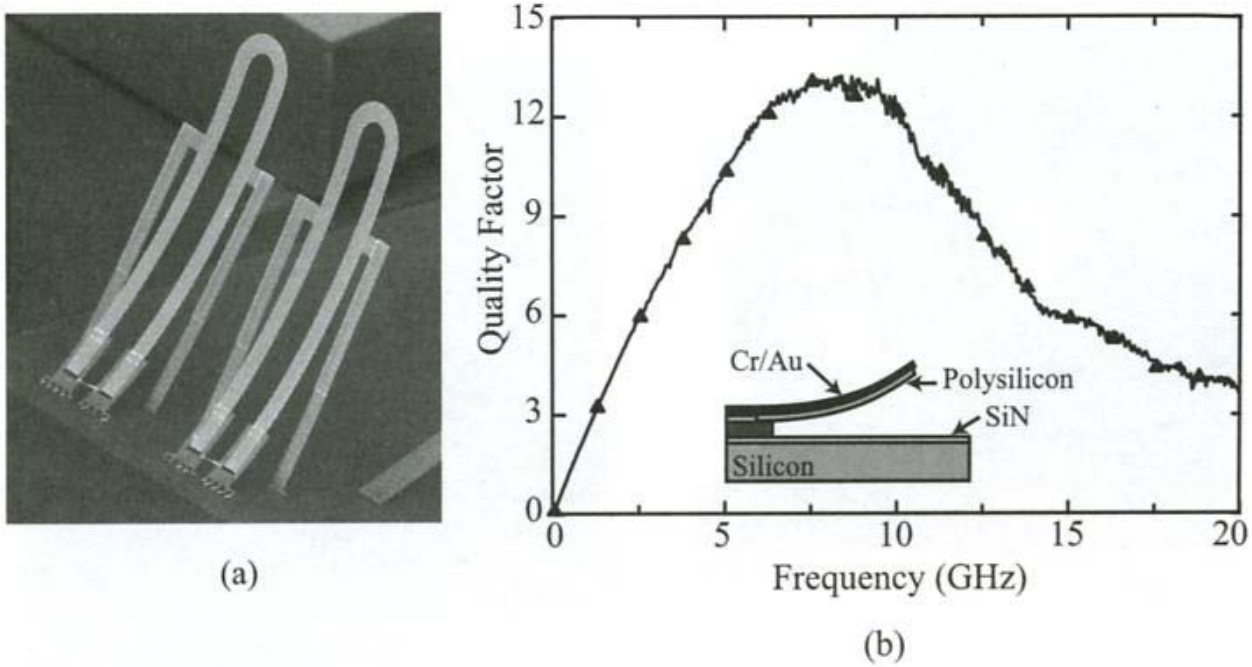


Figure 12.12. Picture (a) and measured Q (b) of a self-assembled 1.2-nH inductor [20] (Copyright IEEE).

Solder surface tension used

Photo resist as sacrificial layer

Copper structure with **solder pads** between anchor and a free movable structure

Heating to 185 ° C → solder pads melt and pull, due to surface tension force, the structure to a vertical position

Cooling → solder hardens

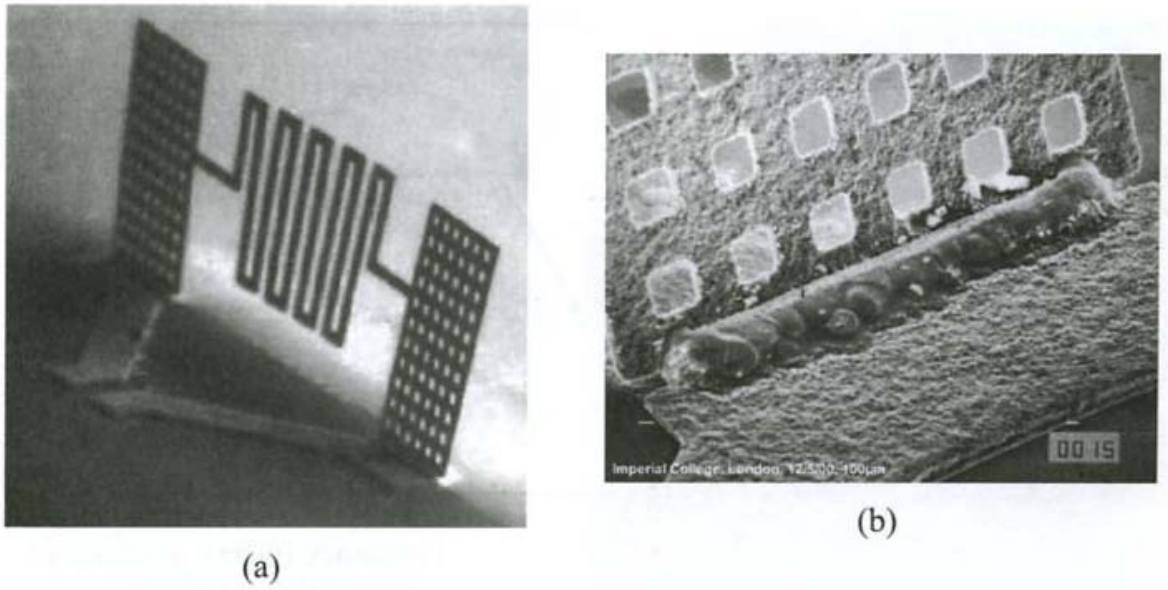
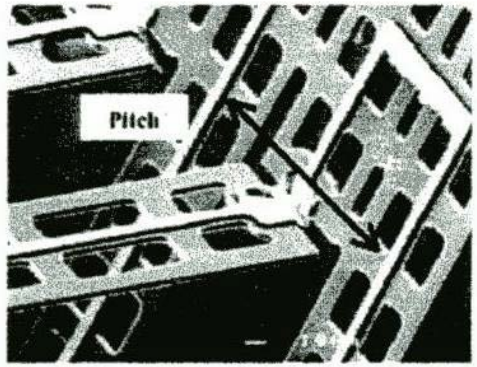
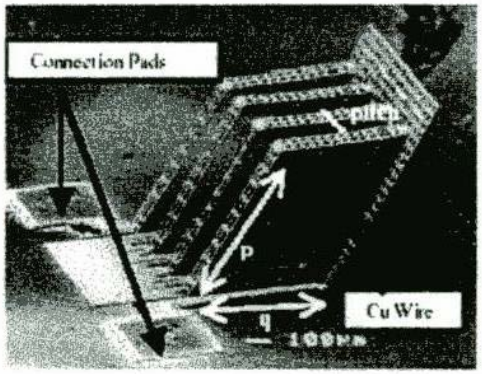


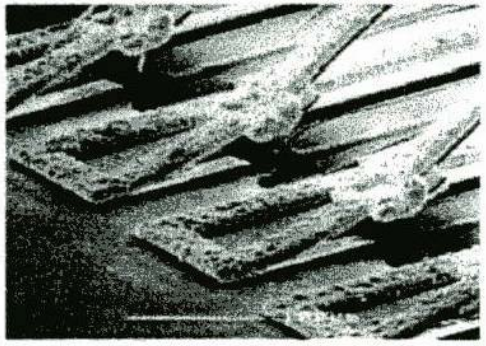
Figure 12.13. (a) Out-of-plane meander-type inductors after self-assembly, and (b) a blow-up of the solder hinges after heating [22, 23] (Copyright IEEE).

Structure with suspension hinges

- Copper structure can **manually** be folded and glued
- Typical ”turns” with large dimensions ~100 µm
- M. Gel et al, Transducers 2001







Today's lecture

- What is an inductor?
- MEMS -implemented inductors
- Modeling
- Different types of RF MEMS inductors
  - **Horizontal plane** inductors
  - Real **solenoids**
- How to increase performance
  - Q-value, Inductance (L), Self resonance frequency (f_max)
- Elevated inductors
- Inductor banks

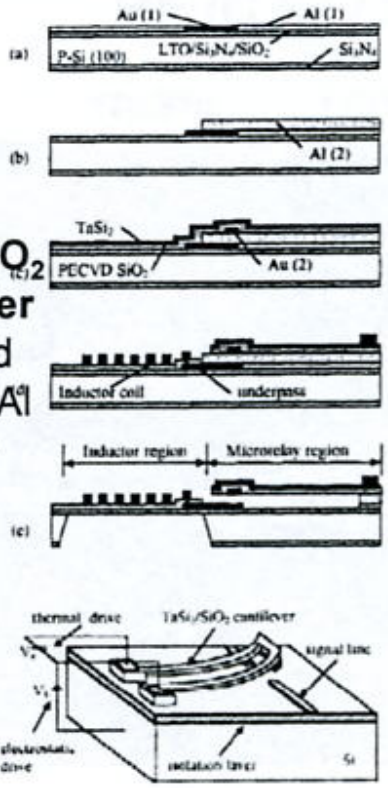
Programmable inductor banks

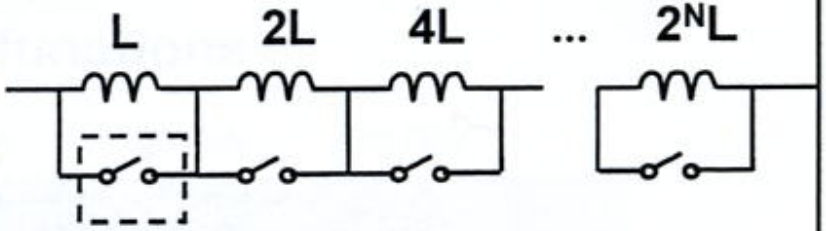
FSRM

Micromachined digitized high-Q inductor banks

Design and process (New jersey Institute of Technology)

- **micro-relays made on $TaSi_2/SiO_2$ bimorph cantilever beam**, gold-to-gold electrical contact, Al as sacrificial layer and thermal actuation
- **gold inductors and pads**





Contact switch (micro-relay)

Thermal actuation!

Performance:

- **L = 2.5 up to 162.4 nH**
- **Q=3.3 @ 1.6GHz**
- electro-thermal relays with **R_{on}=0.6-0.8Ω**
  thermal power=8mW, V=20V
- contacts fails after 10^6 cycles (!!)

$D_3D_2D_1D_0$	L (nH)	$D_3D_2D_1D_0$	L (nH)
0000	324.8	1000	162.4
0001	277.9	1001	105.7
0010	223.2	1010	67.4
0011	185.0	1011	45.9
0100	166.9	1100	60.5
0101	127.3	1101	31.5
0110	103.8	1110	16.2
0111	83.1	1111	2.5

S. Zhou, X.-Q. Sun, W.N. Carr, TRANSDUCERS '97, Vol. 2, June 1997, pp. 1137 –1140.

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[Ionescu]

How different design parameters influence performance

- Q_max and f_rez decrease when area and number of turns increase

Integrated inductor performance versus design space

After Varadan et al. [3]

		Q_{max}	L	f_{rez}
Conductor thickness	↗	↗	-	-
Sheet resistance	↗	↘	-	-
Insulator thickness	↗	↗	-	↗
Substrate resistivity	↗	↘ ↗	-	↗
Area	↗	↘	↗	↘
Number of turns	↗	↘	↗	↘
Track width	↗	↗	↘	↘
Multilayer inductor (extra layer)	↗	↘	↗	↘

(Double arrow: less influence)