INF5490 RF MEMS

LN02: MEMS – Fabrication

Spring 2011, Oddvar Søråsen
Department of Informatics, UoO

Today’s lecture

- Micromachining

- Important process steps
  - General
  - Summary: MEMS-specific steps

- Examples of processes
  - MultiMEMS
  - polyMUMPs

References

- In addition to the course book (Varadan et al):

- Overview articles:
  - "Bulk micromachining of silicon," Kovacs, G.T.A. Maluf, N.I., Petersen, K.E., Proceedings of the IEEE, Aug 1998, Volume: 86, Issue: 8, page(s): 1536-1551
  - "Polysilicon: a versatile material for microsystems," P. J. French, *Sensors and Actuators A: Physical*, *Volume 99, Issues 1-2*, *30 April 2002*, *Pages 3-12*
  - **"**Silicon as a mechanical material**,"** Petersen, K.E. , Proceedings of the IEEE, May 1982, Volume: 70, Issue: 5, Page(s): 420- 457
  - Proceedings of IEEE , Vol 86 No 8, **1998 Special Issue on MEMS**

- Books:
  - Kovacs, Micromachined Transducers Sourcebook, McGraw-Hill 1998
  - Maluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2004
  - Senturia, Microsystem Design, Kluwer, 2001

MEMS for RF?

- MEMS technology is **attractive for RF** due to
  - Miniaturization: small dimensions (~µm)
  - Batch processing
    - Many units at low cost
  - Good quality components
    - High Q, low loss, reduced parasitics
    - Low power consumption
  - Integrated systems possible

- Essential: → **MICROMACHINING!**

Micromachining

- Micromachining, definition:
  - *Accurately, to **define** and **implement** any microscopic mechanical structure **“out of”** or **“on”** a material*

- **Silicon micromachining is mature**
  - Si processes also used by IC industry
    - MEMS-processing ”grown out of” IC-processing
  - New *specific* MEMS processes are also developed
    - A lot of variants, - **few standards!**

What is needed?

- A proper **substrate**
  - Si, SOI, glass (PSG), quarts
- Basic methods
  - Define geometries (pattern)
  - Modify material properties
  - Remove material
  - Add new material
  - Bonding wafers together

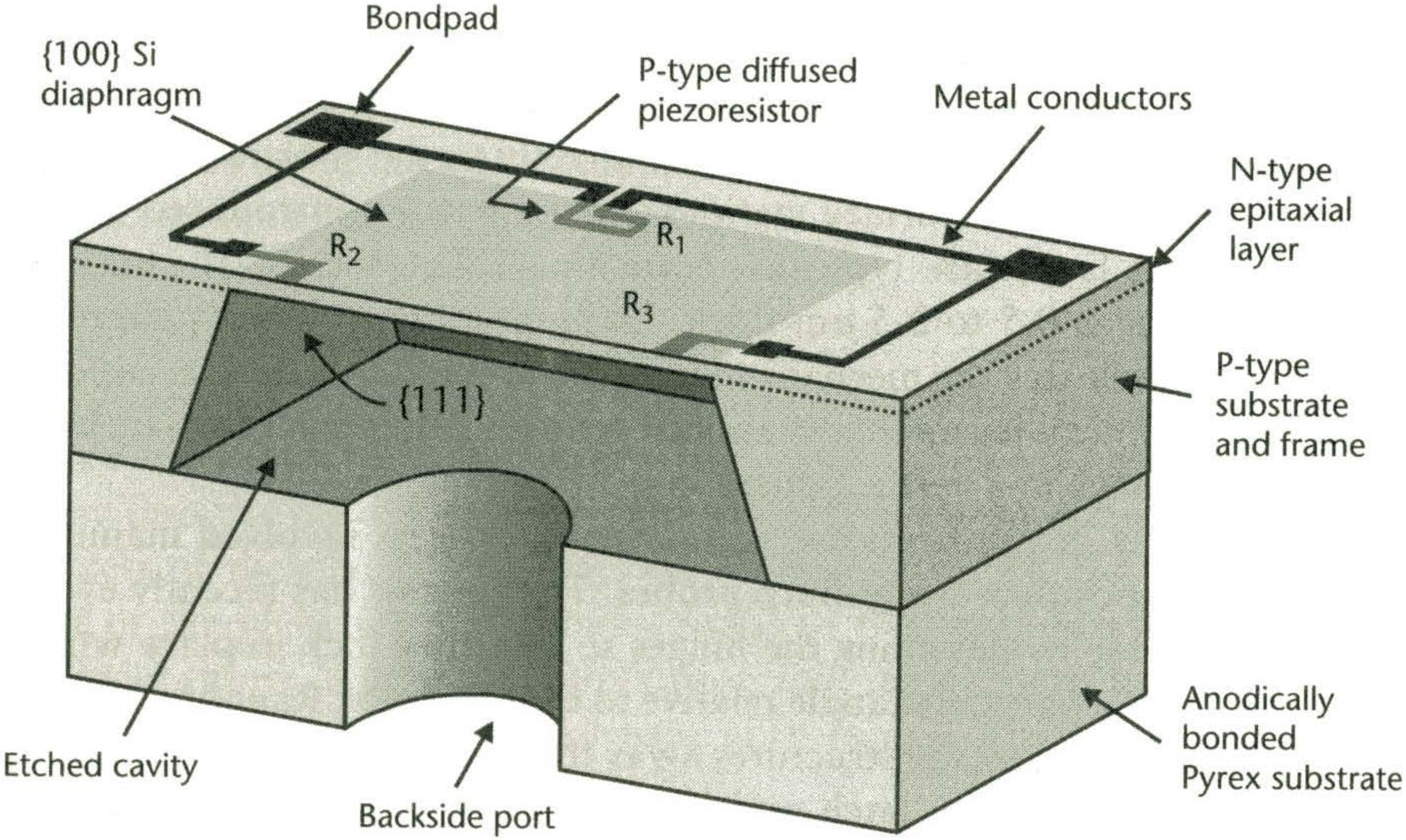
2 main procedures

- **”Bulk”** micromachining
- **”Surface”** micromachining
- An overview is given in the following
  - Details can be found in literature

Bulk micromachining

- Selective **etching** of and **diffusion** into well defined areas **of a substrate**
  - Ex.: Etching of substrate from back side
    - Wet etching: liquid is used
  - Possibly combined with dry etching from front side
- Typical examples
  - Membrane: pressure sensor
  - Suspended mass: accelerometer (“inertial sensor”)
- \+ More mature than surface micromachining
- +/- Coarse-grained structures
- ”Wafer-bonding” typically used
  - Attach/combine whole wafers

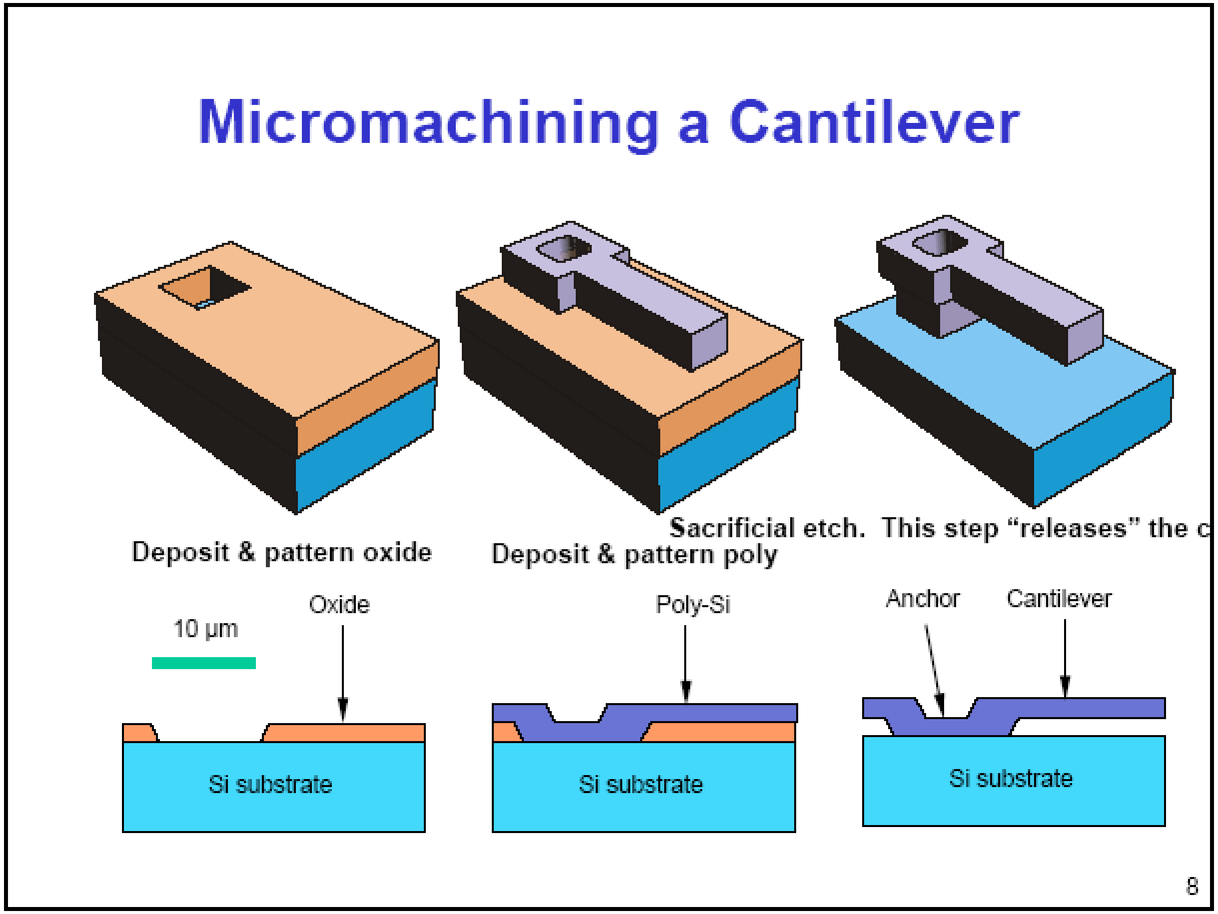
Pressure sensor



Surface micromachining

- **”Surface”** micromachining
  - **Deposit** layers
    - **Structural layer**
    - **Sacrificial layer** = ”distance-keeping” layer

  - Selective **etching** of structural layers
  - **Remove** sacrificial layers
    - → Release structures for movement

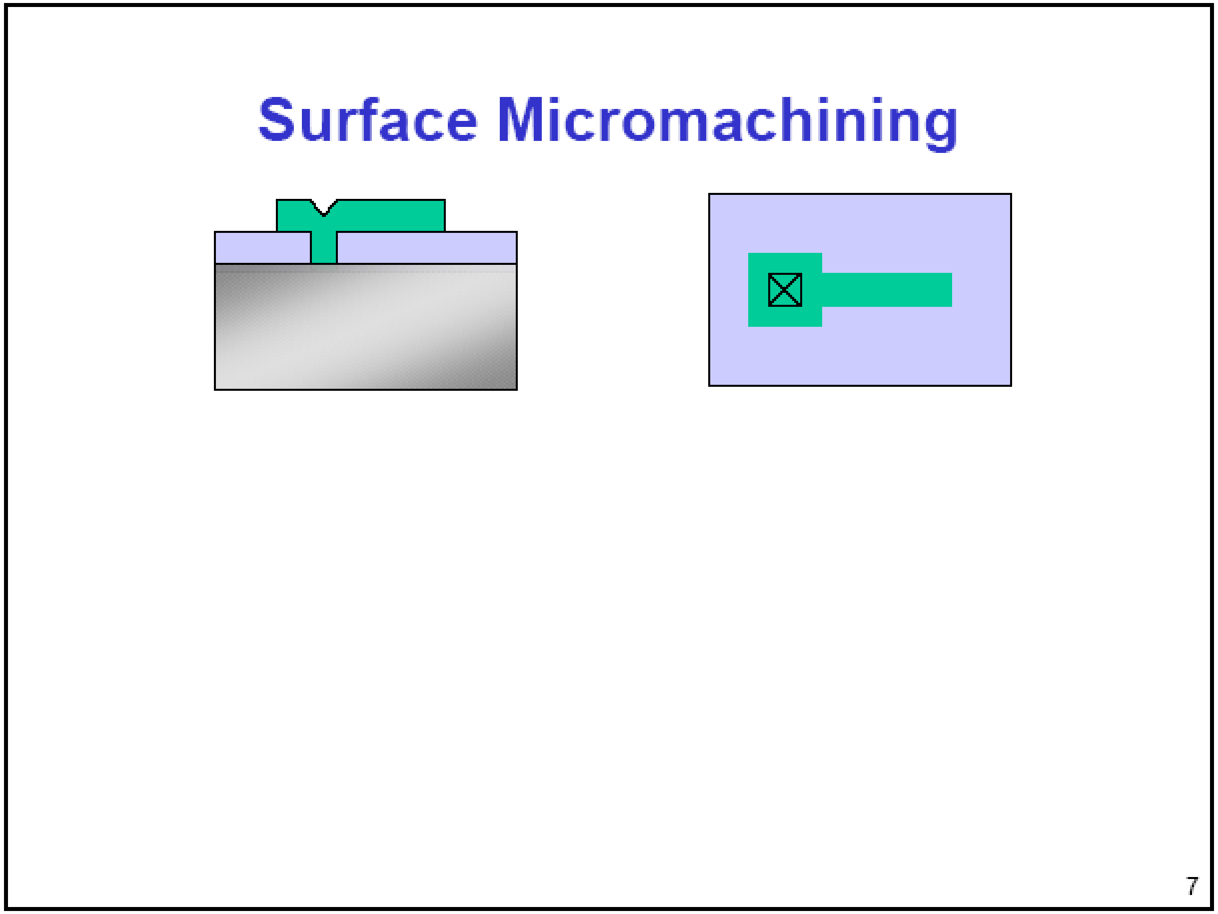


Micromachining a Cantilever

Deposit & pattern oxide

Deposit & pattern poly

Sacrificial etch. This step “releases” the c



Surface Micromachining

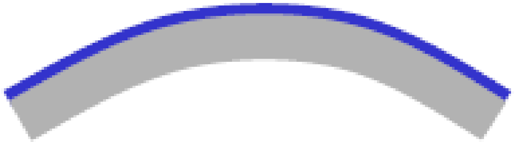
Surface micromachining

- + Can make structures with smaller dimensions
- ÷ Structures have smaller ”mass”
  - Unsufficient for some applications
    - Inertial components (accelerometer)
- + Possible to integrate IC-components
- **Structural layers** must have
  - Desired **electrical** properties
  - Proper **mechanical** properties
    - Elasticity, density, reliability
    - **Stress:** different stress in neighbouring films may be a problem
- **Sacrificial layers**
  - Must be removed effectively by etching
    - Avoid **stiction**
    - **Perforating** large surfaces may be needed

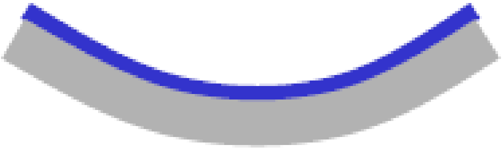
Residual Stress in Thin Films

- Residual film stress
  - Microstructure
  - Thermal mismatch

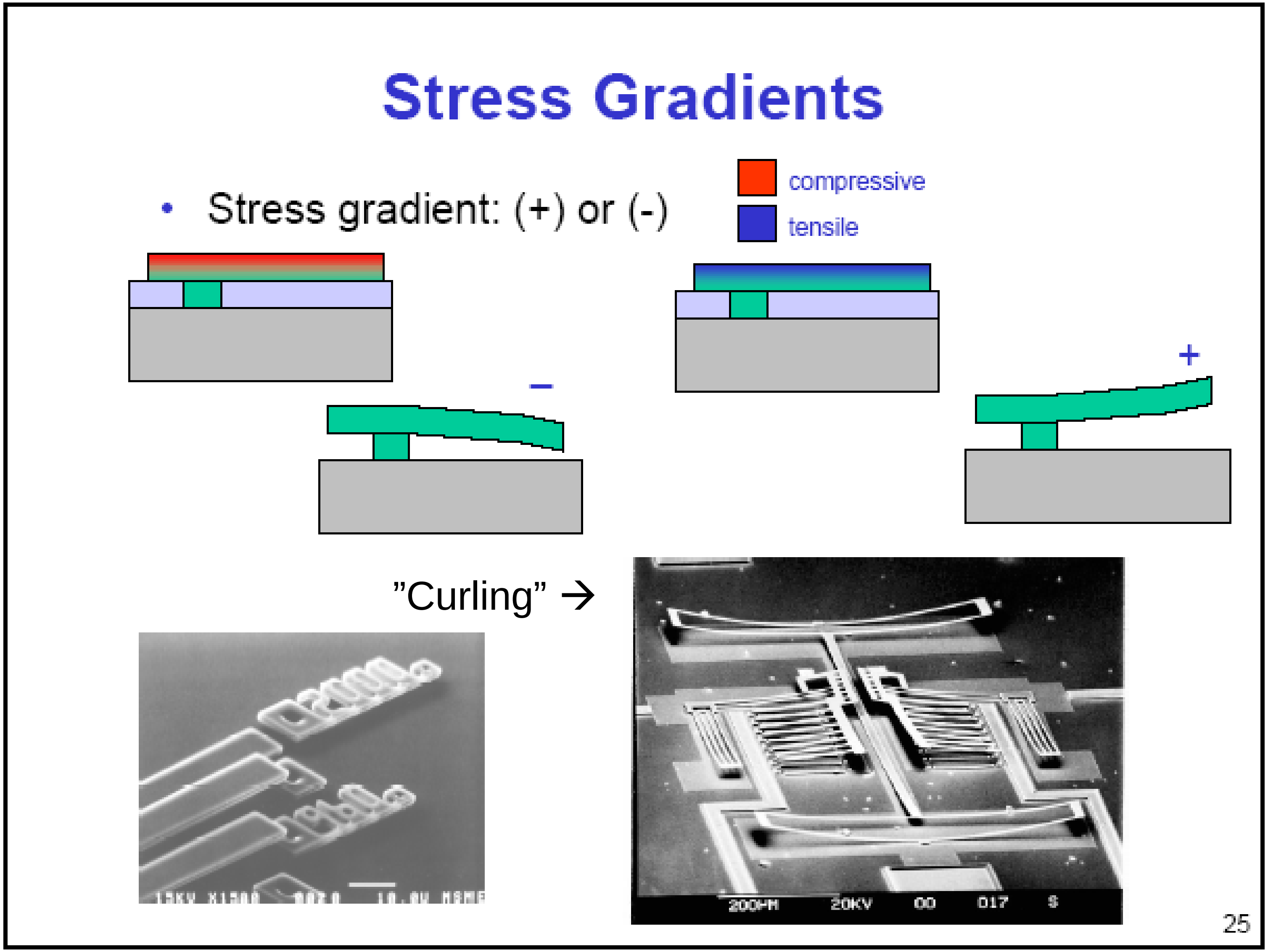
- Compressive vs. tensile stress



Under compressive stress, film wants to expand. Constrained to substrate, bends it in convex way.



Under tensile stress, film wants to shrink Constrained to substrate, bends it in concave way.



Stress Gradients

- Stress gradient: (+) or (-)

🟥 compressive

🟦 tensile

”Curling” →

Important process steps

- Define patterns
  - ***Photolithography***
- Modify semiconductor material properties
  - ***Diffusion***
- Remove material
  - ***Ething***
- Adding material – build structures
  - ***Deposition***

Photolithography

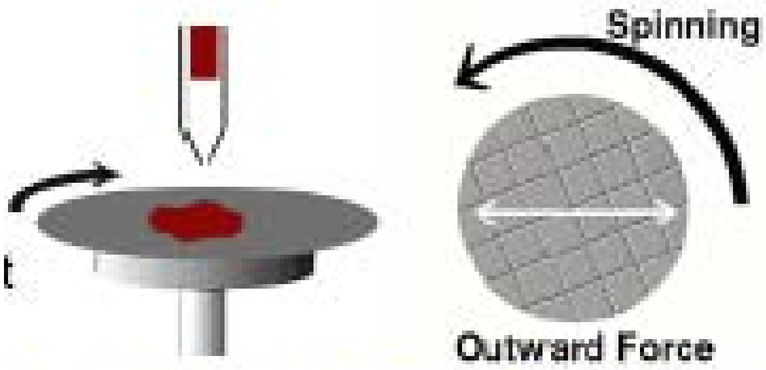
- Transfer design pattern → pattern in material
  - Using **photoresist** (organic) – ”spin-on”
  - Exposure using **photo mask** → developing of photoresist→ ”post bake” → ”treatment” of material (etching/diffusion)

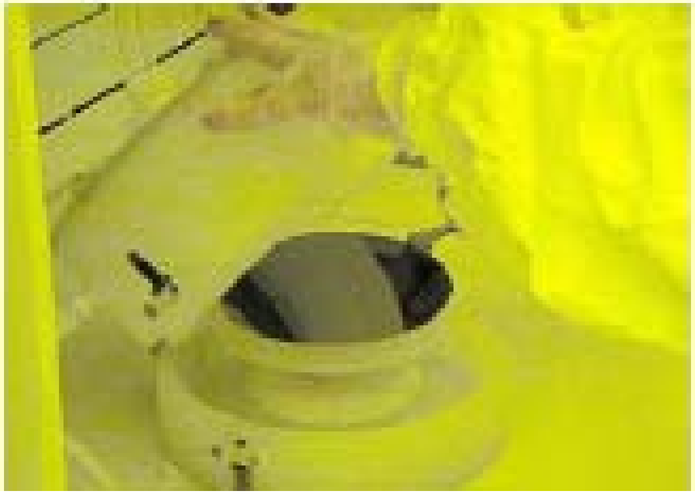
- Mask -types
  - Emulsion mask
  - Chromium mask

- Exposure methods
  - Optical
    - Contact: reduces lifetime of mask
    - ”Proximity”: 25 – 50 µm distance
    - Projection using complex optics
  - Electron beam (e-beam)
    - Direct patterning on wafer

Spin-on methods

- Material drop in centre is spinned on
  - For photo resist
    - Organic materials
      - Polyimides, 0.5 – 20 µm
      - **SU-8** (epoxy-based), > 200 µm
  - For dielectric isolators
- Thickness depends of
  - Concentration, viscosity, speed, time





Topographic height variations give problems

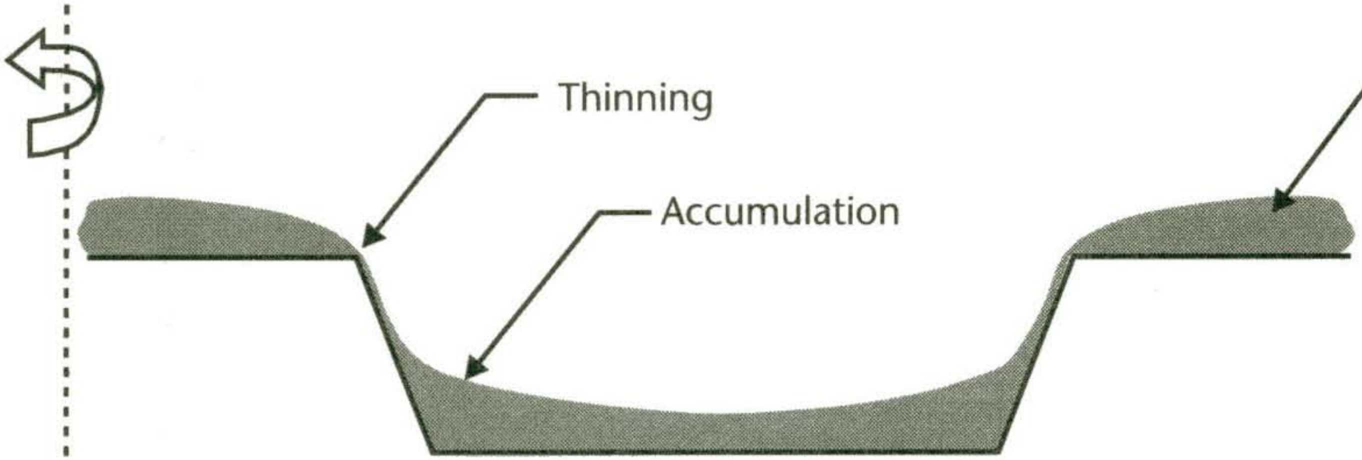
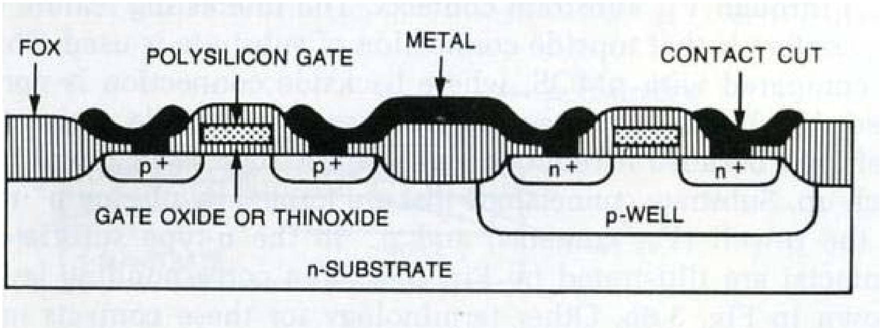


Figure 3.3 Undesirable effects of spin-coating resist on a surface with severe topographical height variations. The resist is thin on corners and accumulates in the cavity.

Maluf

Modify material properties: Diffusion

- Diffusion of impurities in semiconductors
  - Dope materials
    - Phosphorus (n+), Boron (p+)
  - ”Predeposition”,
    - ”ion implantation”
  - ”Drive-in” at high temp



- Type and concentration of dope materials determine electrical properties
  - Two mechanisms
    - **Diffusion current** due to concentration gradients of free charges (n, p)
    - **Drift of charges** due to electric field

Remove material: Etching

- Wet-etching or dry-etching

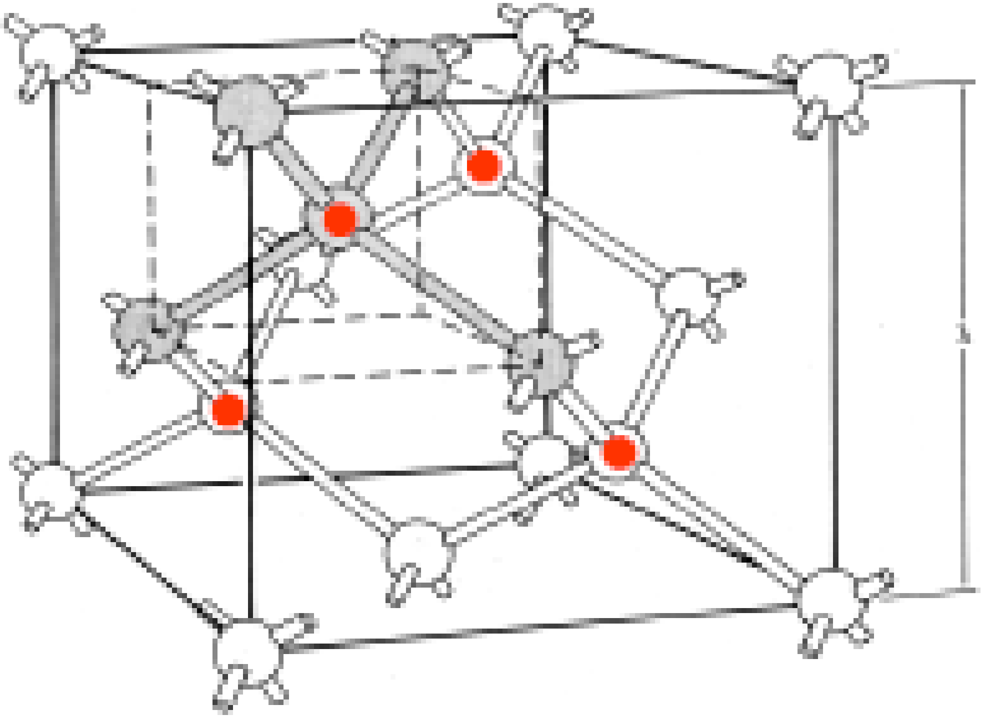
- **Wet-etching**
  - Deep etching of Si substrate is essential in bulk micromachining
  - Using liquids
  - Etching speed depends on:
    - Concentration of liquid, time, temperature
    - Not very precise!
  - Low cost batch processing
  - Both **isotropic** or **anisotropic** etching possible

Wet-etching

- **Isotropic** = uniform etching in all directions
  - **HF** or blends are usual (hydrofluoric acid)
  - 0.1 – 100 µm/min etch speed

- **Anisotropic** = etching faster along some directions
  - Etch speed depends of **crystal orientation**
  - **NaOH, KOH** used (sodium hydroxide, potassium hydroxide)
    - Silicon nitride used as mask for **KOH**

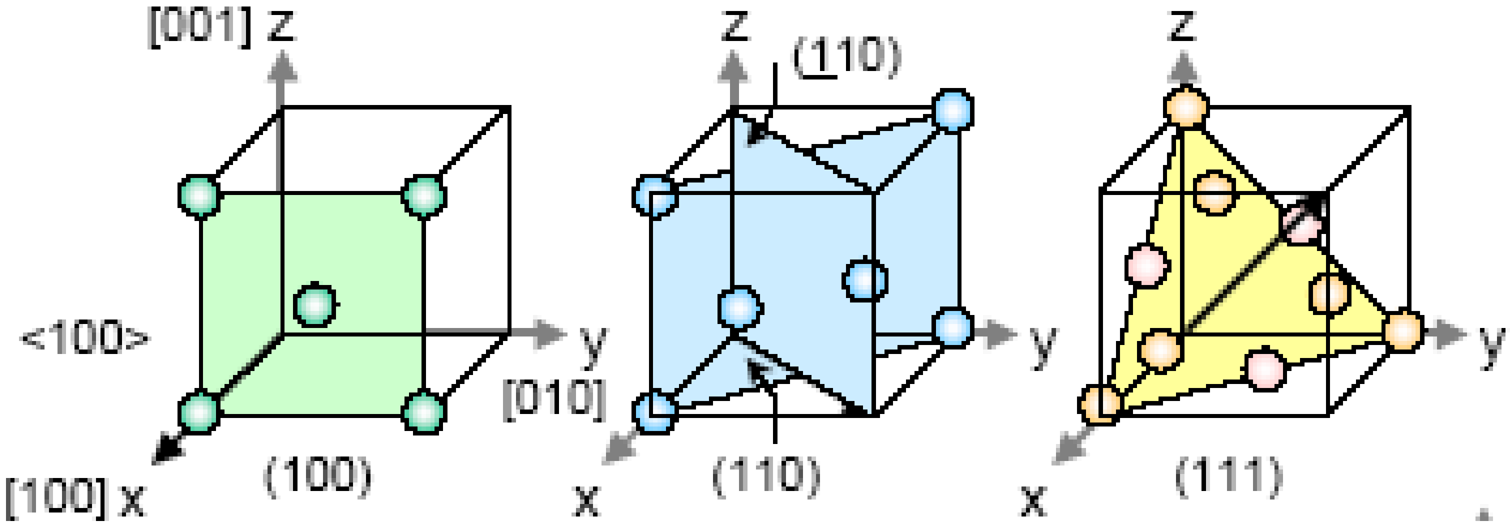
Crystal orientation in Si



Silicon crystal structure
$\lambda = 5.43$ Å

Wolf and Tauber

Crystal directions



Miller indekser: (plan), {familie av plan}, [retning], <familie av retninger>

Different etch methods

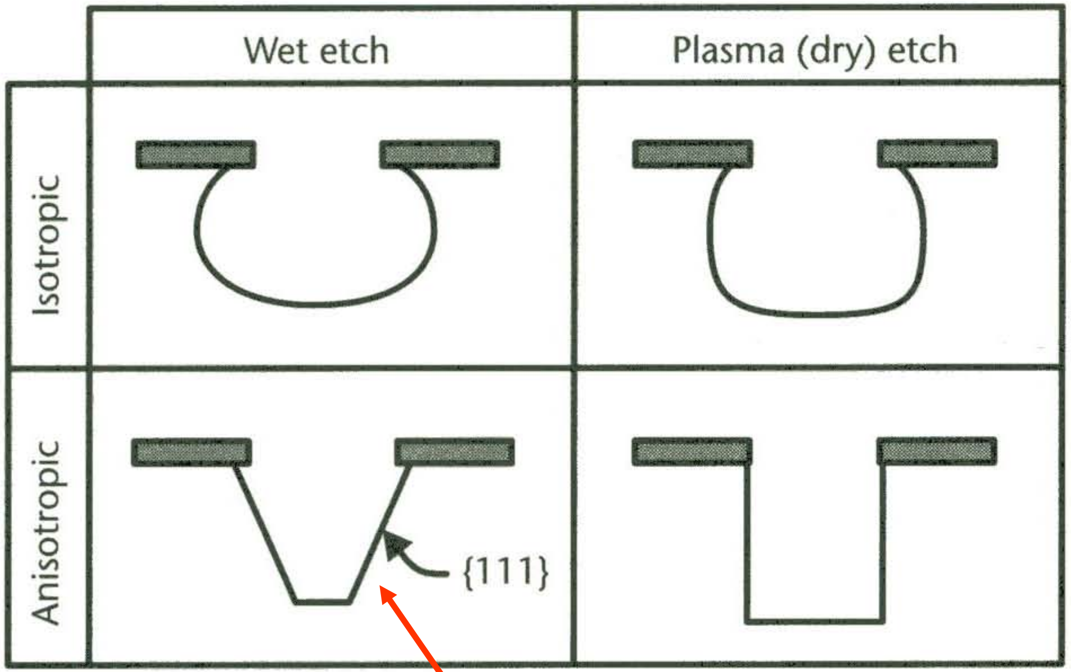


Figure 3.5 Schematic illustration of cross-sectional trench profiles resulting from four different types of etch methods.

54.7°

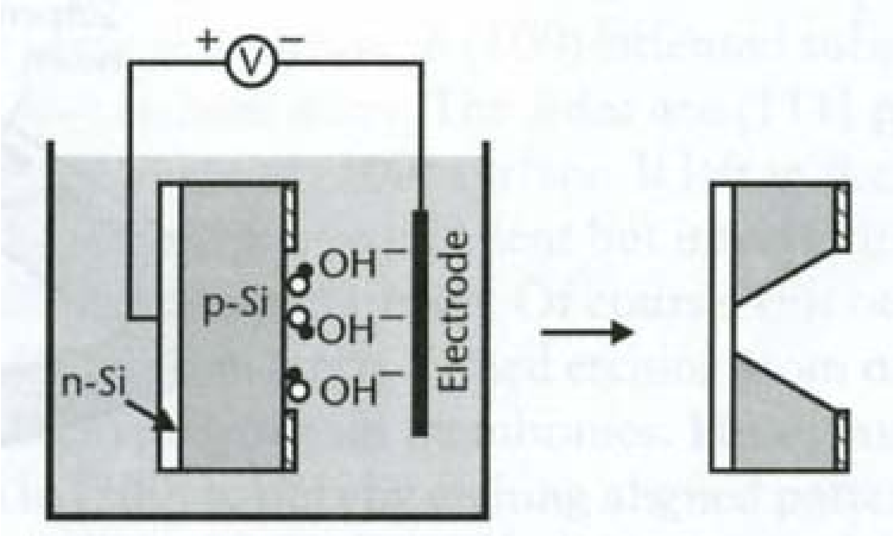
[Maluf]

Anisotropic wet etching

- **KOH** etching
  - {110} planes are etched 2x the speed of {100}
  - {111} plans are etched 100 x slower than {100}
    - Disagreement on reason: density of energy bands or formation of thin oxide layer?
- Used for making V-grooves
- Other anisotropic etch liquids
  - **TMAH**, ratio (100)/(111) = 10 – 35
    - TMAH = Tetramethylammonium hydroxide
    - SiO_2 used as a mask

Controlling etch depth

- Etch depth controlled by **electrochemical etching**
  - Precise growing of epi-layer
    - Ex. n-type on p-wafer
  - Apply electric potential
    - pn-diode reverse biased
  - p-material etched
  - Etching stops at pn-junction
    - Thin SiO2 layer formed
  - Used to define thickness of membranes



Dry-etching

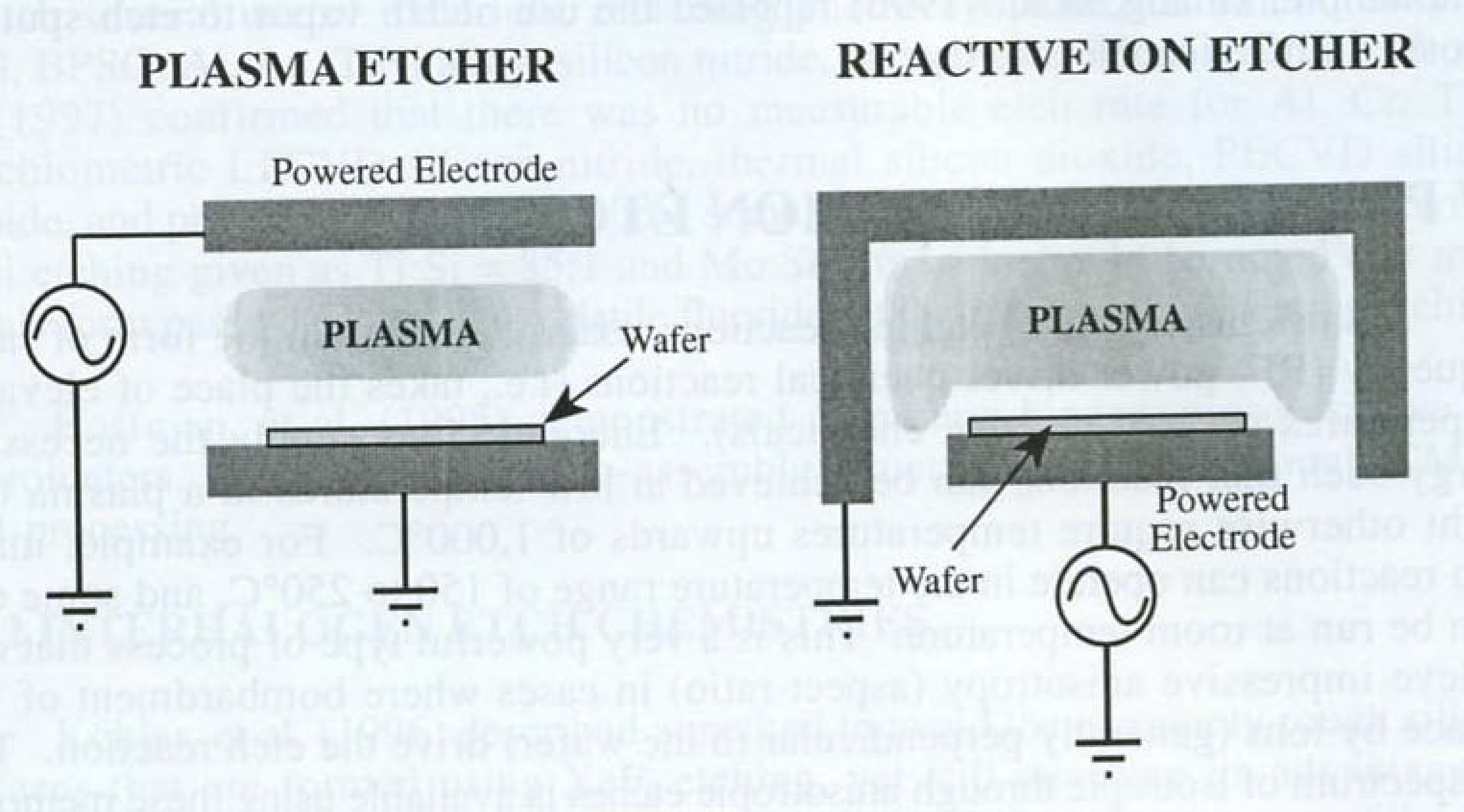
- 1. Vapor-phase etching
- 2. Plasma etching
- 3. Reactive Ion Etching
  - RIE
  - DRIE
- 4. Ion milling

Dry-etching, contd.

- **1. Vapor-phase etching**
  - Use reactive gases (”vapor”)
  - Both isotropic and anisotropic etching
- **2. Plasma etching**
  - *Plasma: ”electric neutral, highly ionized gas of ions, electrons and chemical reactive, neutral particles”*
    - Chemical reactive particles and ions are **accelerated** in an electric field towards the Si substrate
    - The **chemical reaction** at the surface is critical
    - Low temperature etching!
  - Etching Si, SiO_2, Si_3N_4, polysilicon, metals

Dry-etching, contd.

- **3. RIE – Reactive Ion Etching**
  - Ion beam generated in **plasma**
  - **Bombarding the Si-surface** with reactive particles
  - Low pressure
  - Anisotropy is possible
    - Vertical beam: vertical anisotropy
  - High etching speed

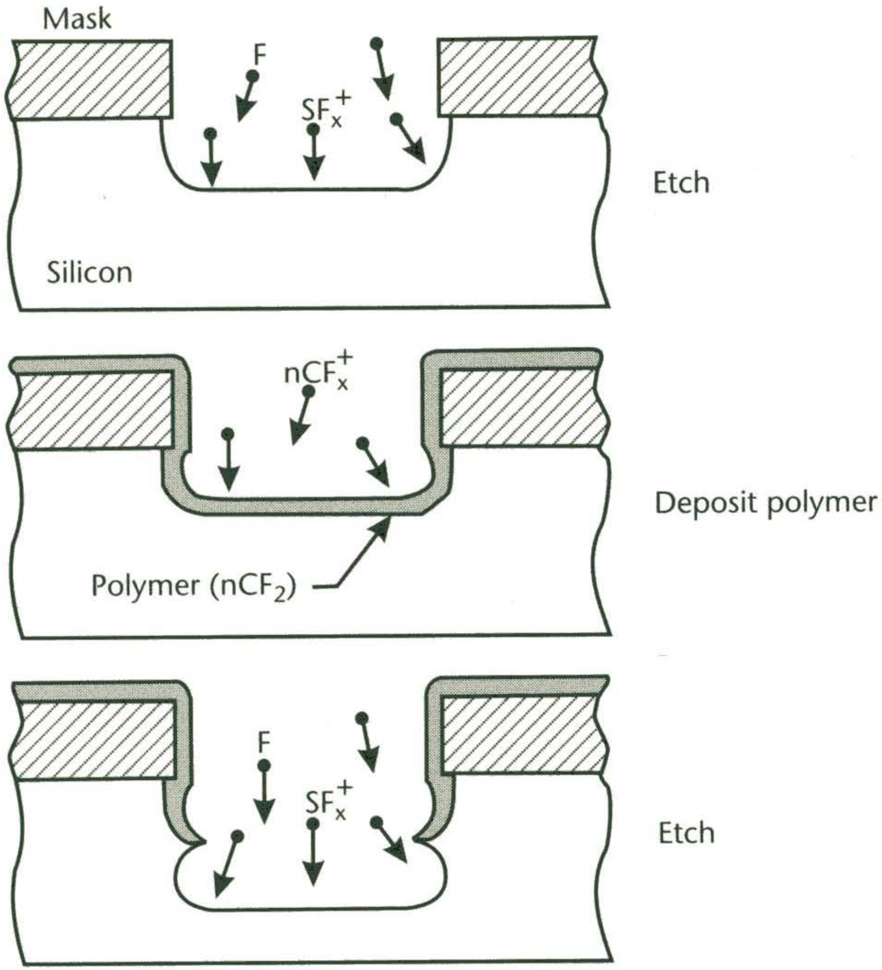

PLASMA ETCHER
Powered Electrode
PLASMA
Wafer
REACTIVE ION ETCHER
PLASMA
Powered Electrode
Wafer

[Kovacs]

DRIE

- **DRIE** – Deep Reactive Ion Etching (1995-)
  - – Vertical etching
  - – Can etch deep holes (> 500 µm) with almost perfect vertical sidewalls
  - – Bosch-method
    - Figure →
    - High ”aspect-ratio” obtainable
    - Etching and deposition every second step
      - – **Etch:** SF6, mostly at the bottom! (Sulfur hexafluoride)
      - – **Deposit:** polymer, C4F8 (Octafluorocyclobutane)

Bosch-process

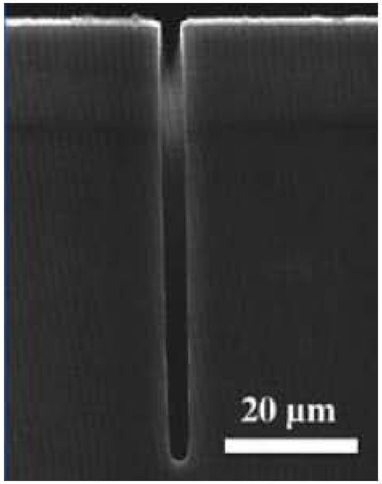


”Scalloped” hole

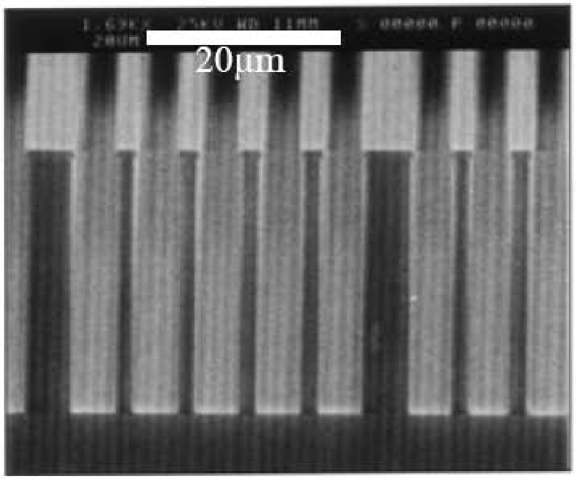
Figure 3.12 Profile of a DRIE trench using the Bosch process. The process cycles between an etch step using SF_6 gas and a polymer deposition step using C_4F_8. The polymer protects the sidewalls from etching by the reactive fluorine radicals. The scalloping effect of the etch is exaggerated.

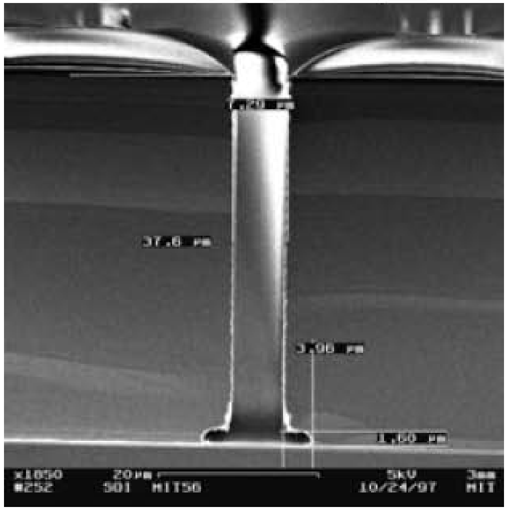
Maluf

Deep RIE Examples



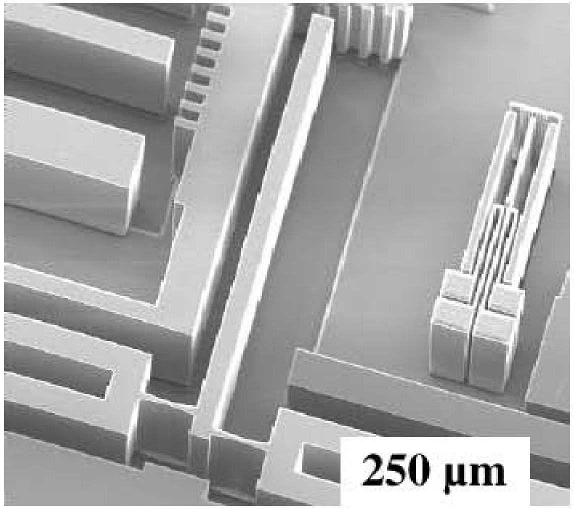
STS 1999





Ayon et al., 1998 (MIT)

Klaassen et al., 1995 (Stanford)



4. Ion milling

- Inert gas (Argon) accelerated towards substrate
  - ~ 1kV
- No chemical reaction, but milling!
  - **All materials can be etched by this method**
- Vertical etch profile
- Lower etch speed than RIE

Building of structures

- **Deposition** of thin or thick layers (”films”)
  - Conductors: Al, Cu
  - Semiconductors: Si, polySi
  - Isolators: SiO2, Si3N4
  - Polymers (organic)
- **Bonding-techniques**
  - Interconnecting wafers

Deposition

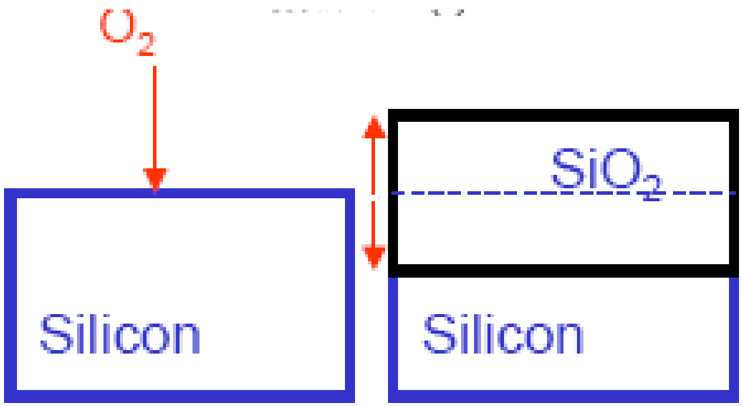
- Adding films on substrate surface
  - **Structural layers**
  - **Sacrificial layers (”spacers”)**
- Techniques
  - a. Epitaxial growth
  - b. Oxidation
  - c. Vaporization
  - d. Chemical Vapor Deposition, CVD
  - e. Sputtering
  - f. Moulding

a. Epitaxial growth

- Epitaxial growth
  - – Heavily used in IC industry
  - – Growth of **crystalline** Si on a Si-wafer
    - Vapor-phase chemical deposition > 800 °C
    - Gives the same crystalline orientation as the wafer
    - Doped materials used: arsenic, phosphorus, boron
    - Thin, 1-20 μm
  - – Growth of **polycrystalline** Si material on SiO_2
  - – Growth of Si on Sapphire (SOS)

b. Oxidation of Si

- Thermal oxidation
  - **High quality** thermal grown oxide
    - Dry O_2 or vapor at **high temp**, 850-1150 °C
  - Thermal oxidation generates compressive stress
    - Volume of SiO_2 is larger than Si
    - Different Thermal Coefficients of Expansion, TCE



c. Vaporization

- Heating the material source to high temp
  - → vapor → condensation → **film deposition** on wafer
  - ~Vacuum
- Vaporization by thermal heating or e-beam bombardment
- Is a directive deposition method
  - The source is relatively small
  - Material deposited at a <u>specific angle</u>
  - Gives bad step coverage (corners, sidewalls)
- Most films get **tensile** stress (stretched)

d. CVD

- **Chemical Vapor Deposition**
  - **Chemical reaction** between vapor and heated surface
  - High temperature process
  - Gives **high quality** thin films
    - PolySi, dielectrics, metal films
  - Influenced by: temperature, pressure, vapor-flow, material

- Categories
  - **PECVD**, Plasma-enhanced, ~ 300 °C or lower
    - Plasma excitation using RF
    - Good control of stress
  - **LPCVD**, Low-pressure, 400-800 °C

Deposition of **polysilicon**

- Poly is an attractive mechanical material for surface micromachining
  - Various thicknesses may be fabricated (nm → µm)

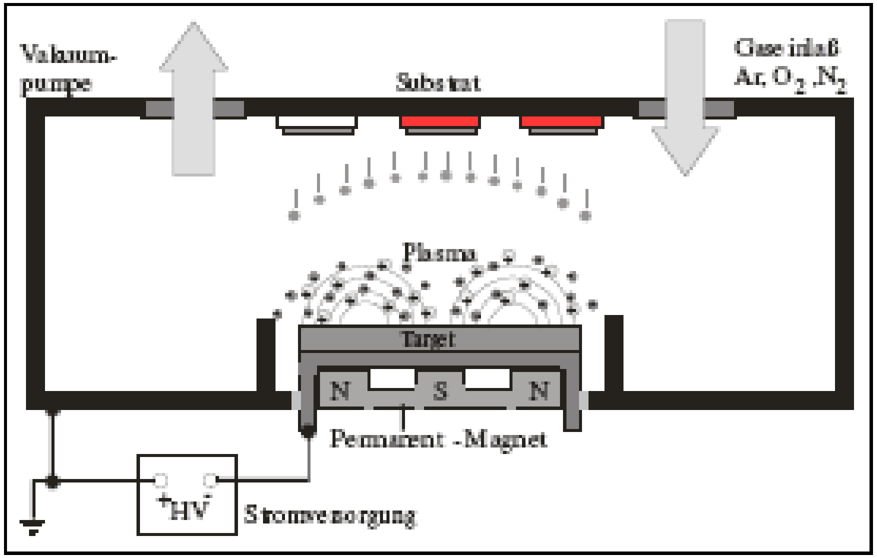
- Deposition using LPCVD
  - Crystalline grain structure achieved when > 630 °C
  - Temperature determines **tensile** or **compressive** stress
  - **”Annealing”** at 900 °C reduces stress

Deposition of insulators

- Deposition of **SiO2**
  - LPCVD or PECVD may be used
  - **LTO = low-temp oxide,** < 500 °C, amorphous
    - **The quality is not as good as for a thermal grown oxide!**
    - Used as isolator or sacrificial layer
    - Etched using HF
- Deposition of **Si_3N_4**
  - Used for passivation
  - Used as mask for some etchings (KOH)

e. Sputter deposition

- **Method:**
  - **Target** material bombarded with a flow of inert gas ions (Ar+)
  - ~ vacuum
  - Released atoms deposited on the wafer
- **Low temperature** <150 °C
  - Many applications in MEMS
- **Many types of materials**
  - Both conducting and isolating materials can be sputtered
    - Thin metal films, glass, piezoelectric films (PZT)

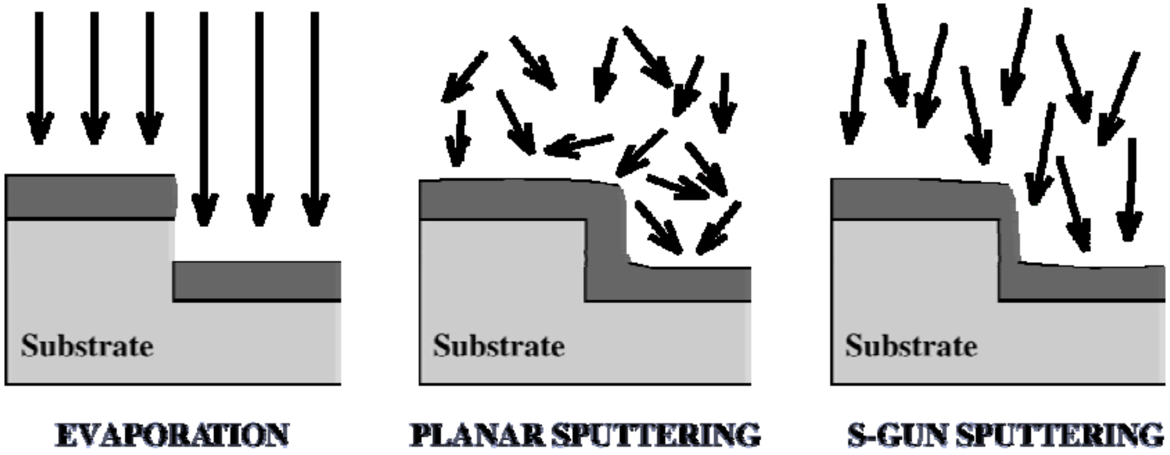


[Futura Sciences]

Sputter deposition, contd.

- Alternative type: **reactive sputtering**
  - – Nitrogen or oxygen gas is added, **reacts!**
- Direction ”randomness” can be achieved
  - – When sputter “target” (source) is larger than wafer
  - – Gives good step coverage
- Good stress control
  - – Stress level depends of sputter power and pressure in chamber
    - *Tensile stress:* low power, high pressure
    - *Compressive stress:* high power, low pressure

Sputtering vs. Evaporation



Geometry of evaporation and sputtering chambers (as well as electromagnetic fields) determine *directionality* of deposition:

Good or bad step coverage (can be advantage or disadvantage)

Figure: G. Kovacs, 1996.

”Adhesion layer”

- Many metals have bad adhesion to Si, SiO_2, Si_3N_4
  - Peeling off

- Add a thin layer to increase **adhesion**
  - Adhesion layers: chromium (Cr), titanium (Ti)
  - Gold, silver, platinum to be deposited

  - Avoid oxidation of the adhesion layer during processing, - will destroy adhesion

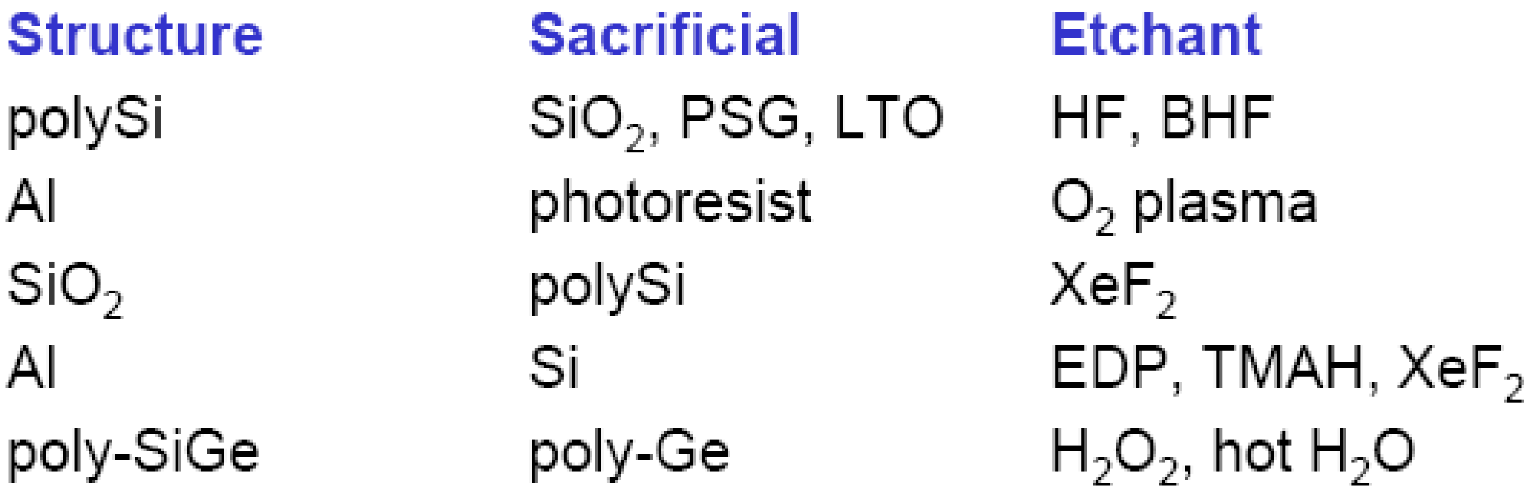
f. Moulding

- LIGA = a moulding method
    - **“Lithographie, Galvanoformung, Abformung”**
  - X-ray used for mask exposure
  - “Galvanoforming” → a metal mould is formed
  - Moulding → components are formed
    - **Plastic**, metal, ceramic –components

- + Flexible method
- ÷ X-ray used, high fabrication cost
- + Gives high aspect ratio, 3D components!
- ÷ Limited in versatility
  - because 3.rd dimension is limited to be vertical

- Thick **photoresist** may also be used to build a mould

Structural – sacrificial layers



Structure	**Sacrificial**	**Etchant**
polySi	SiO_2, PSG, LTO	HF, BHF
Al	photoresist	O_2 plasma
SiO_2	polySi	XeF_2
Al	Si	EDP, TMAH, XeF_2
poly-SiGe	poly-Ge	H_2O_2, hot H_2O

[Srinivasan]

[Varadan:]

polySi	SiO2
Polyimide	aluminum
Si3N4	polySi
Wolfram	SiO2

Summary: MEMS-specific steps

- Methods **especially** developed for MEMS
  - Anisotropic chemical wet-etching
  - Deep reactive ion-etching, RIE, DRIE
  - Etching of sacrificial layer
  - Moulding

  - ”Wafer bonding”
  - “Electroplating”
  - ”Critical-point drying”

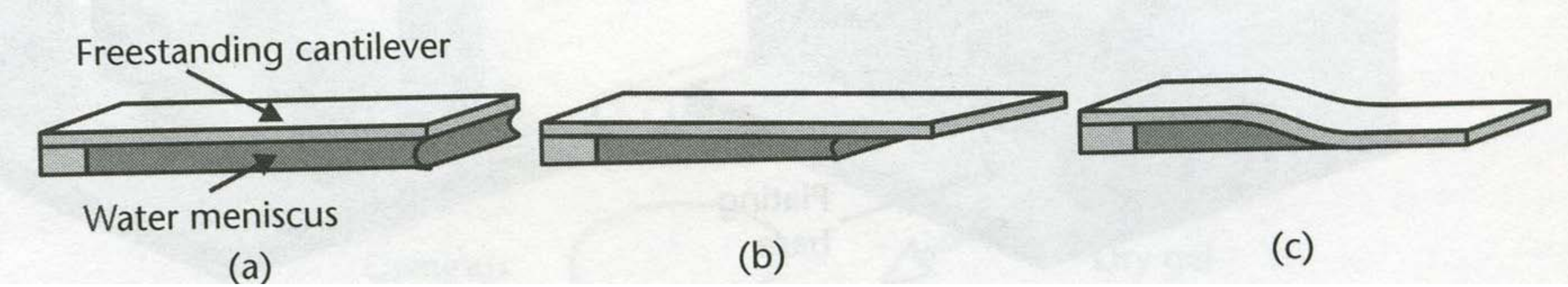
MEMS advanced process steps

- **Anodic bonding**
  - Si-wafers are bonded together, glass – Si
    - Used for pressure sensors (jmfr. MultiMEMS →)
  - 200 – 500 °C, 500 – 1500 V
  - Glass has negative ions at the contact interface with Si

- **Electroplating**
  - Thin **seed layer** is deposited on the Si substrate
    - *“A thin metal layer is **electroplated** on the surface using either chemical or electrolytic plating” (Norw: “plettering”)*
  - Plating by using gold, copper, nickel etc.
  - May give thick layers, 5 – 100 µm
  - May be used for **moulding:** - a method for making a **mould**

Supercritical drying

- **Removing sacrificial layer** is problematic
  - By HF etches → water rinsing is used
  - The water may stick to the structures due to the surface tension
    - Thin wafer (”meniscus”) is formed
  - The volume of the liquid decreases when dried
  - Structure is pulled down → **”stiction”** → **structure must be released!**
- **”Supercritical Point Drying”:** avoids forming of meniscus
  - Wet wafer is placed in a methanol chamber
  - Liquid CO2 is added → the blend is removed →CO2 rest is heated to the supercritical region (transition: gas - liquid) → the gas is removed



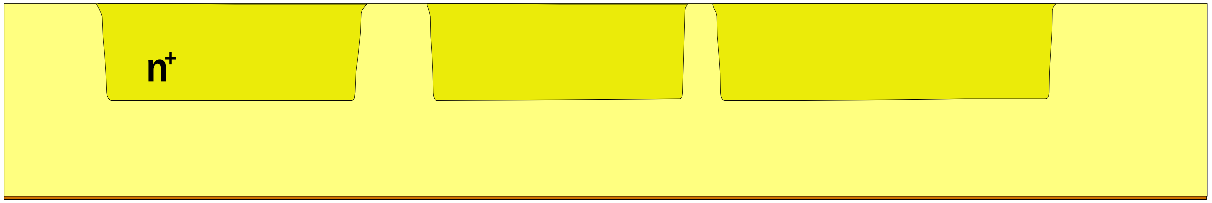
Examples of processes

- Bulk micromachining
  - **MultiMEMS from InfineonSensoNor →**

MPW Process (1)

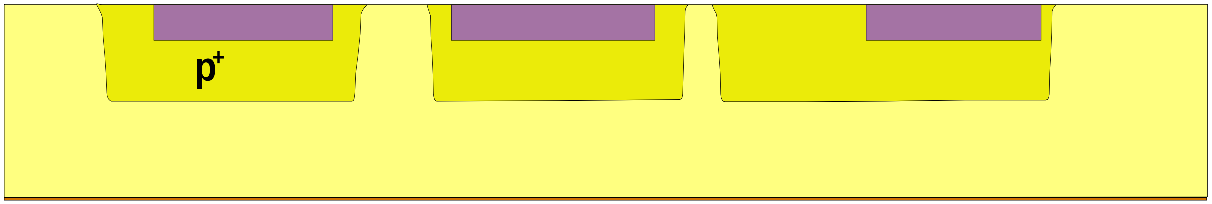
- NOWEL :

  n impl. + diff.



- BUCON :

  p impl. + diff.

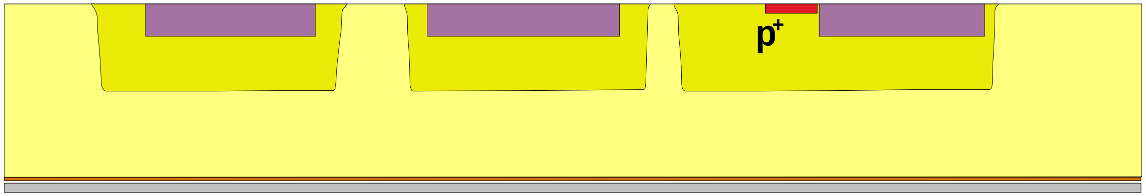


The following slides are from MultiMEMS, SensoNOR/Europractice

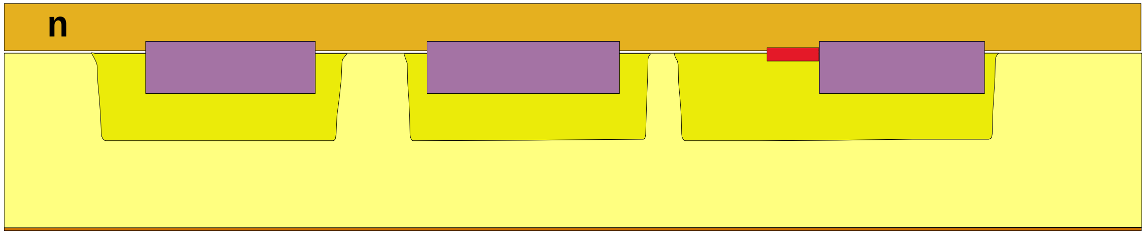
MPW Process (2)

- BURES :

  p impl. + diff.



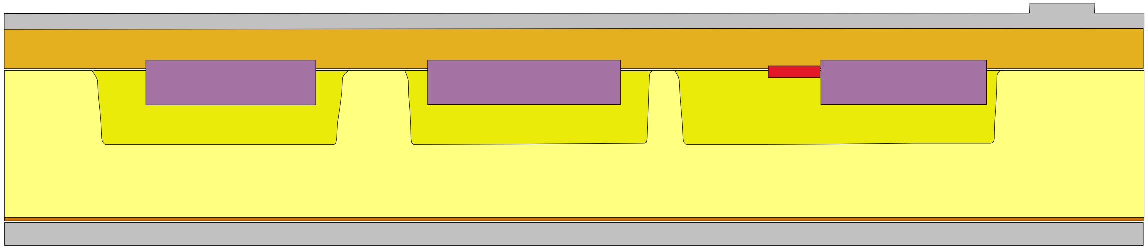
- n epi



MPW Process (3)

- TIKOX :

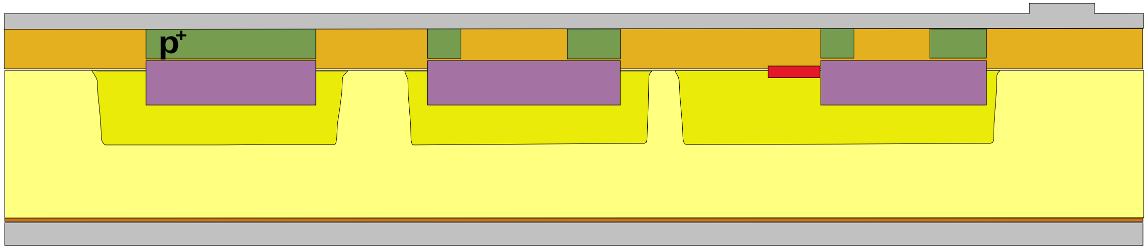
  2 oxidations



- SUCON :

  p impl. +

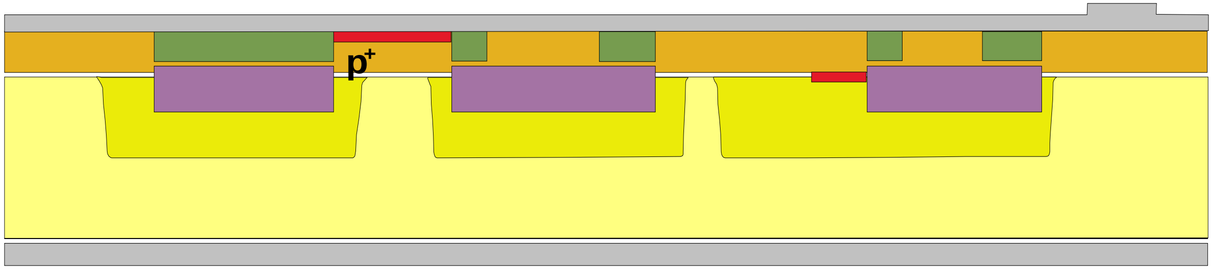
  diff.



MPW Process (4)

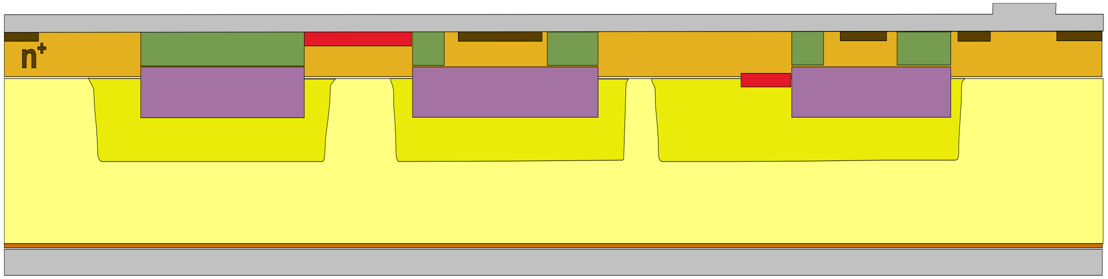
- SURES :

  p impl.



- NOSUR :

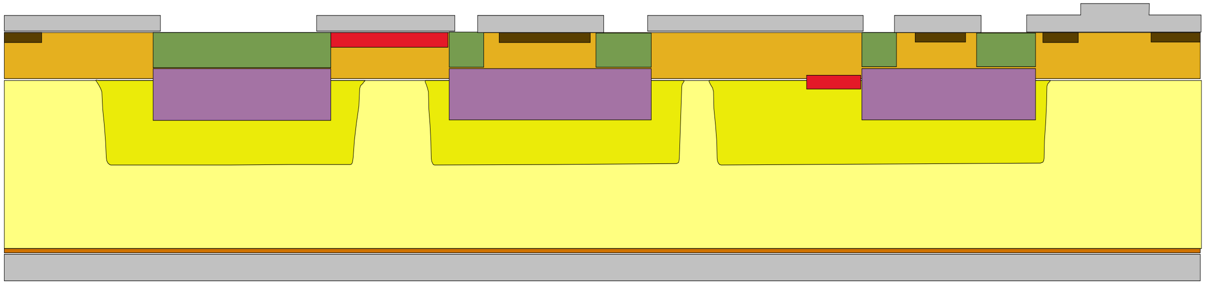
  n impl. + diff



MPW Process (5)

- COHOL :

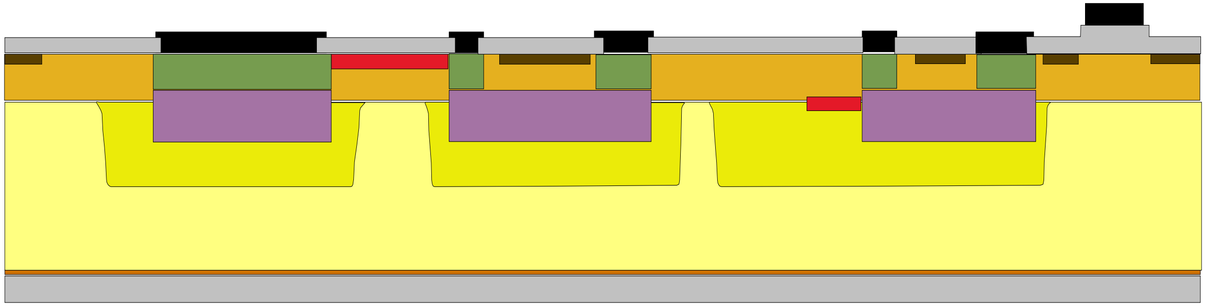
  oxide etch



- MCOND :

  Al sputter +

  pattern



MPW Process (6)

- BETCH :

  TMAH

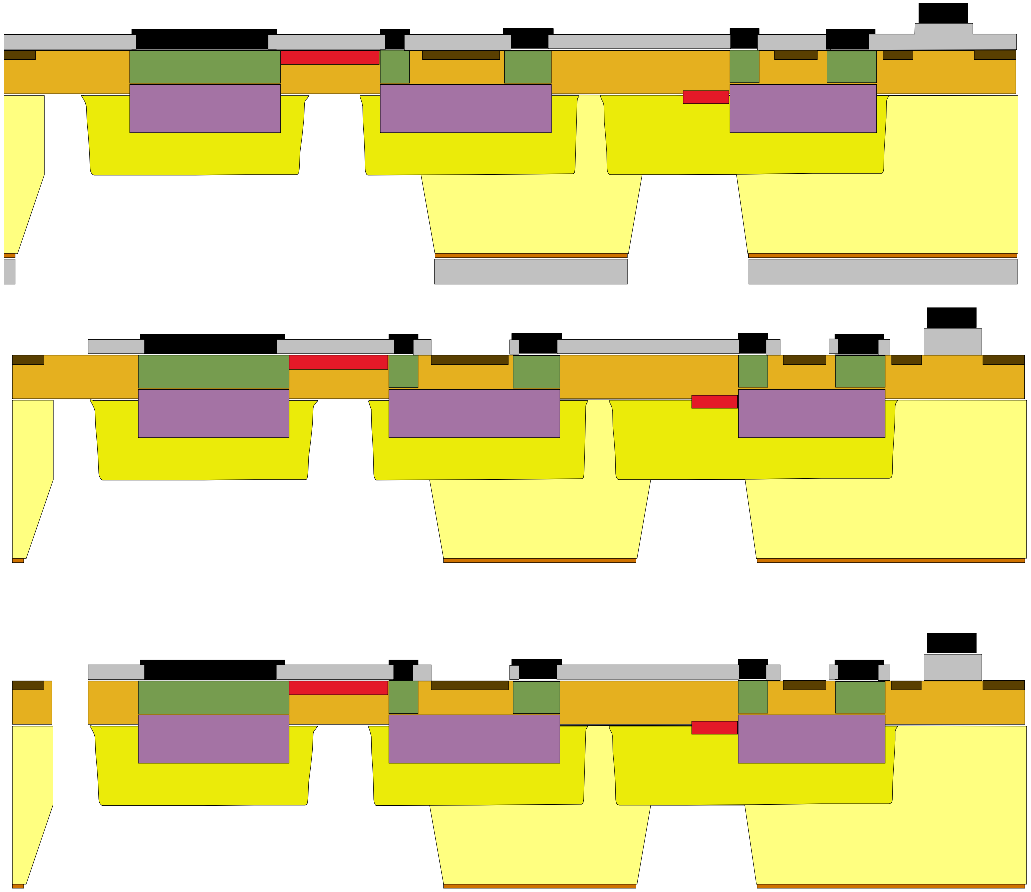
  etch

- NOBOA :

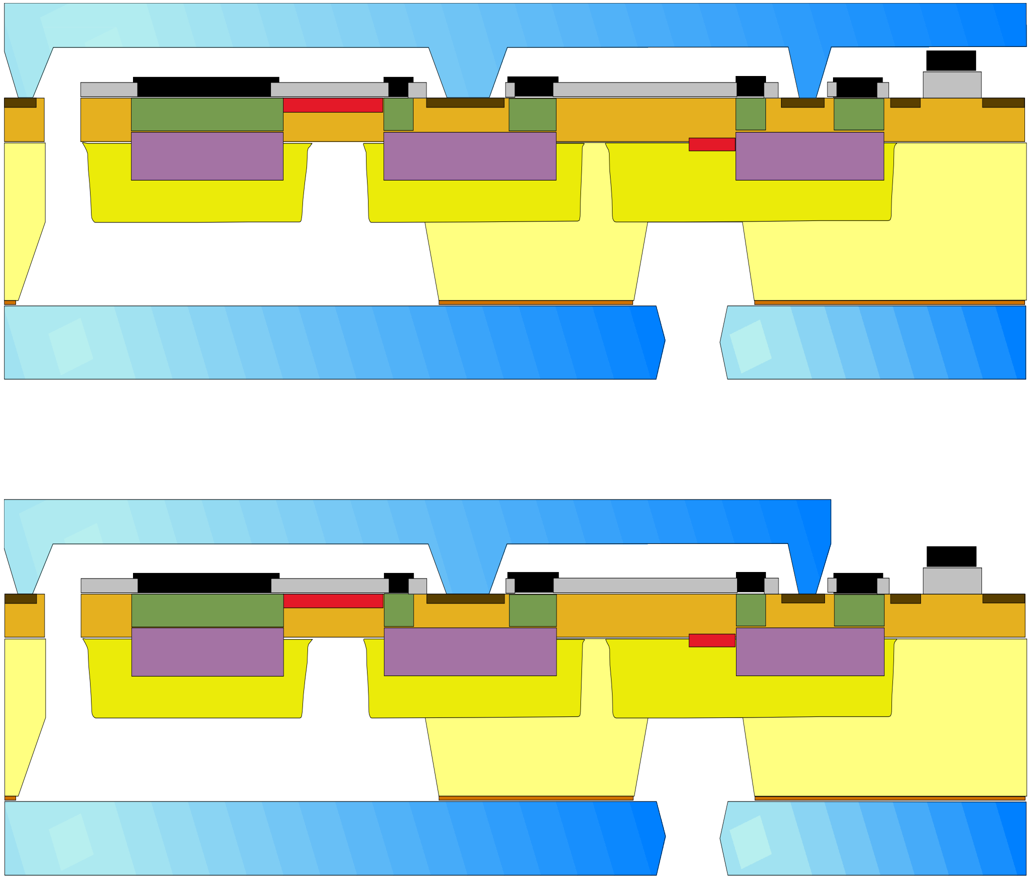
  oxide etch

- RETCH :

  dry etch



MPW Process (7)

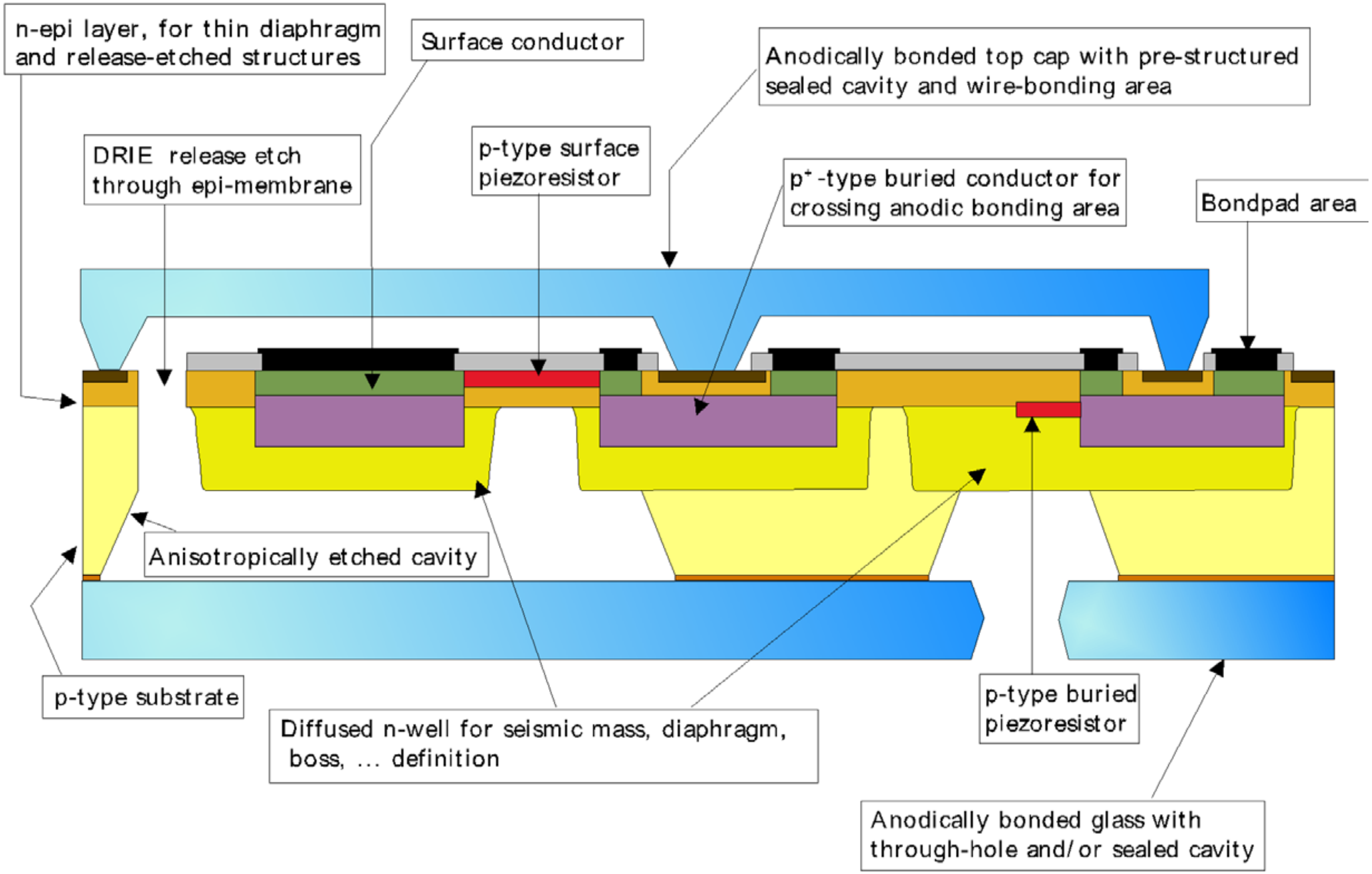


- TOGE; BOGEF; BOGEB :

  wet etching of glass + anodic bonding

- Dicing

Cross section overview



n-epi layer, for thin diaphragm and release-etched structures

Surface conductor

Anodically bonded top cap with pre-structured sealed cavity and wire-bonding area

DRIE release etch through epi-membrane

p-type surface piezoresistor

p^+-type buried conductor for crossing anodic bonding area

Bondpad area

Anisotropically etched cavity

p-type substrate

Diffused n-well for seismic mass, diaphragm, boss, … definition

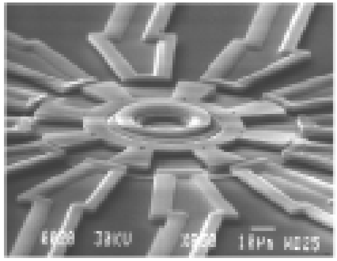
p-type buried piezoresistor

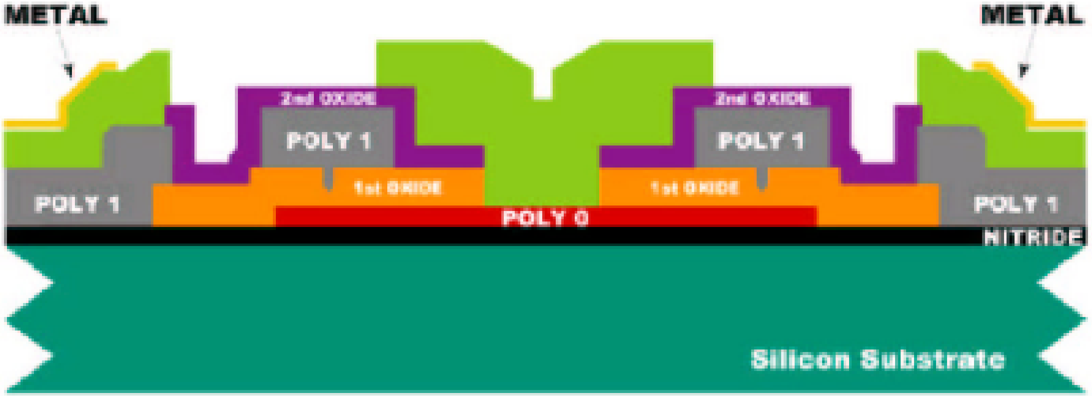
Anodically bonded glass with through-hole and/or sealed cavity

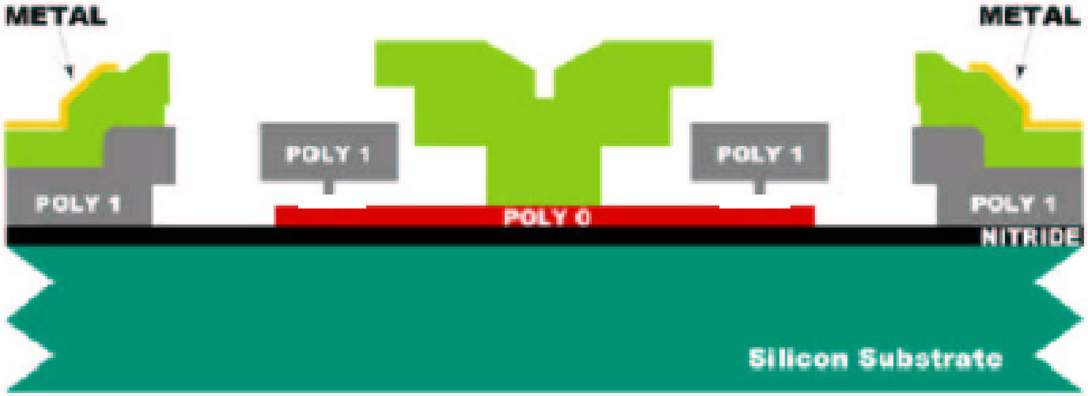
Examples of processes

- Surface micromachining
  - **polyMUMPs from MEMSCAP →**

MUMPS Micromotor







Følgende slides fra polyMUMPs:

FIGURE 1.2. The surface of the starting n-type (100) wafers are heavily doped with phosphorus in a standard diffusion furnace using POCl 3 as the dopant source. A 600 nm blanket layer of low stress silicon nitride (Nitride) is deposited followed by a blanket layer of 500 nm polysilicon (Poly 0). The wafers are then coated with UV-sensitive photoresist.

FIGURE 1.3. The photoresist is lithographically patterned by exposing it to UV light through the first level mask (POLY0) and then developing it. The photoresist in exposed areas is removed leaving behind a patterned photoresist mask for etching.

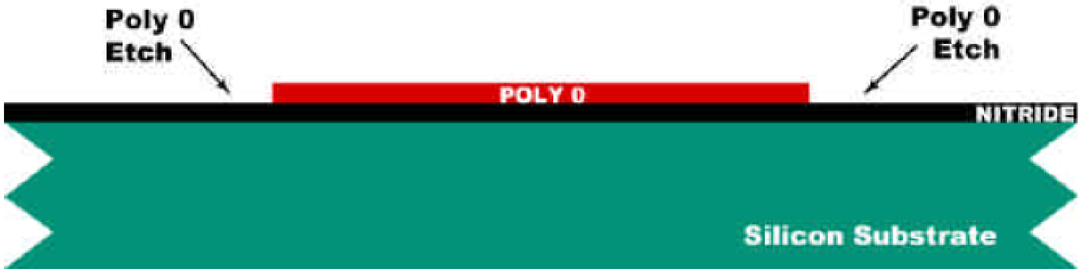


FIGURE 1.4. Reactive ion etching (RIE) is used to remove the unwanted polysilicon. After the etch, the photoresist is chemically stripped in a solvent bath. This method of patterning the wafers with photoresist, etching and stripping the remaining photoresist is used repeatedly in the PolyMUMPs process.

FIGURE 1.5. A 2.0 μm layer of PSG is deposited on the wafers by low pressure chemical vapor deposition (LPCVD). This is the first sacrificial layer.

FIGURE 1.6. The wafers are coated with photoresist and the second level (DIMPLE) is lithographically patterned. The dimples, 750 nm deep, are reactive ion etched into the first oxide layer. After the etch, the photoresist is stripped.

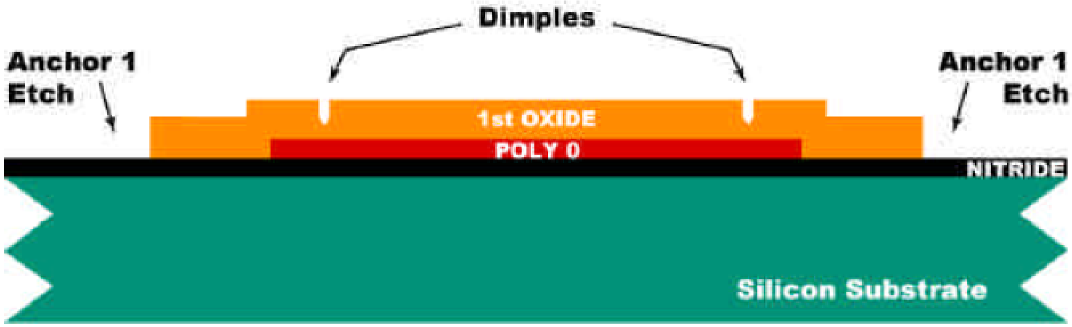


FIGURE 1.7. The wafers are re-coated with photoresist and the third level (ANCHOR1) is lithographically patterned. The unwanted oxide is removed in an RIE etch and the photoresist is stripped.

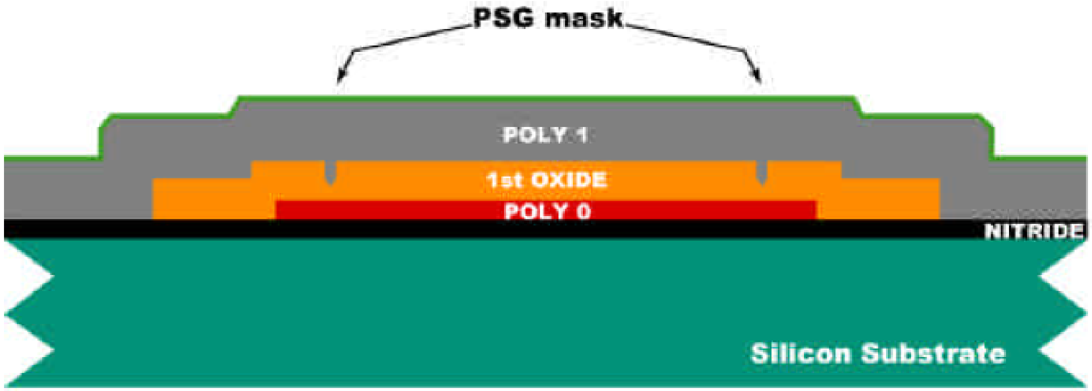


FIGURE 1.8. A blanket 2.0 µm layer of un-doped polysilicon is deposited by LPCVD followed by the deposition of 200 nm PSG and a 1050°C/1 hour anneal. The anneal serves to both dope the polysilicon and reduce its residual stress.

FIGURE 1.9. The wafer is coated with photoresist and the fourth level (POLY1) is lithographically patterned. The PSG is first etched to create a hard mask and then Poly 1 is etched by RIE. After the etch is completed, the photoresist and PSG hard mask are removed.

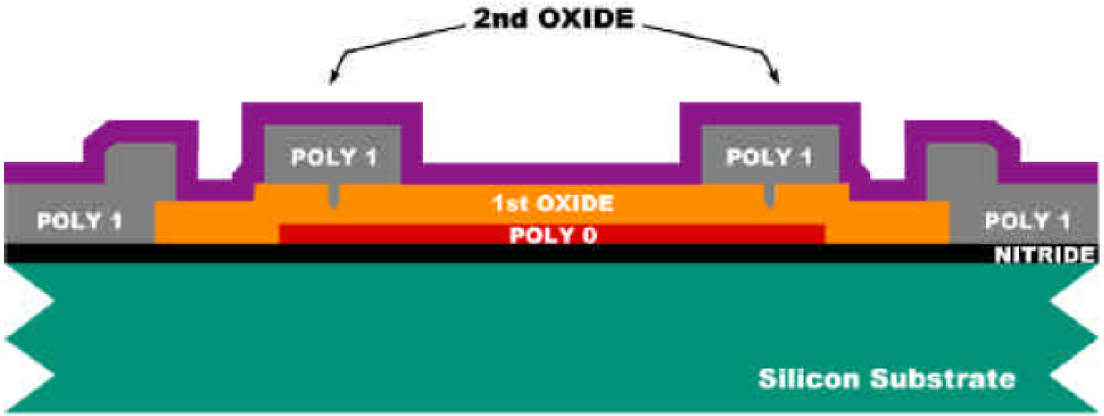


FIGURE 1.10. The Second Oxide layer, 0.75 µm of PSG, is deposited on the wafer. This layer is patterned twice to allow contact to both Poly 1 and substrate layers.

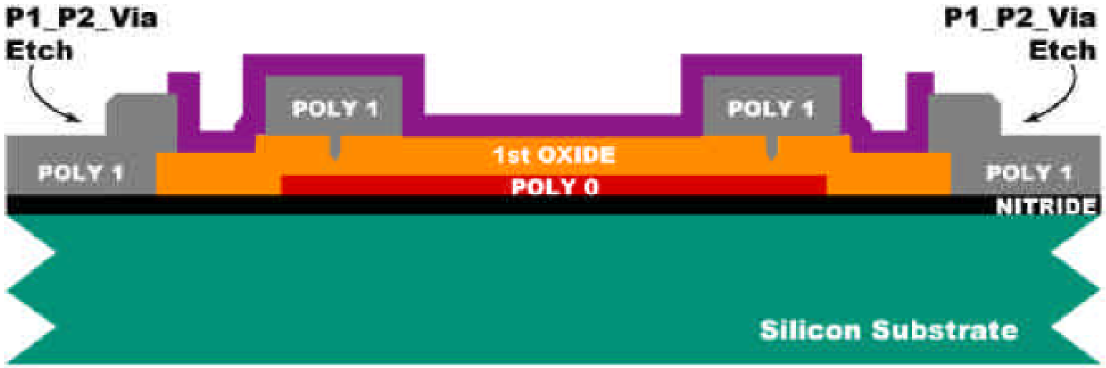


FIGURE 1.11. The wafer is coated with photoresist and the fifth level (POLY1_POLY2_VIA) is lithographically patterned. The unwanted Second Oxide is RIE etched, stopping on Poly 1, and the photoresist is stripped.

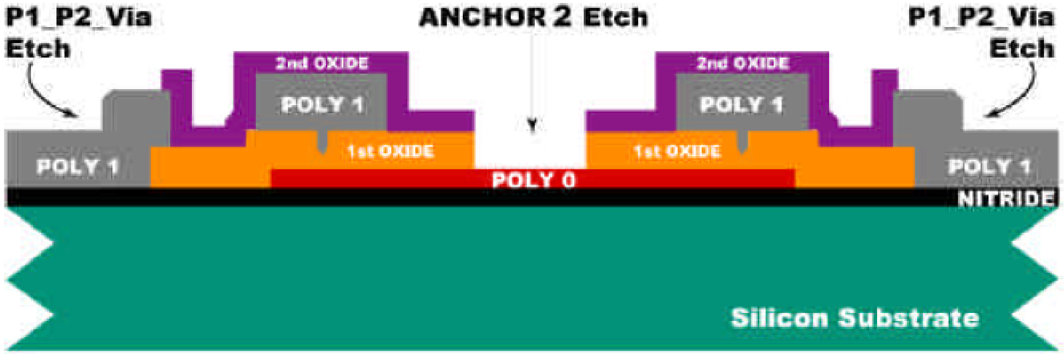


FIGURE 1.12. The wafer is re-coated with photoresist and the sixth level (ANCHOR2) is lithographically patterned. The Second and First Oxides are RIE etched, stopping on either Nitride or Poly 0, and the photoresist is stripped. The ANCHOR2 level provides openings for Poly 2 to contact with Nitride or Poly 0.

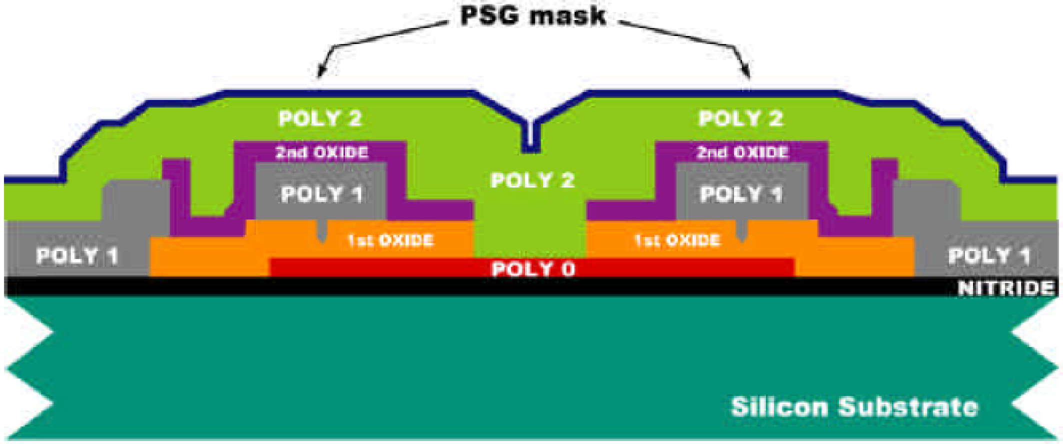


FIGURE 1.13. A 1.5 μm un-doped polysilicon layer is deposited followed by a 200 nm PSG hardmask layer. The wafers are annealed at 1050°C for one hour to dope the polysilicon and reduce residual stress.

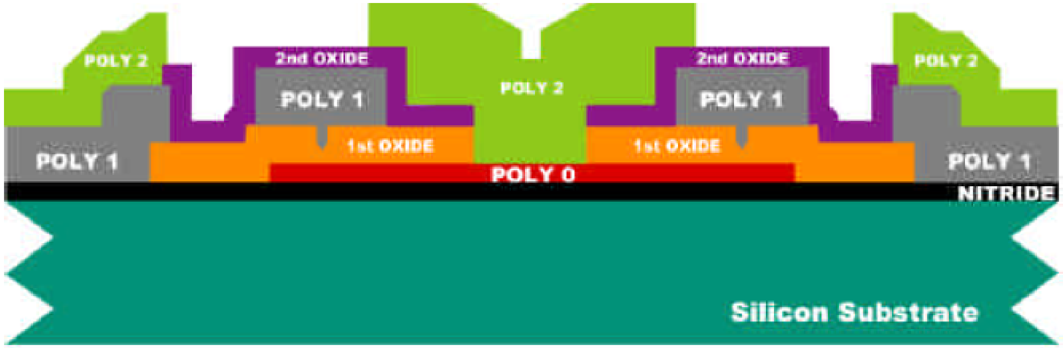


FIGURE 1.14. The wafer is coated with photoresist and the seventh level (POLY2) is lithographically patterned. The PSG hard mask and Poly 2 layers are RIE etched and the photoresist and hard mask are removed. All mechanical structures have now been fabricated. The remaining steps are to deposit the metal layer and remove the sacrificial oxides.

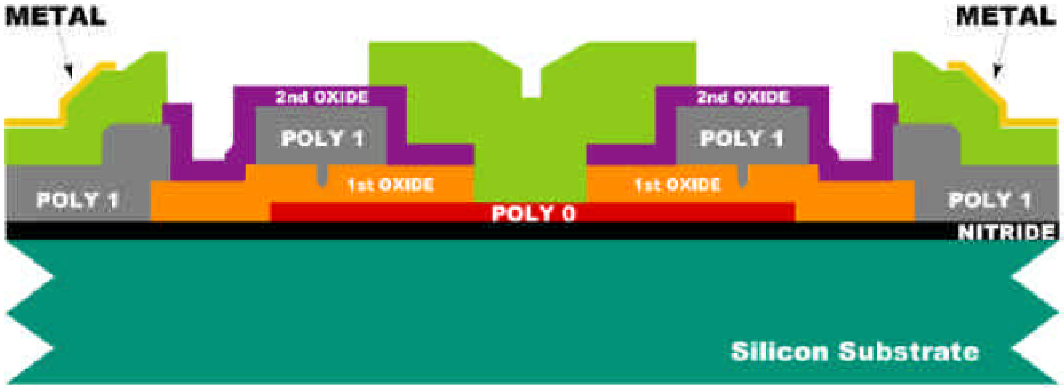


FIGURE 1.15. The wafer is coated with photoresist and the eighth level (METAL) is lithographically patterned. The metal (gold with a thin adhesion layer) is deposited by lift-off patterning which does not require etching. The side wall of the photoresist is sloped at a reentrant angle, which allows the metal to be deposited on the surfaces of the wafer and the photoresist, but provides breaks in the continuity of the metal over the reentrant photoresist step. The photoresist and unwanted metal (atop the photoresist) are then removed in a solvent bath. The process is now complete and the wafers can be coated with a protective layer of photoresist and diced. The chips are sorted and shipped.

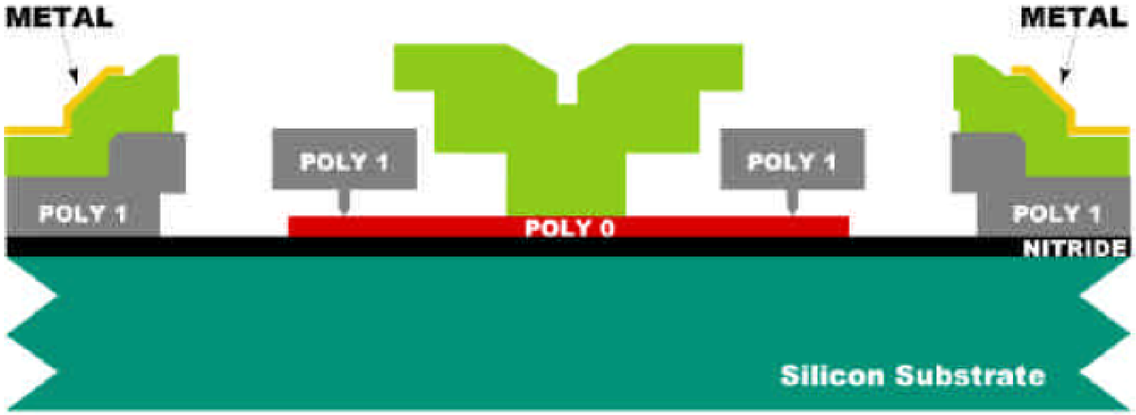
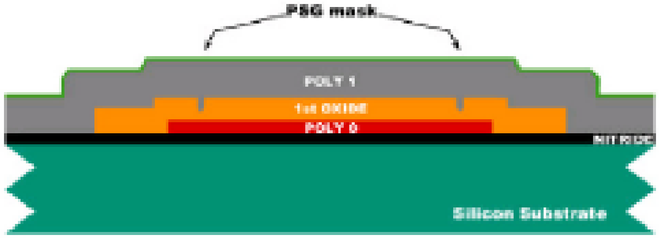
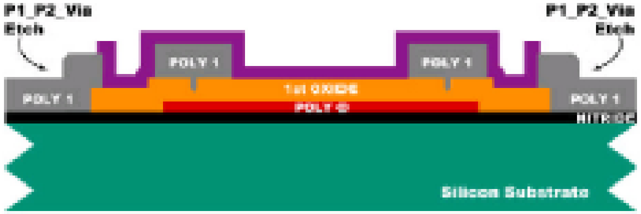
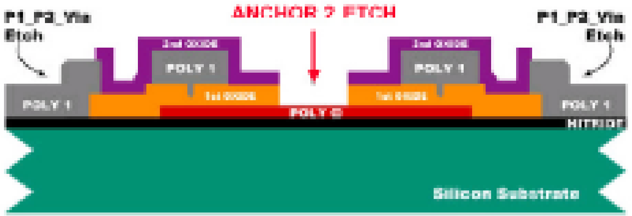


FIGURE 1.16. The structures are released by immersing the chips in a 49% HF solution. The Poly 1 "rotor" can be seen around the fixed Poly 2 hub. The stacks of Poly 1, Poly 2 and Metal on the sides represent the stators used to drive the motor electrostatically.

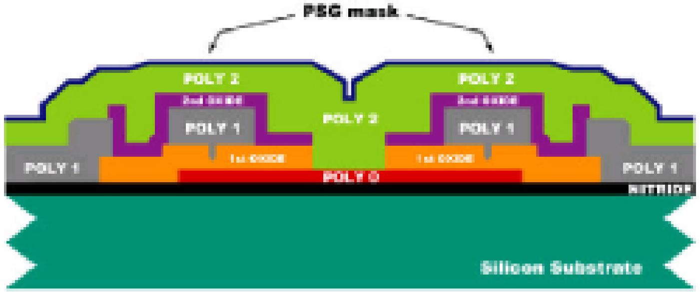
MUMPS Process Flow I

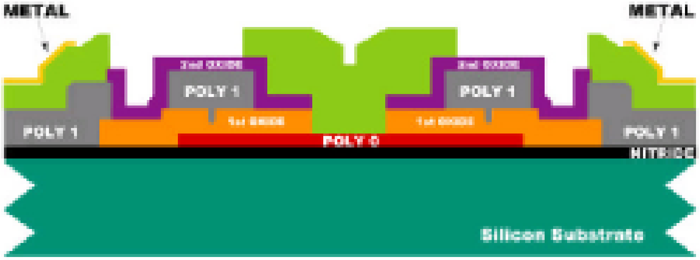


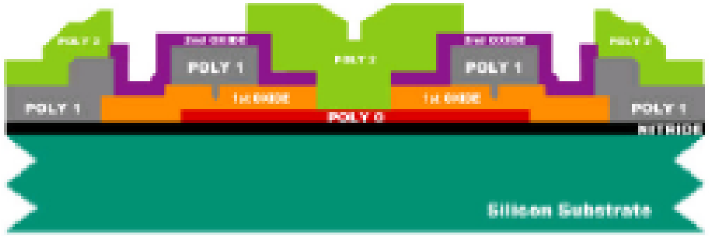


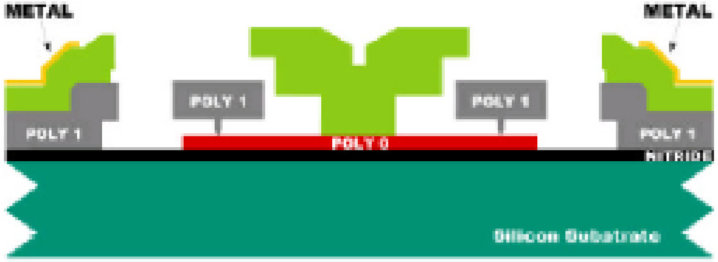


MUMPS Process Flow II









Examples from SINTEF MiNaLab

Process highlights

- "Full MEMS" processing capabilities
- 100 & 150mm wafer diameter
- Automatic lithography lines
- PECVD deposition of Si_3N_4 and SiO_2
- Dry etching of Al, Poly-Si, Si_3N_4 and SiO_2
- Deep Reactive Ion Etching of silicon
- Wet etching of silicon
- Advanced wafer bonding technologies
- Deposition of Au, Al, Ni, NiCr, Ti, etc
- Automatic visual inspection
- Full automatic electric wafer test
- Wafer dicing

Processing equipment

- Diffusion / oxidation furnaces
  - Diffusion
  - Annealing
  - Oxidation
  - LPCVD poly-Si
  - LPCVD Si3N4
  - POCl3
  - SiC tube for growth of extra thick oxide

Processing equipment

- Mask aligners
  - Contact / proximity printing
  - Front to back-side alignment
  - Throughput of 170 wafers / hour

- Automatic resist coaters
  - Double sided coating
  - fully automated

Processing equipment

- PECVD deposition
  - Si3N4
  - SiO2
  - Amorphous silicon
- RIE etching
  - Silicon (Bosch / Cryo)
  - SiO2
  - Si3N4
  - Poly - silicon
  - Aluminum
  - polyimide