INF5490 RF MEMS

LN11: RF MEMS capacitors

Spring 2011, Oddvar Søråsen

Department of Informatics, UoO

Today's lecture

- Passive components in RF circuits
  - Capacitors, C
  - Inductors, L
- Tunable **RF MEMS capacitors**
  - **Vertical** tunable capacitors
  - **Lateral** tunable capacitors
  - **Thermal** tunable MEMS capacitance
  - **Piezoelectric** actuator tunable capacitors
  - Tuning by changing of **dielectric** material
- RF MEMS **capacitance banks**

Passive components in RF circuits

- **→ MEMS capacitors and inductors**
  - Relevant as **replacements** for traditional "off-chip" passive components
  - Tuneability and programability are desired
- **MEMS capacitors**
  - Discrete, tunable capacitances
    - **= varactor** ("variable reactor")
  - Programable capacitance banks with fixed C´s
- **MEMS inductors** (LN12)
  - Discrete, fixed value inductors
  - Programable inductance banks with fixed L´s

Use of tunable capacitors

- VCO = "Voltage controlled oscillator"
  - Value of C determines the frequency
  - C is tuned by voltage
  - VCO has strict requirements on
    - Stability
    - Low phase noise
    - Wide frequency range

- Tunable filters
- Tunable networks for impedance matching
- Phase shifters

MEMS compete with commercial semiconductor technologies

- Discrete Si and GaAs **varactors** exist
  - → 30 GHz
  - Ex. Q = 30-60 for 0.5-5 GHz (SiGe)
  - MEMS varactors not mature enough to replace GaAs varactors, especially for frequencies below 5 GHz

- MEMS varactors have not developed as fast as MEMS switches
  - But: is the RF MEMS component closest to commercial applications
  - Already, many replacements using MEMS have been demonstrated, DC → 100 GHz

Typical characteristics for MEMS varactors

- + Potential for **high Q-values**
  - High Q-value (>100) over a wide frequency band
    - Ex. Q = 100 – 400 for mm-frequencies
- + Simple, compared to alternative technologies
- + Capable of sustaining large RF voltages
- + Low cost fabrication
  - On glass, ceramic, high-resistivity Si-substrate
  - Ex. "low-cost" 3 – 60 GHz tunable networks and filters
- + More reliable
- + Simple and low-cost packaging

Why high Q-values?

- Q-factor characterizes loss due to power dissipation in elements

- Q should be as high as possible to reduce Insertion loss

- Quality factor fundamentals (definition)

$$Q = 2\pi \frac{\text{max imum ins tan t energy stored in circuit}}{\text{energy dissipated per cycle}}$$

Characterize power loss due to dissipation mechanisms in reactive elements.

$$Q_{\text{Tuned Circuit}} = \frac{f_0}{B} \qquad Q_{\text{Capacitor}} = \frac{\omega_0 C}{G} \qquad Q_{\text{Inductor}} = \frac{\omega_0 L}{R}$$

Unloaded : Q (intrinsic)
Loses due to external load : Q_L → Insertion loss at resonance: $IL(dB) = 20 \log (1 + \frac{Q_L}{Q})$

Relation between Q-factor and oscillator stability

- **Q-factor is critical for RF circuit performance!**

Achieving High Oscillator Stability

Frequency-Selective Tank Element

$0^{o}-\Delta\theta$

$0^{o}+\Delta\theta$

v_o

T_o

Low-Q

$Q=10$

(e.g. LC or ring oscillators)

$\Delta f = 400$ kHz

$\Delta\theta = 40^{o}$

High-Q

$Q=1000$

(e.g. crystal oscillators)

$\Delta f = 4$ kHz

$\Delta\theta = 40^{o}$

- High tank $Q \Rightarrow$ high frequency stability

C. T.-C. Nguyen — Univ. of Michigan
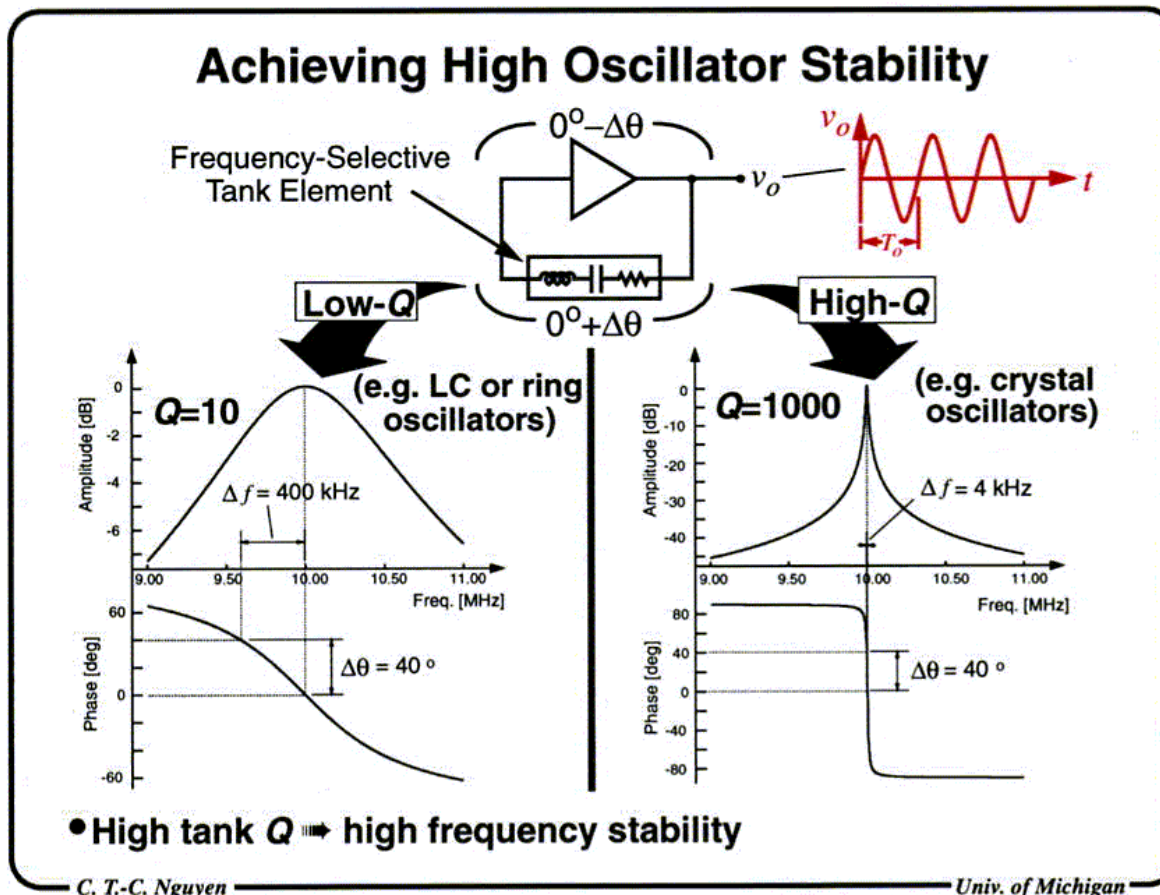
Equivalent circuit for capacitor

- At high frequency → inductance
  - has a characteristic self resonance frequency
  - Inductance should be as low as possible so the self resonance frequency is much higher than the frequency used in normal operation
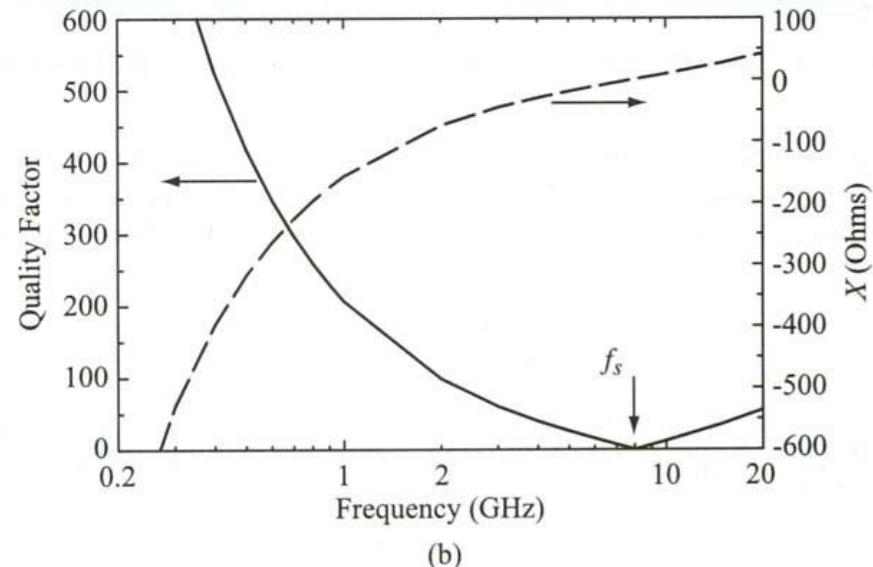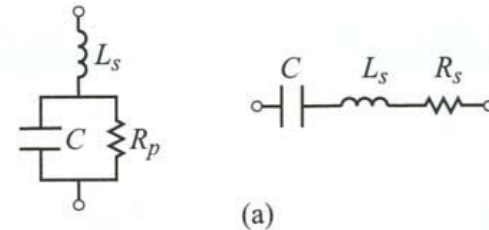
Figure 11.1. (a) Capacitor models. (b) Calculated reactance and Q of a 1-pF capacitor with $L_s = 0.4$ nH and $R_s = 0.83\ \Omega$ ($f_s = 8$ GHz).

Calculations I:

$\underline{SERIE}$ (series) $-||-mm-ww-•$

        C L R
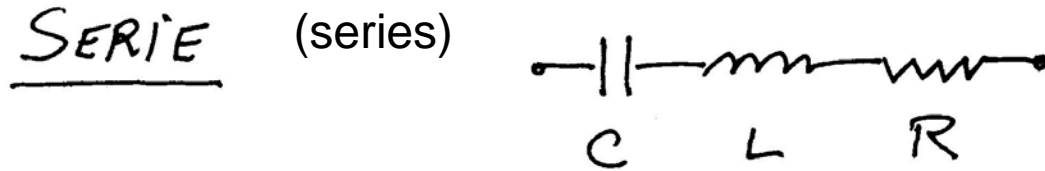
$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right)$$

Selvresonans : $Im(z) = 0$ $\omega_0 = \frac{1}{\sqrt{LC}}$
(Self resonance)

Under selvresonans
Below self resonance) $\omega^2 \ll \frac{1}{LC}$

    $\omega L \ll \frac{1}{\omega C}$

$$Q = \frac{|Im(z)|}{Re(z)} \approx \frac{\frac{1}{\omega C}}{R} = \frac{1}{\omega C R}$$

Calculations II

PARALLELL

(parallel)
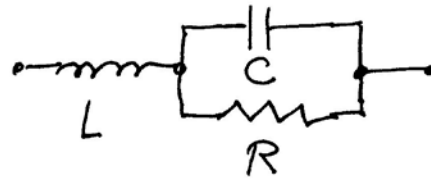
$$Z = sL + (C /\!/ R) = sL + \frac{\frac{1}{sc} \cdot R}{\frac{1}{sc} + R} = sL + \frac{1}{sC + \frac{1}{R}}$$

$$Z = sL + \frac{1}{sc} + t$$

$$t = \frac{1}{sC + \frac{1}{R}} - \frac{1}{sc} = \frac{-\frac{1}{R}}{s^2 C^2 + sC\frac{1}{R}} = \frac{-1}{s^2 C^2 R + sc}$$

$$t = \frac{1}{w^2 C^2 R - jw c} \approx \frac{1}{w^2 C^2 R}$$

$\llcorner$ Dominerende ved lave frekvenser (dominating term at low frequencies)

$$Z = j\left(wL - \frac{1}{wc}\right) + t = j\left(wL - \frac{1}{wc}\right) + \frac{1}{w^2 C^2 R}$$

$$Q = \frac{|Im(z)|}{Re(z)} = \frac{\frac{1}{wc}}{\frac{1}{w^2 C^2 R}} = \frac{w^2 C^2 R}{wc} = \underline{\underline{wCR}}$$

11

Impedance and Q-factor for a discrete capacitor

Q-factor given for ωL<<1/ωC

$$Z = R_s + j\left(\omega L_s - \frac{1}{\omega C}\right) \qquad \text{for a series model}$$

$$\simeq \frac{1}{\omega^2 C^2 R_p} + j\left(\omega L_s - \frac{1}{\omega C}\right) \qquad \text{for a parallel model} \qquad (11.2)$$

The capacitor quality factor, Q, is derived to be

$$Q = \frac{|\text{Im}(Z)|}{\text{Re}(Z)} = \frac{1}{\omega C R_s} \qquad \text{for a series model}$$

$$= \omega C R_p \qquad \text{for a parallel model} \qquad (11.3)$$

[Rebeiz]

Challenges for RF MEMS capacitors

- → Obtain required **Tuning Ratio (TR)**
  - Definition TR: $C_{\max}/C_{\min}$
  - Should be > 2

- ÷ Tuning ratio is generally low
  - TR = 1.2 − 2.5
  - For semiconductor varactors: TR = 4 − 6

- ÷ MEMS is sensitive to various noise effects
  - C value can change due to low spring constant, k
  - Low k is desired for 3 − 5 V applications
  - A low k-value is a challenge due to
    - Acceleration, RF power self actuation, noise effects

Parallel plate capacitor

- Basic equations
  - $Q = V\,C$, $I = C\,dV/dt$
  - $C = \varepsilon\,A\,/\,g$

- NB! C generally tuned by 3 parameters
  - g, gap
  - A, area
  - ε, dielectric constant

Tunable RF MEMS capacitors

- Electrostatic actuation is a dominating mechanism for tuning
  - Low power consumption, simple
- **Vertical** electrostatic displacement
  - Tuning the gap (**non-linear** change) in parallel plate capacitor
    - 2-plate capacitance
    - 3-plate capacitance
    - Double air-gap capacitance
    - Other examples
- **Horizontal** (lateral) displacement
  - Tuning of area (**linear** change)
- **Thermally** tunable MEMS capacitance
- **Piezoelectric** actuator tunable capacitance
- Tuning by change of **dielectric** material between plates

Two-plate tunable MEMS capacitance

- **Young & Boser, Berkeley**
- Gap-tuning
- One plate can move by electrostatic actuation
- Equilibrium between elastic and electrical forces

C

Al (1-2μm)

Few μm air gap

Al ground plane

Si substrate
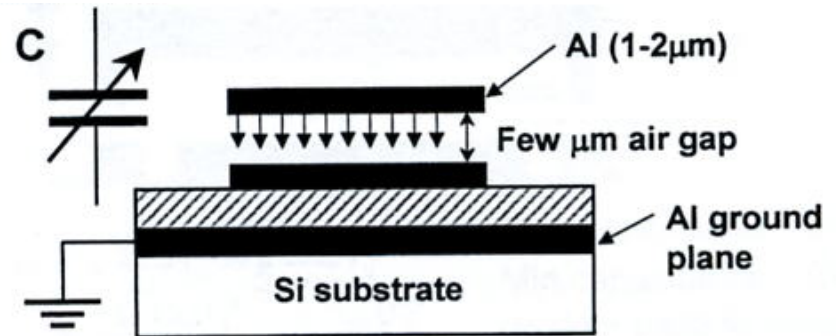
Calculation of TR for 2-plate capacitance
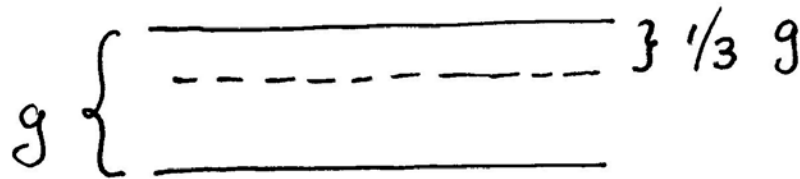
$$C_{min} = \varepsilon \frac{A}{g} \qquad\qquad C_{max} = \varepsilon \frac{A}{\frac{2}{3}g} = 1.5\, C_{min}$$

$$C_{max} = 150\% \cdot C_{min} \qquad \Rightarrow \qquad TR = 150\%$$

Theoretical TR = 150%. Limited by the pull-in effect

Young & Bover, Berkeley

- Etching a hole in capacitance plate
  - For decreased squeezed-film damping
  - Positive for "release"-step in the process

- **Theoretical tuning range:** 50% (limited by pull-in effect)
- **Practical tuning range (demonstrated):**
  TR=16%, C_{max}=2.46pF, C_{min}=2.11pF, V_A=5V
- **RF performance:** Q=62 @ 1GHz

200 µm
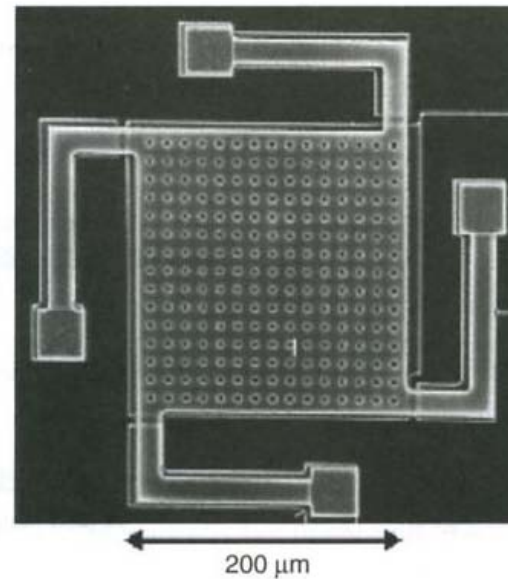
Figure 4.33 Top view of a micromachined variable capacitor. Reproduced from D.J. Young and B.E. Bover, 1996, 'A micromachined variable capacitor for monolithic low-noise VCOs', in *Proceedings of the International Conference on Solid-state sensors and Actuators*, IEEE, Washington, DC: 86–89, by permission of IEEE, © 1996 IEEE

Varadan

Implementation

- Typical features for a Berkeley implementation →

- Surface micromachining
  - 2 metal layers + Al gnd-plane
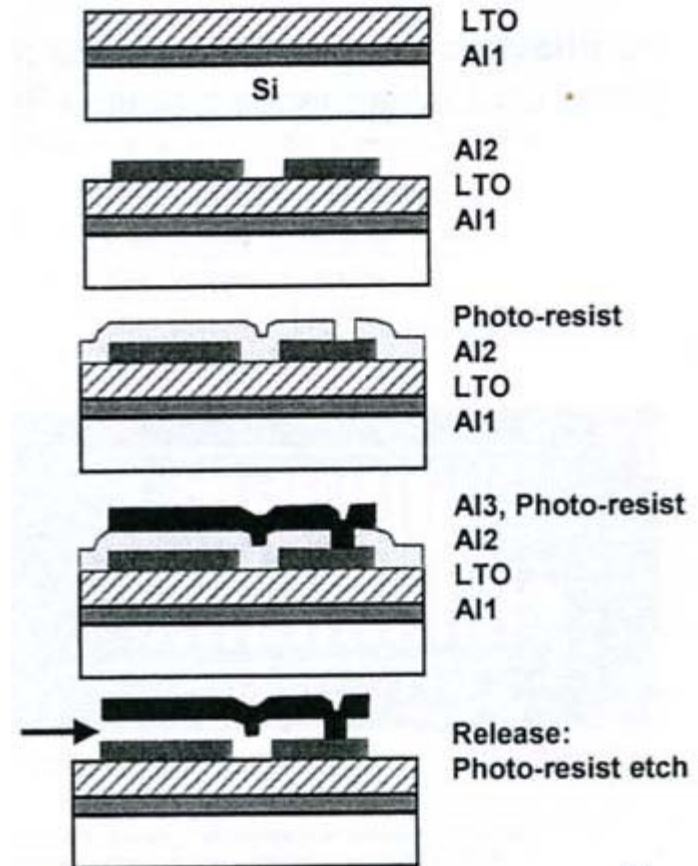
LTO = Low temperature oxide

LTO
Al1
Si

Al2
LTO
Al1

Photo-resist
Al2
LTO
Al1

Al3, Photo-resist
Al2
LTO
Al1

Release:
Photo-resist etch

3-plate tunable MEMS capacitance

- TR can be increased by introducing a 3rd plate
  - A. Dec & K. Suyama: "Micromachined Electro-Mechanically Tunable Capacitors and Their Applications to RF IC´s" 1998. **Columbia University**
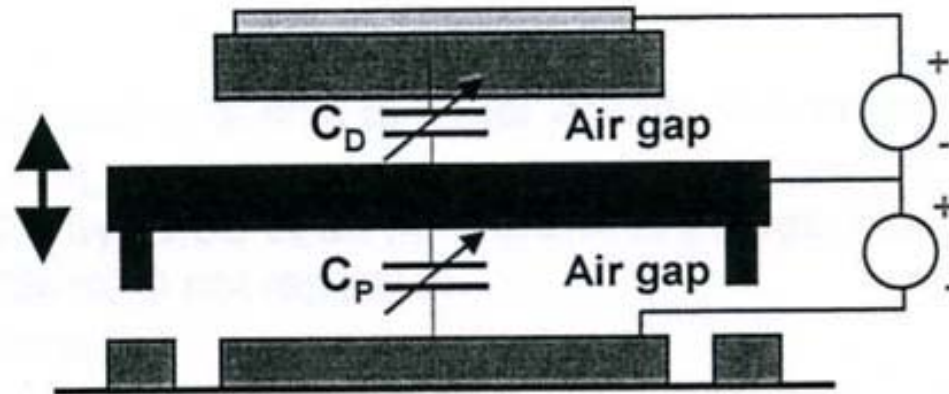
Calculating TR for 3-plate

$\frac{1}{3}g$

$\frac{1}{3}g$

C_{max}

C_{min}

C_D
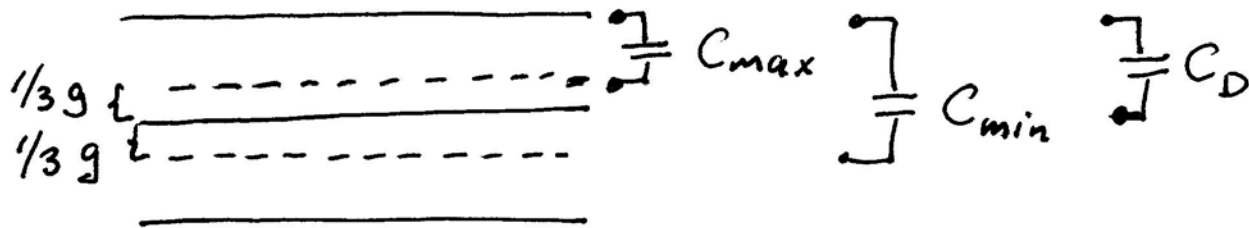
$$C_{max} = \frac{3}{2} C_D \qquad C_{min} = \varepsilon \frac{A}{\frac{4}{3}g} = \frac{3}{4} C_D$$

$$TR = \frac{C_{max}}{C_{min}} = \frac{\frac{3}{2} C_D}{\frac{3}{4} C_D} = 2 = 200\%$$

TR = 200%, e.g.: can be tuned 100%
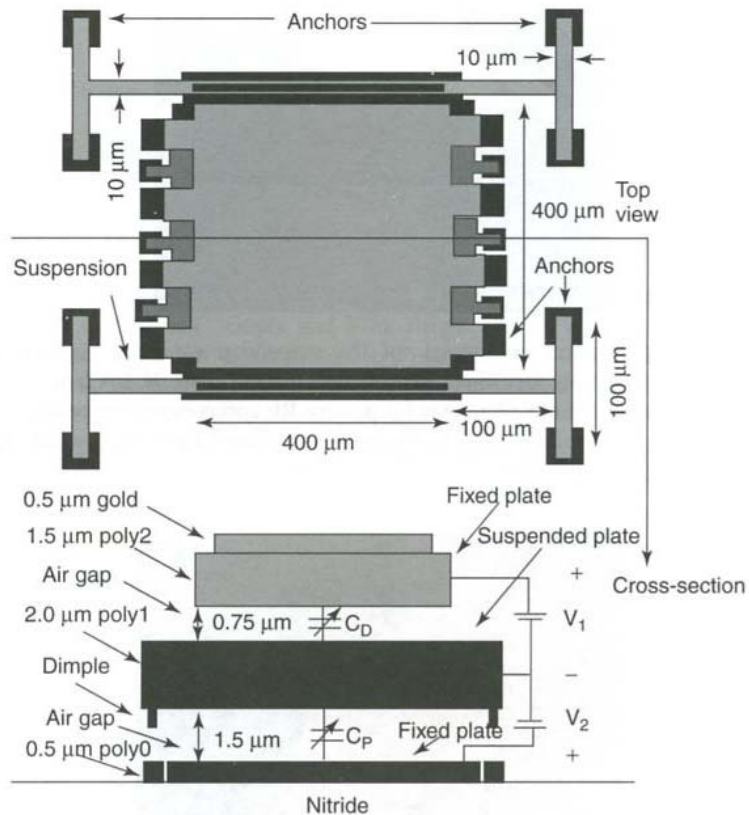
Figure 4.35 Top and cross-sectional views of three-plate varactor. Reproduced from A. Dec and K. Suyama, 1998b, 'Micromachined electromechanically tunable capacitors and their applications to RF IC's', *IEEE Transactions on Microwave Theory and Techniques* **46**(12): 2587–2596, by permission of IEEE, © 1998 IEEE

**Demonstrated values,
Dec & Suyama:**

- **Theoretical tuning range: 100%**
- **Practical tuning range:**
  TR=87%, C_{min}=3.4pF, C_{max}=6.4pF, V~4V
- **RF performance: Q = 15.4 @ 1GHz, 7.1 @ 2GHz**

(a)

Suspended plate   Fixed plate

$0.75\ \mu m \neq C_D$

V_1

$1.5\ \mu m \neq C_P$

V_2

Dimple   Fixed plate

- Gold 0.5 μm
- Poly 2 1.5 μm
- Poly 1: 2.0 μm
- Poly 0: 0.5 μm
- Anchor

(b)

$V_1 = 0\ V$
$V_2 = V_B$

$V_1 = V_B$
$V_2 = 0\ V$

V_B [V]

(c)
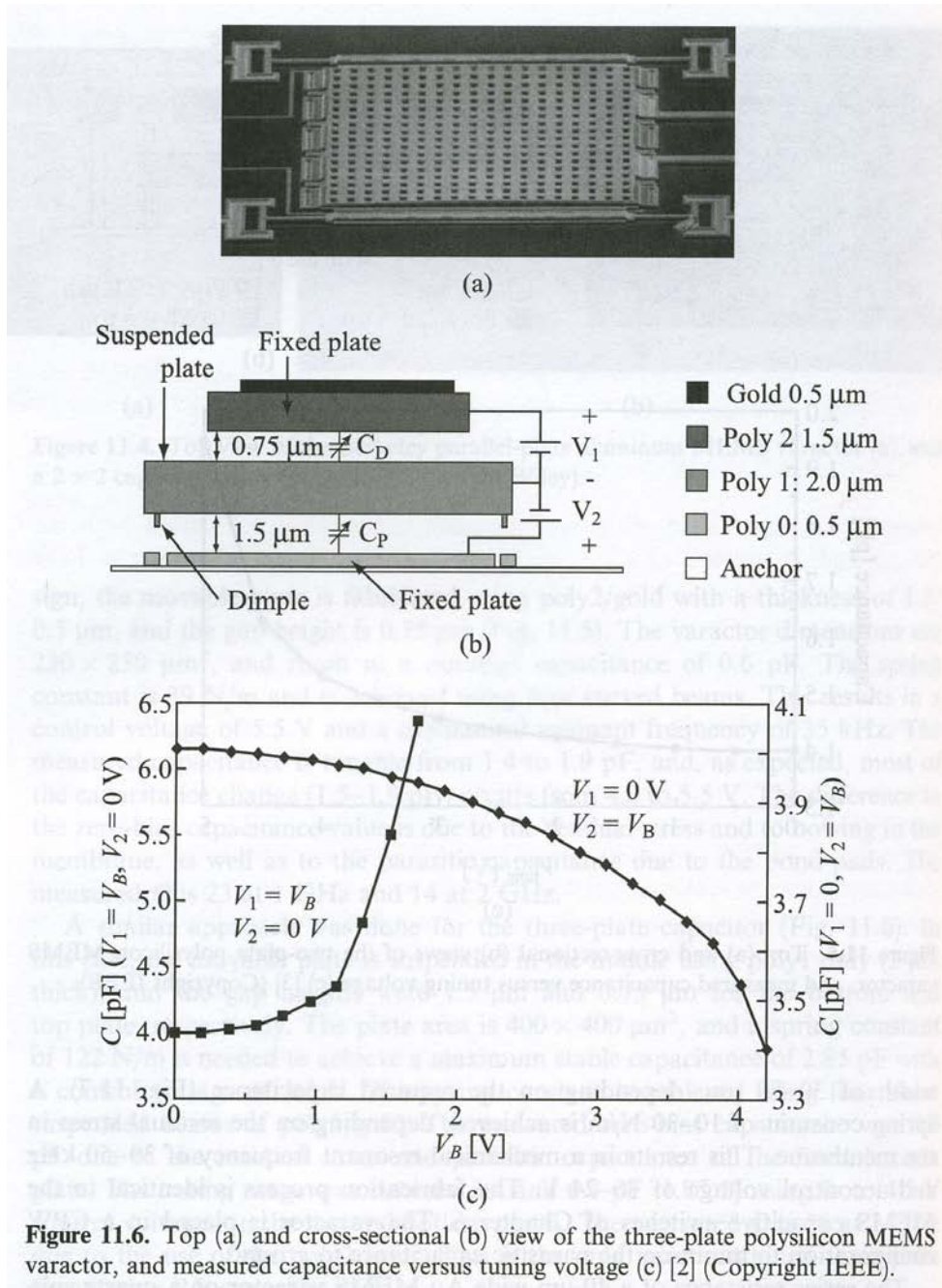
C is between upper plates

Rebeiz:
Dec & Suyama

Figure 11.6. Top (a) and cross-sectional (b) view of the three-plate polysilicon MEMS varactor, and measured capacitance versus tuning voltage (c) [2] (Copyright IEEE).

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Dec & Suyama, contd.

- Process
  - Standard 3-layer poly surface micromachining (MUMP´s) with HF etching and "supercritical drying"
  - **Poly** often used as parallel plate due to superior mechanical properties instead of Al (in spite of Al having better conductivity)

TABLE I

SUMMARY OF SELECTED MUMP'S PROCESS PARAMETERS

Layer	Thickness	Sheet Resistance
Poly0	0.5 μm	30 Ω/sq
Poly1	2.0 μm	10 Ω/sq
Poly2	1.5 μm	20 Ω/sq
Gold	0.5 μm	0.06 Ω/sq

Dec & Suyama, ex.2
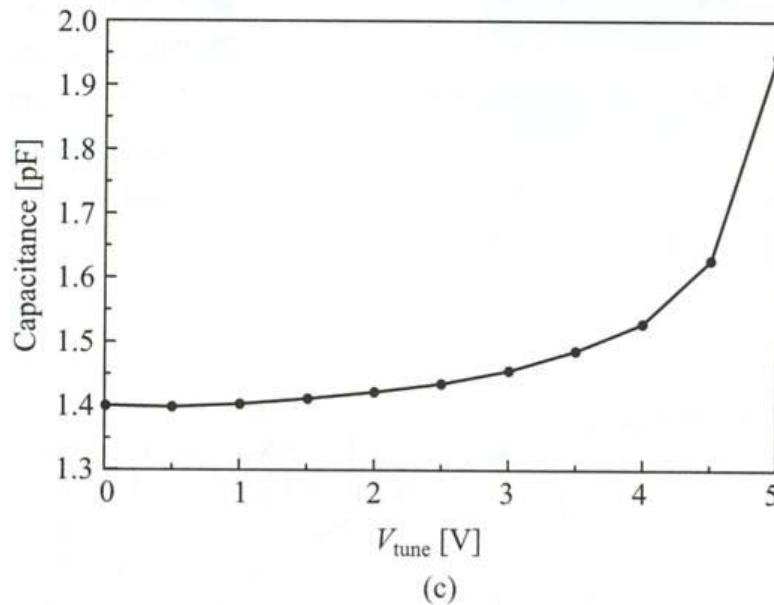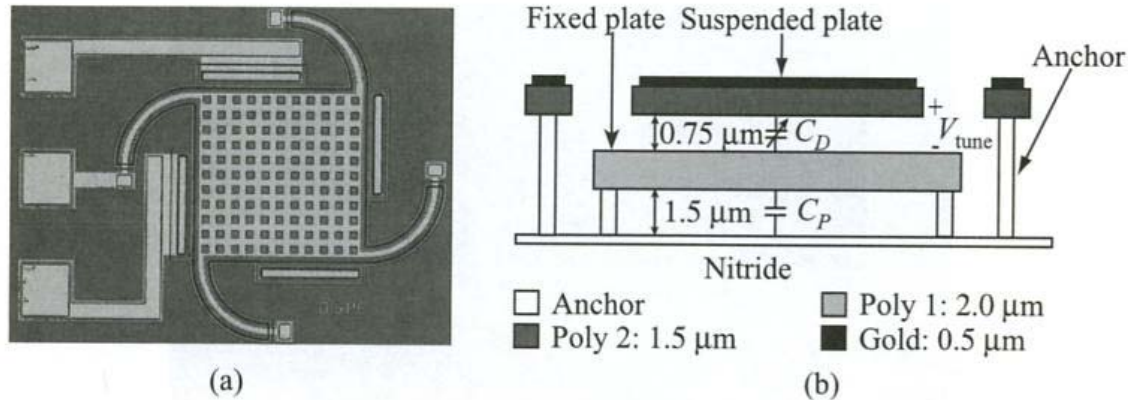
Figure 11.5. Top (a) and cross-sectional (b) views of the two-plate polysilicon MEMS varactor, and measured capacitance versus tuning voltage (c) [3] (Copyright IEEE).

Rebeiz

Double air-gap capacitance

- **J. Zou et al, 2000, Univ of Illinois**
- Why double air-gap?
  - Increase TR
    - Eliminate pull-in effect
  - May deflect down to 1/3 d_2 before pull-in
  - TR may increase significantly if $1/3 * d_2 > d_1$
    - Eg. **centre electrode can be fully deflected without pull-in!**
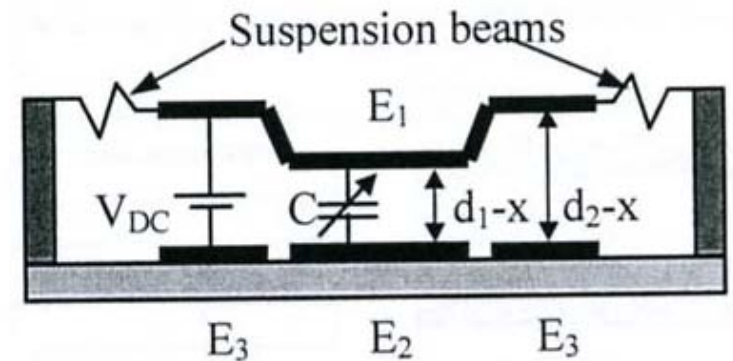
Univ of Illinois, contd.
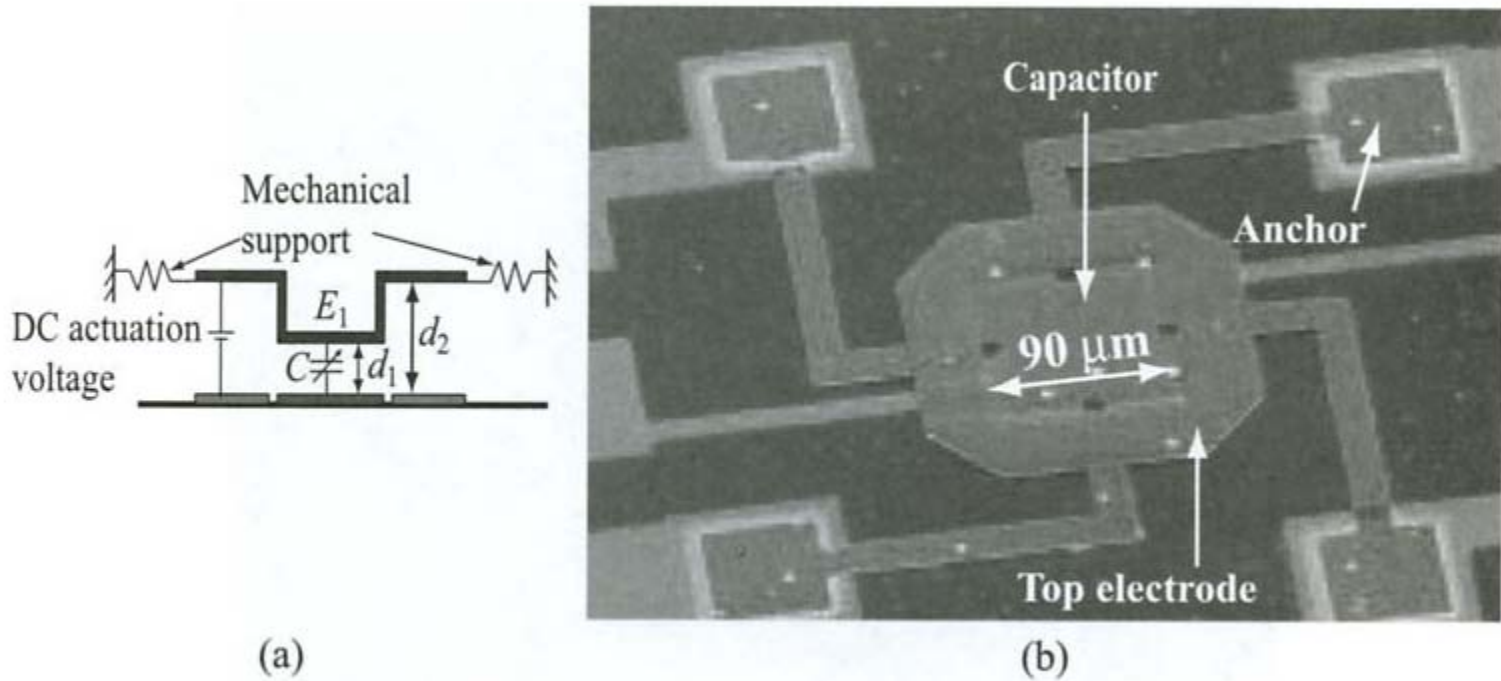
Figure 11.12. Cross-sectional (a) and top (b) view of the University of Illinois wide-tuning-range varactor [11] (Copyright Wiley).

Univ of Illinois, contd.

Simplified fabrication process
- Cu as sacrificial layer
- Metals: gold & permaloy (Ni-Fe)
- Air-gap: d_1 = 2 μm, d_3 = 3 μm

(a) 0.5-μm gold and 1-μm copper evaporation

(b) Copper patterning

(c) 2-μm copper evaporation

(d) 2-μm Ni–Fe electroplating, copper sacrificial layer etching, and device releasing
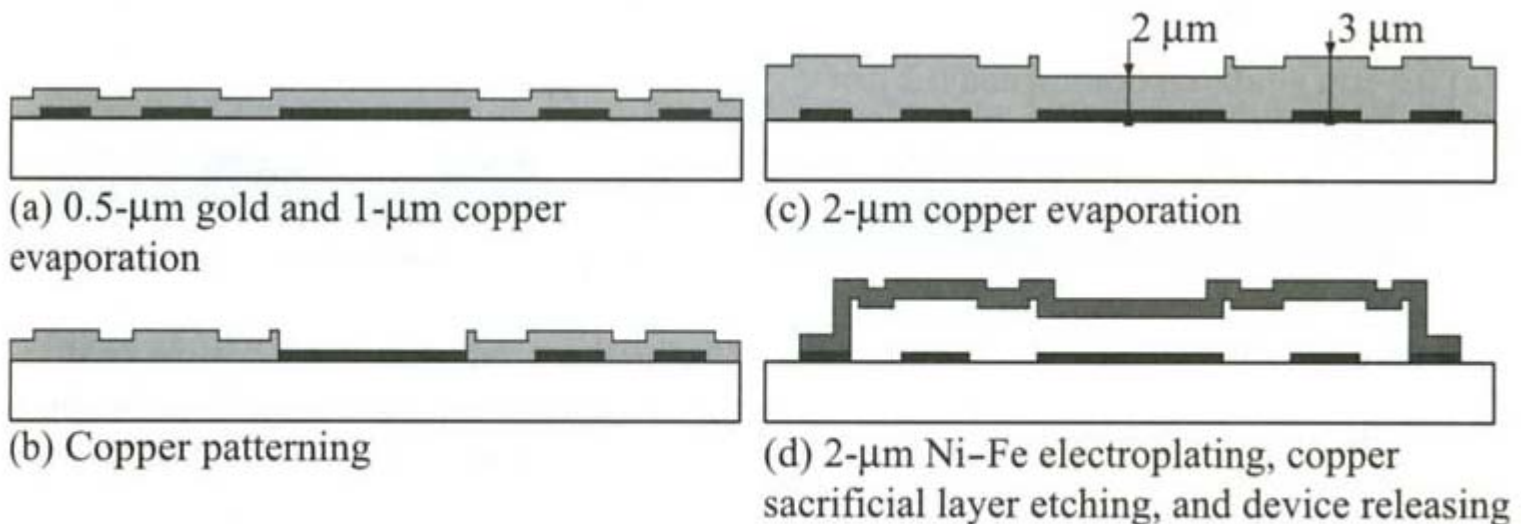
Figure 11.13. Fabrication process of the University of Illinois wide-tuning-range varactor [11] (Copyright Wiley).

Ex. from Univ of Michigan
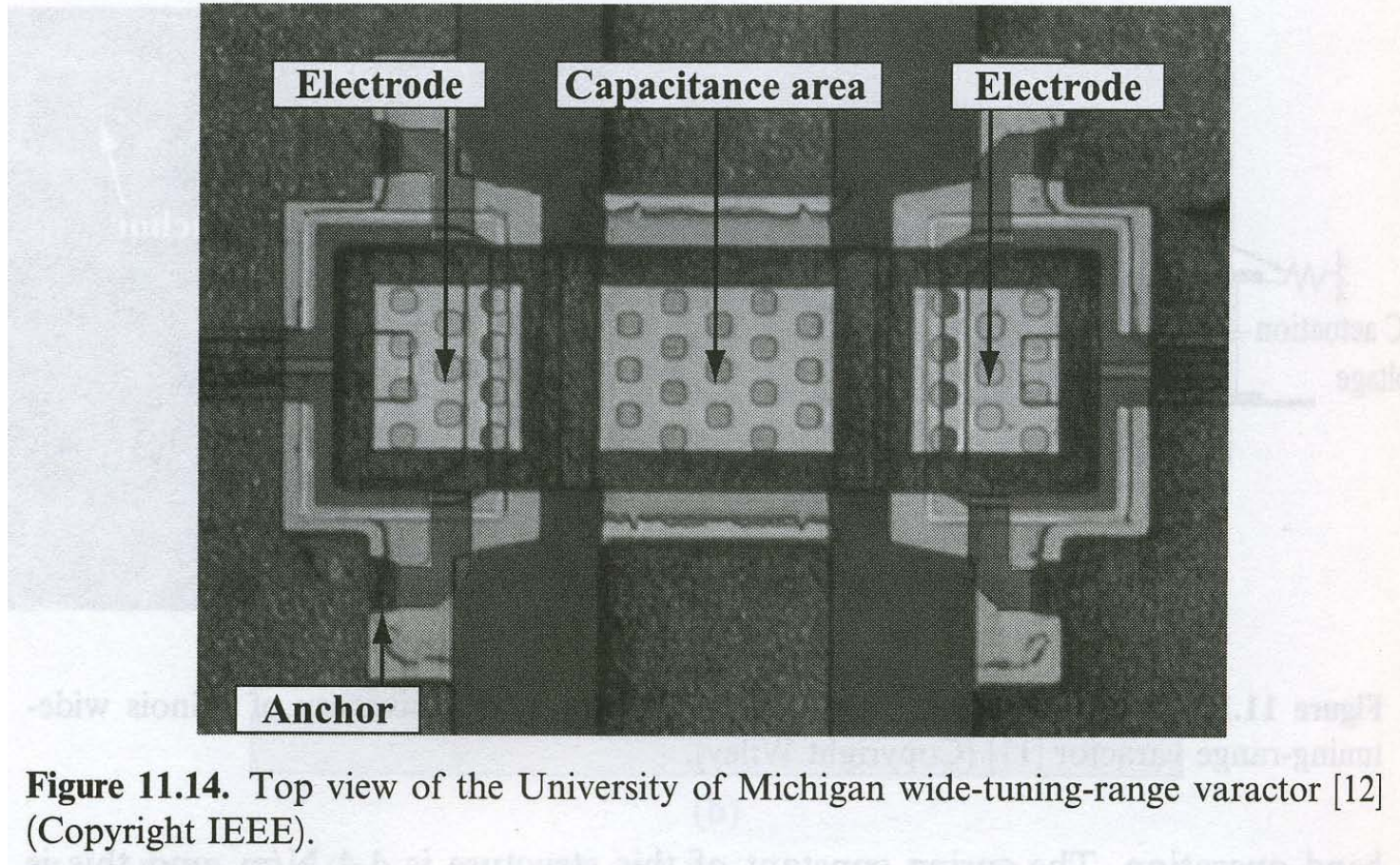
Figure 11.14. Top view of the University of Michigan wide-tuning-range varactor [12] (Copyright IEEE).

Ex. from Univ of Michigan, contd.

- Implemented on quartz substrate
- SiO2 sacrificial layer partly etched → 2-steps Au membrane
- Q = 120 @ 34 GHz
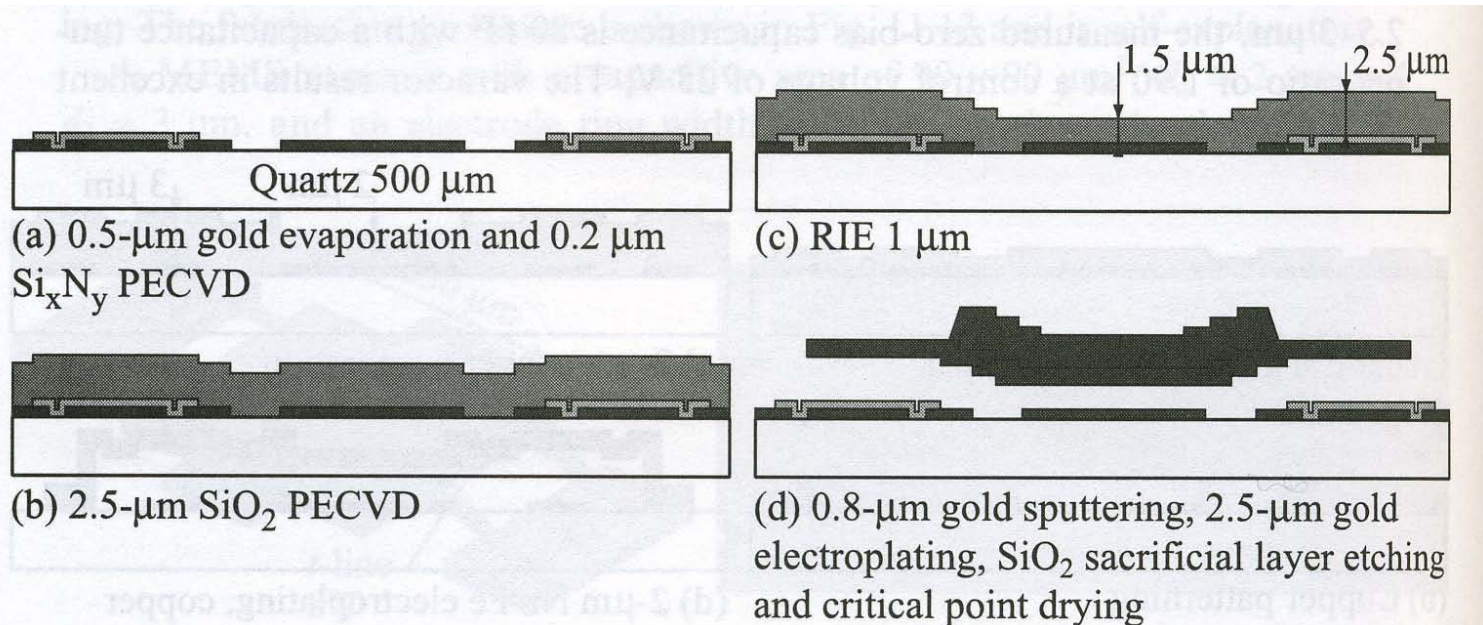
Figure 11.15. Fabrication process of the University of Michigan wide-tuning-range varactor [12] (Copyright IEEE).

Univ of Michigan, discrete 2-valued
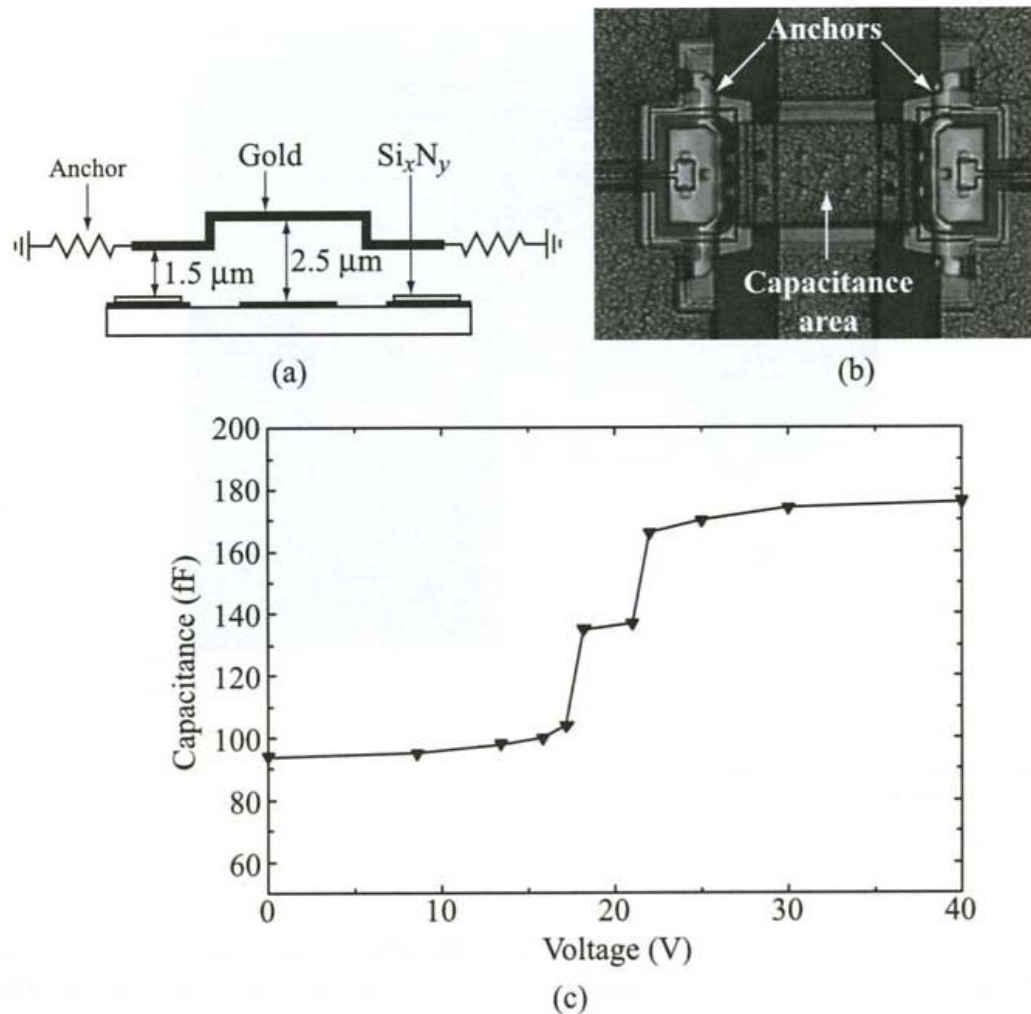
Figure 11.29. Cross section (a), top view (b), and measured capacitance (c) of the Michigan discrete two-value MEMS varactor [12] (Copyright IEEE).

Multi-state MEMS capacitors with multi-airgap

- capacitive-switch like design: t_{up} and t_{down} depend on k & voltage
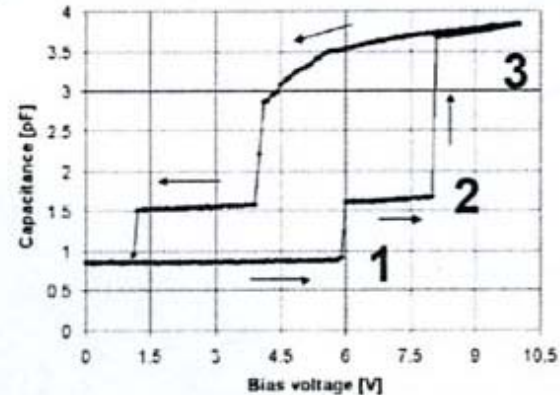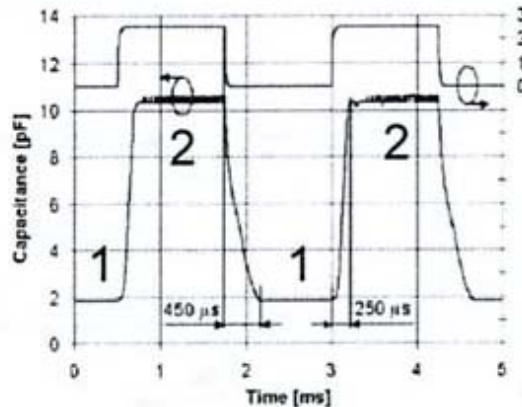
2-state MEMS capacitor
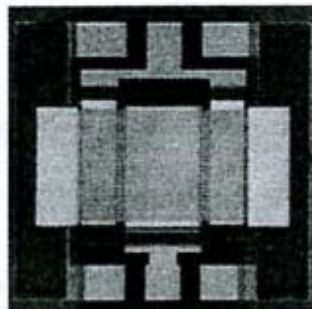
3-state MEMS capacitor

73
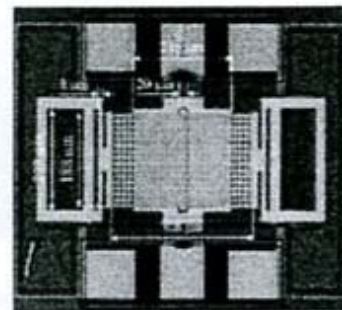
H Nieminen, V Ermolov, K Nybergh, S Silanto and T Ryhanen, J. Micromech. Microeng. 12 (2002) pp. 1–10.

Different segments with multi-gap. May be tuned to 2 or 3 levels. Hystereses properties

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Ionescu, EPFL: H. Nieminen et al (Nokia)

Working principle:

C_0

C_1

C_2

33
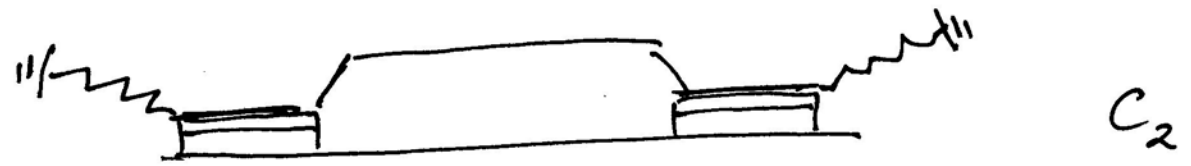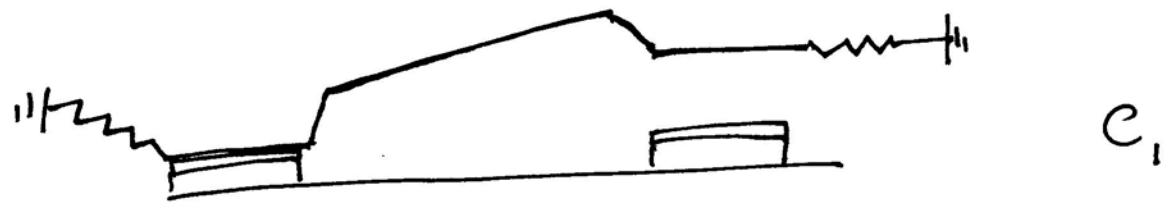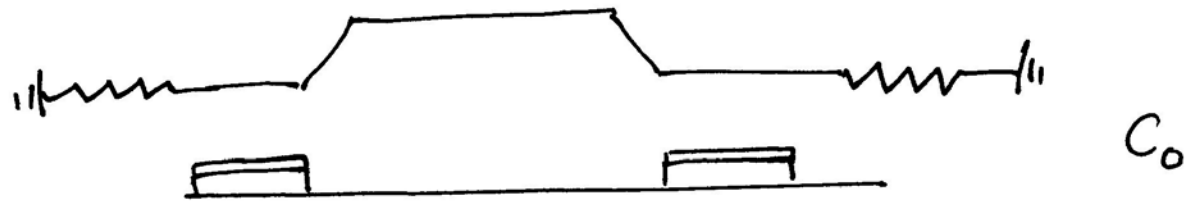
"Zipper" capacitor

- Ex. zipper cantilever capacitor

- Design and fabrication at Columbia University

  – Long, thin beam deflected gradually from one edge
  – Small capacitances added in parallel

Zipper-action catilever
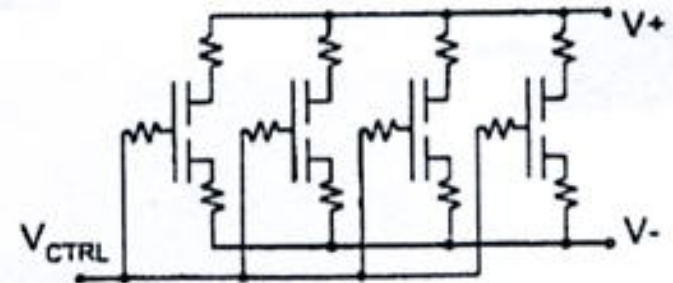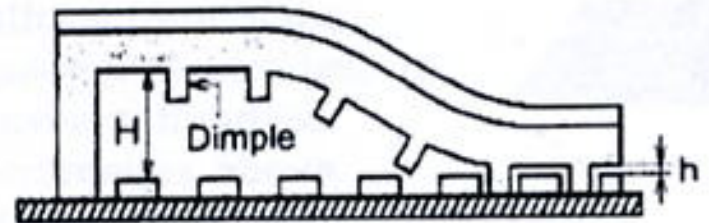
Performance:
- **TR: 46%** with voltage~35V
- **Q=6.5 @1.5GHz**
- a CMOS VCO with this capacitor exhibited TR of 4.8% with center frequency of 1.5GHz and phase noise of −131dBc/Hz @ 600kHZ offset

Ex. from MIT
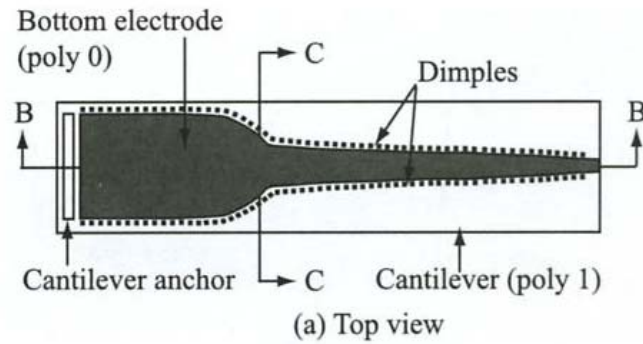
Softest at the tip
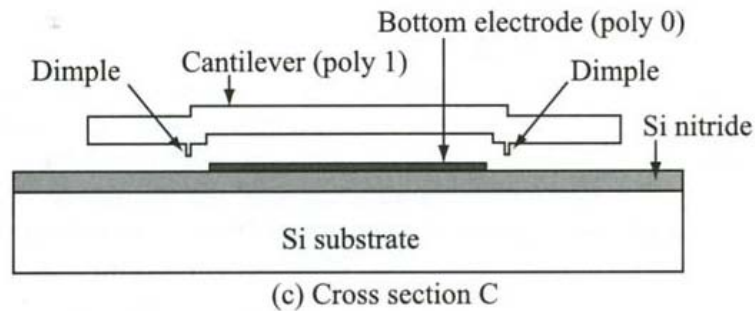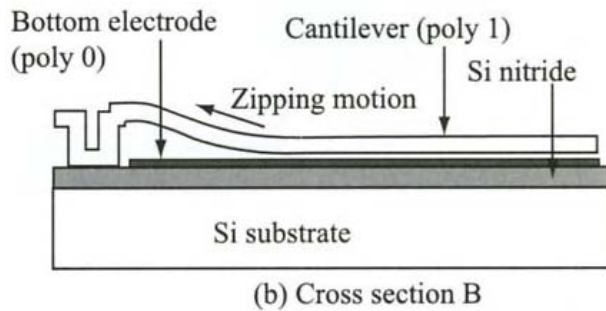
Figure 11.9. Top (a) and cross-sectional (b,c) view of the MIT zipper varactor [8].

Rebeiz

Univ of Colorado, Boulder

- Digitally controlled individual capacitances
- Has individual plates that may be actuated sequentially
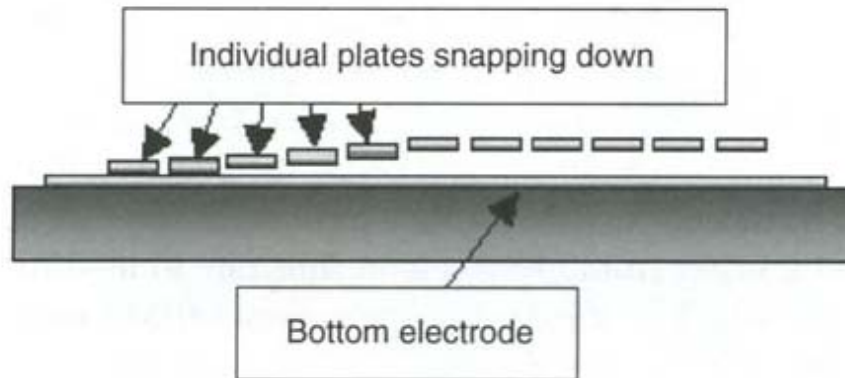
Figure 4.38 Schematic diagram of the capacitor plate arrangement. Reproduced from N, Hoivik, M.A. Michalicek, Y.C. Lee, K.C. Gupta and V.M. Bright, 2001, 'Digitally controllable variable high-Q MEMS capacitor for RF applications', in *Proceedings of IEEE MTT-S Symposium, May 2001, Volume 3*, IEEE, Washington, DC: 2115–2118, by permission of IEEE, © 2001 IEEE

Varadan

Univ of Colorado, Boulder

Gold   RF capacitors   Polysilicon

Carrier substrate

Dielectric layer   Single bond pad

(a)

(b)
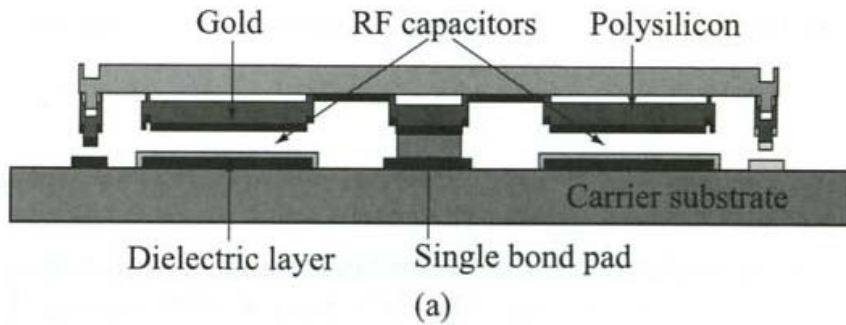
Each "plate" coupled with **different width** of beam, eg. different spring constant (= softness) for each part
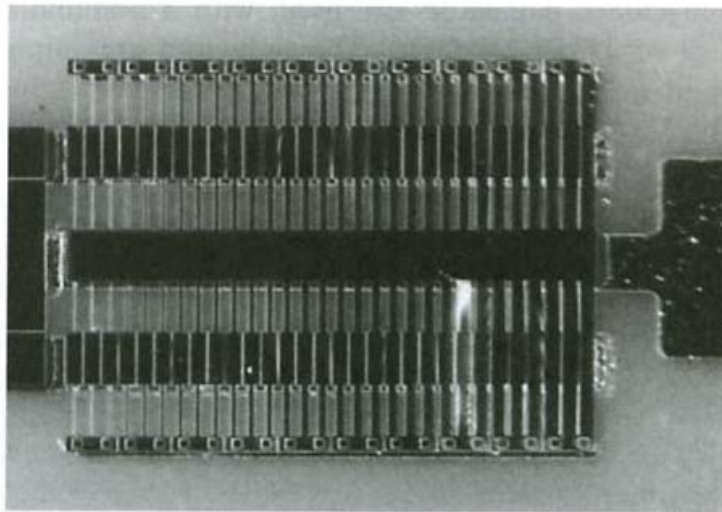
Standard MUMP´s process (poly-Si and gold), alumina-substrate

Electrostatic actuation V= 30 V
TR = 4 : 1
Q = 140 @ 750 MHz

Figure 11.30. Cross section (a) and top view (b) of the Colorado RF MEMS varactor. The variable capacitors are the dark rectangles on both sides of the center conductor [23] (Copyright IEEE).

Elevated platform capacitance

- L. Fan et al, 1998
  - One of the electrodes may be elevated to several hundred micrometers above the substrate
    - 250 µm elevation, TR 2400%
    - ÷ Fine tuning difficult

- Uses actuators pushing the structure together
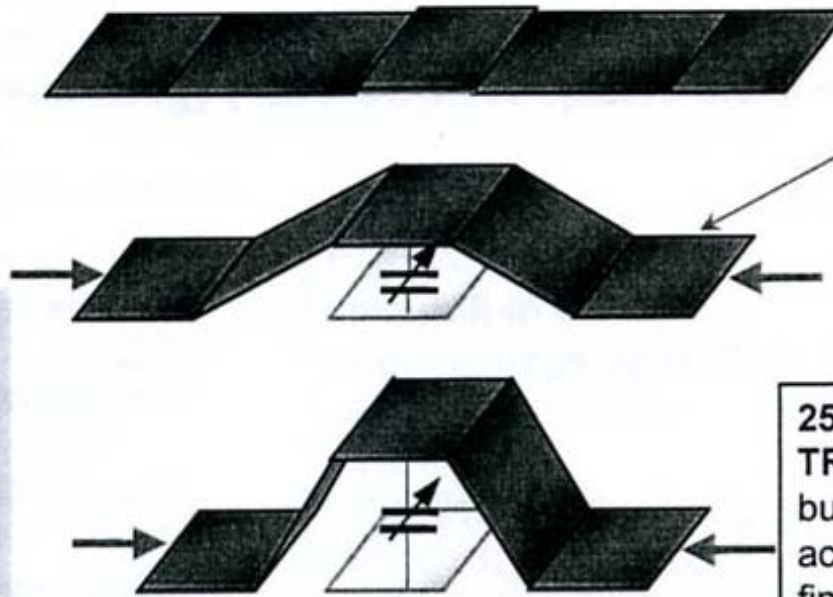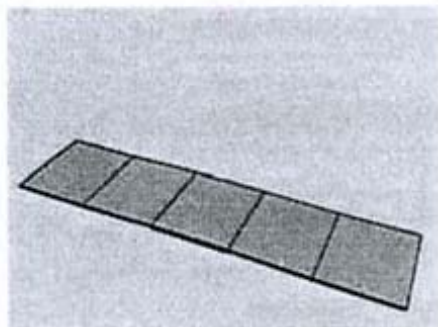 - "Scratch drive actuator"
  - Must implement hinges

SCRATCH DRIVE ACTUATOR
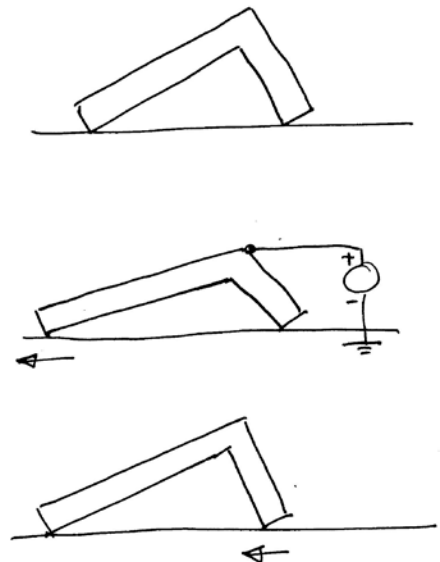
Elevated platform MEMS capacitor

Idea: raise a conductive platform (one of the capacitor electrodes) up to several hundred micrometers above substrate (silicon) surface

Scratch drive actuator (SDA) arrays

250µm elevation (!!)
TR: 2400%
but very difficult to achieve
fine tuning

L. Fan, R. T. Chen, A. Nespola, 11th Annual International Workshop on Micro Electro Mechanical Systems (MEMS '98), 1998.

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Ionescu, EPFL

Self actuation

- Design parallel plate capacitances to handle RF power
  - AC applied over the RF MEMS capacitance
    - RF frequency does not modulate C-value
  - BUT, RMS-value of RF-signal will influence C and could induce pull-in by self actuation

- Capacitances for gap-tuning has limited RF power handling capability due to small electrode gap
  - Decrease distance → RF breakdown can occur

Lateral tunable capacitors

- Horizontal displacement
  - – C can be tuned by changing the **area**, $C = \varepsilon A / g$
  - – + No theoretical limit for TR
  - – + Pull-in effect avoided
  - – ÷ Photolithography determines precision of dimensions
  - – ÷ More complicated suspension structures?
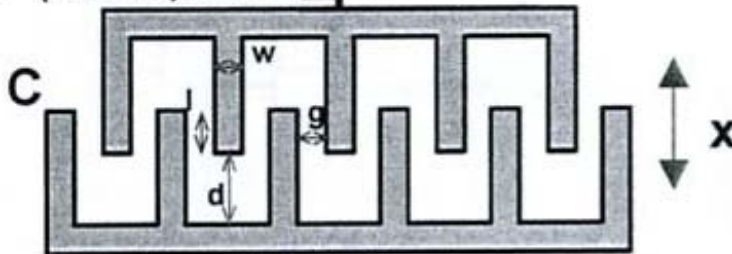   - Make sure that the movable structure is suspended!

- Comb structure is common

Comb-like (inter-digital) tunable MEMS capacitors

Deflection:
$$x = V^2 (dC/dx) / 2k$$

Idea: **area-tuning capacitor**
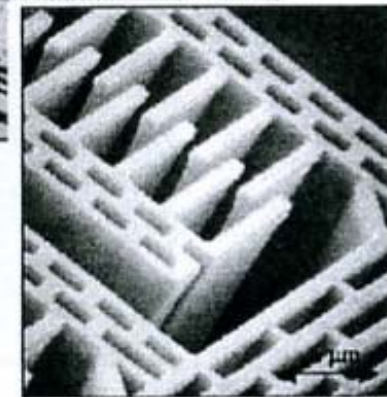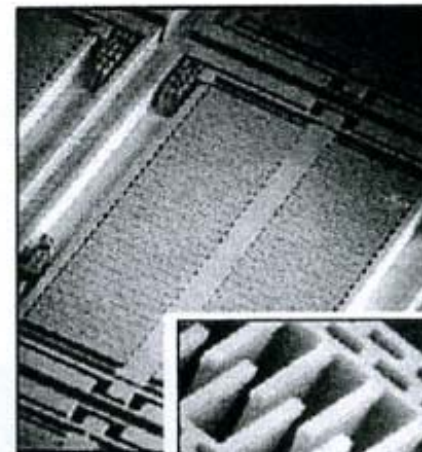
Design and fabrication
(Rockwell Science Center):
- Comb-like structure using single mask process
- Deep anisotropic silicon etching technique in ICP (inductively coupled plasma) reactor
- **Very flexible design**: **large range of C and TR**

Figures of merit:
- **TR= 200% C_{max}=3.2pF, C_{min}=6.44pF, V=5V**
- **Recent results show: Q > 40-160 @ 400-1600MHz**

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J.J. Yao, S. Park and J. DeNatale, Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 1998, pp. 124-127.

Ionescu, EPFL: J. J. Yao et al, Rockwell

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Simple comb structure

- Ex. from Rockwell Science Center →

    - Inter-digital tunable MEMS capacitance

    - One set of combs is stationary, the other set can be moved

    - Gap is not changing

    - Length of comb and finger length limit tuning range

    - Can be tuned by an electrostatic micro motor or by applying different actuation voltages

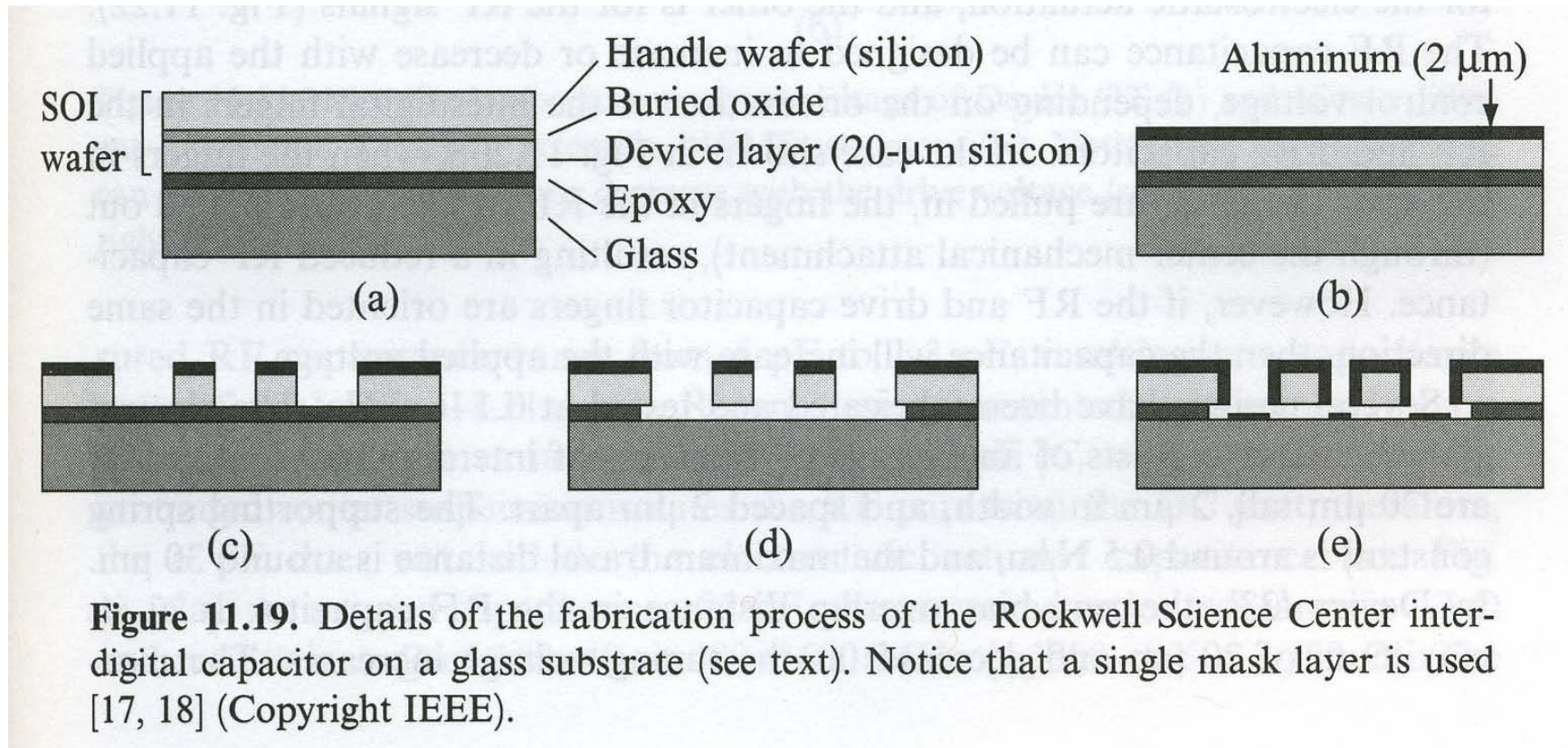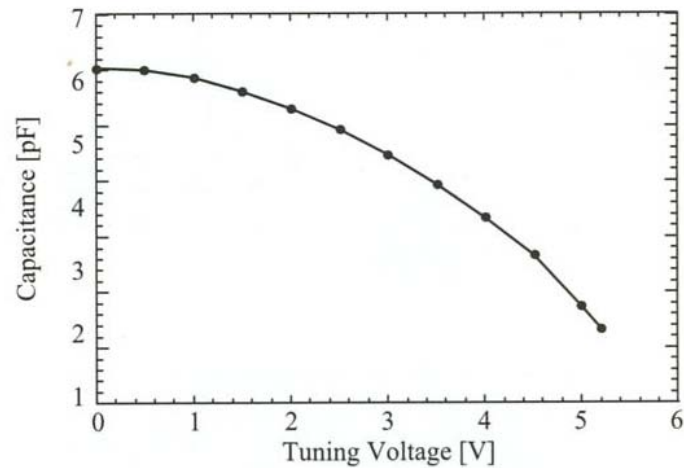# Rockwell Science Center, forts.

Ex. of tuning

VS = RF

HS = tuning
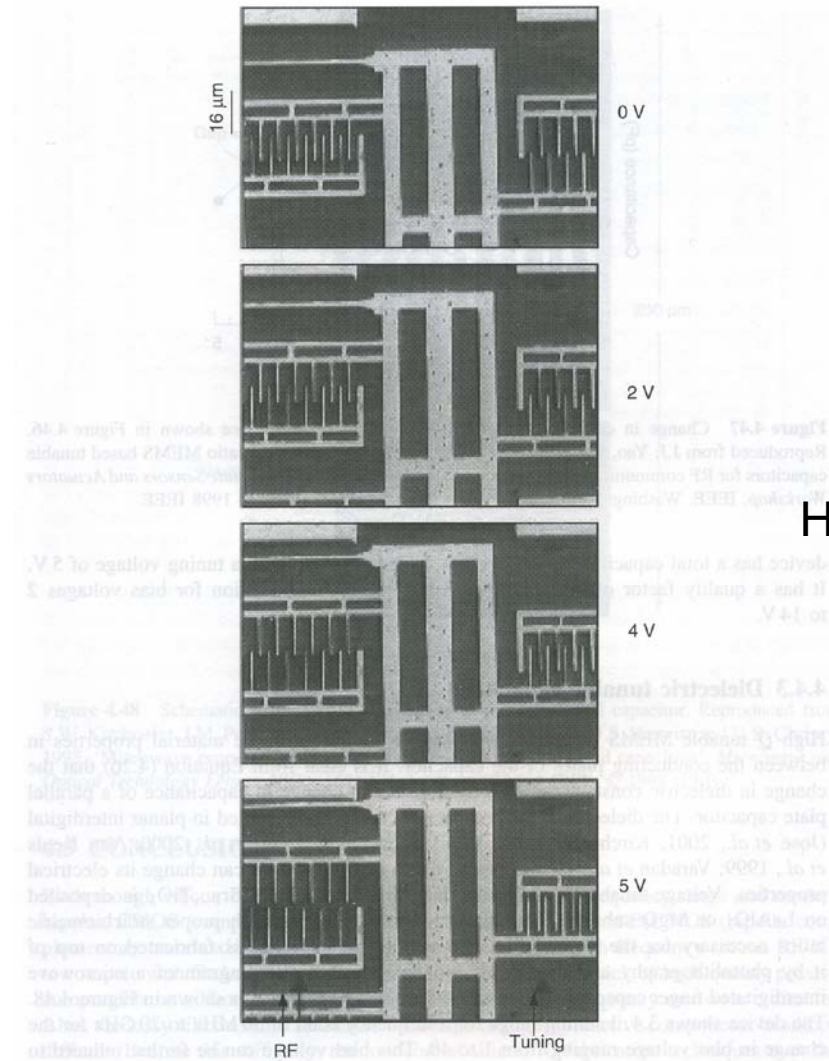
Figure 4.46 Series of images showing a MEMS tunable capacitor with a tuning voltage of 0 to 5-V. Reproduced from J.J. Yao, S. Park and J. DeNatale, 1998, 'High tuning ratio MEMS based tunable capacitors for RF communications applications' in *Proceedings of solid-state sensors and Actuators Workshop*, IEEE, Washington, DC: 124–127, by permission of IEEE, © 1998 IEEE
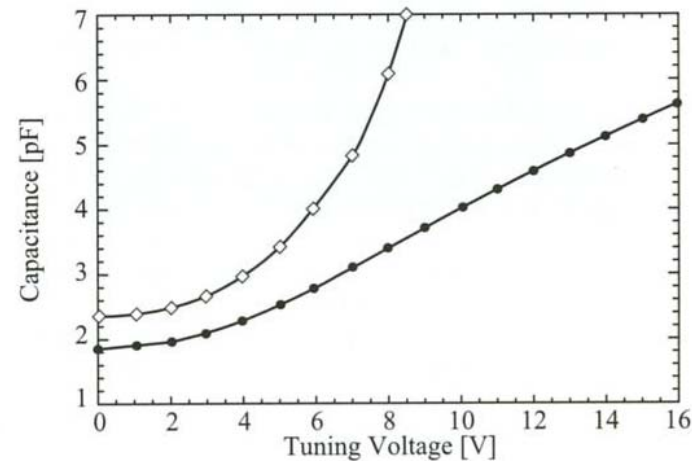
Varadan

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Rockwell Science Center, contd.

Figure 11.19. Details of the fabrication process of the Rockwell Science Center interdigital capacitor on a glass substrate (see text). Notice that a single mask layer is used [17, 18] (Copyright IEEE).

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Rockwell Science Center, contd.

Figure 11.21. Measured capacitance versus voltage of Device '33' (a) and of two different interdigital Rockwell Scientific MEMS varactors (b). Notice that the capacitance can be designed to increase or decrease with the drive voltage (see text) [17, 18] (Copyright IEEE).

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Thermal tunable parallel-plate MEMS capacitance

- Use hot and cold arms
  - A high resistivity arm will be hotter and deform more
    - Differential thermal expansion

- Challenges with this technology
  - **Power dissipation**
  - **Low speed**
  - But removes the pull-in limitation!
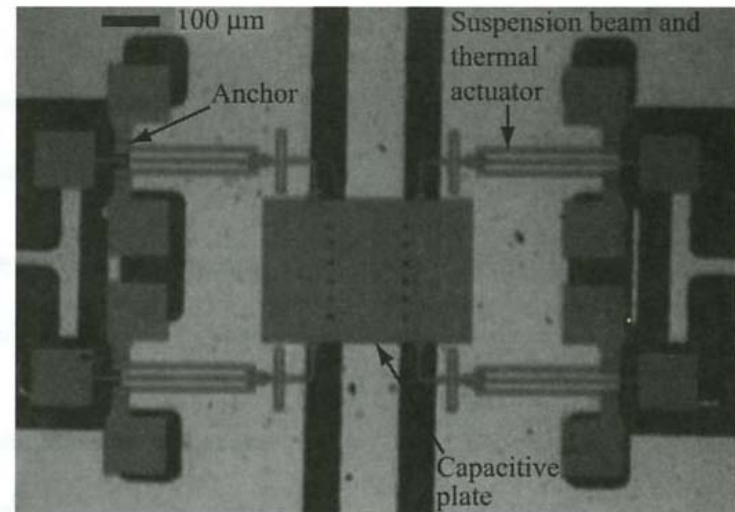
Figure 11.16. Top view of the University of Colorado thermally actuated MEMS varactor in a CPW circuit [13] (Copyright IEEE).
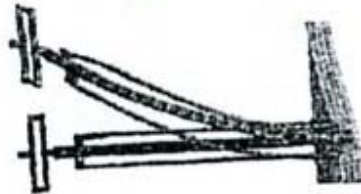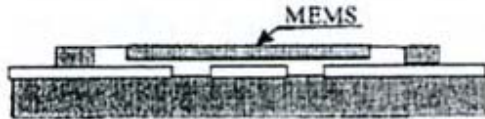
Univ of Colorado
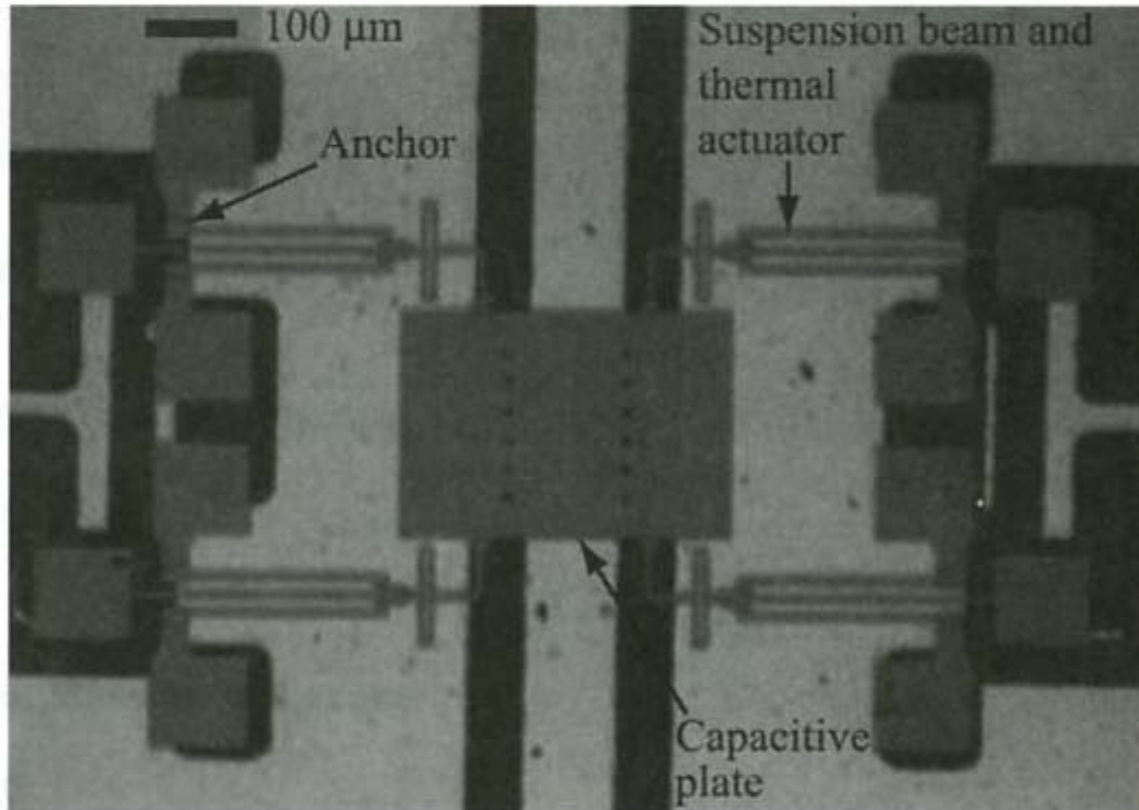
Figure 11.16. Top view of the University of Colorado thermally actuated MEMS varactor in a CPW circuit [13] (Copyright IEEE).

Z. Feng et al, Univ of Colorado: **Design and Modeling of RF MEMS Tunable Capacitors Using Electro-thermal Actuators**
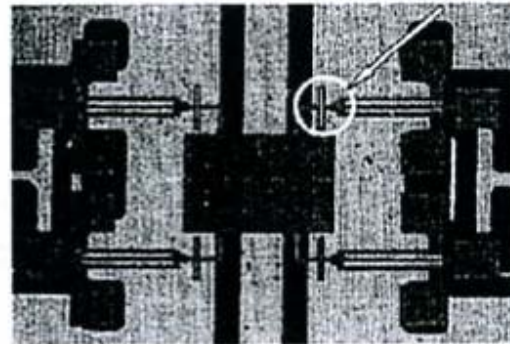
Rebeiz

Thermally tunable parallel-plate MEMS capacitor
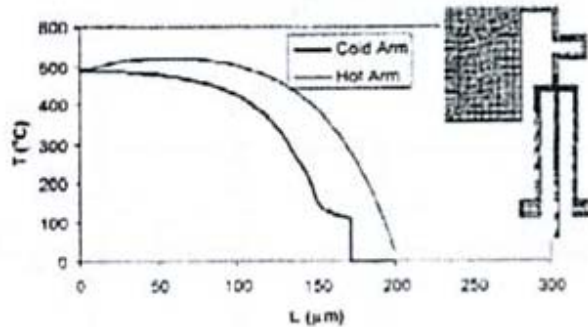
- capacitor designed for milimeter-wave (up to 40GHz) applications using standard MUMP's process (poly-Si and gold) and transfer of the device on ceramics substrate
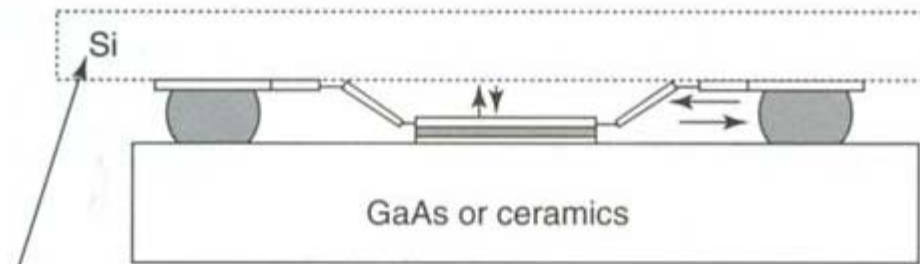- **actuation is electro-thermal by 4 vertical electrothermal actuators** (hot & cold arms)

Performance:
TR=2.7:1
Q=300 @
C=0.1pF, 10GHz

Z. Feng, W. Zhang, B. Su, K.F. Harsh, K.C. Gupta, V. Bright, Y.C. Lee, Microwave Symposium Digest, 1999 IEEE MTT-S International , Volume: 4 , June 1999, pp. 1507–1510.

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Temperature gradient causes a vertical displacement

Electro-thermal tuning

Figure 4.39 Flip-chip assembly of silicon-based MEMS. Reproduced from K.F. Harsh, B. Su, W. Zhang, V.M. Bright and Y.C. Lee, 2000, 'The realization and design considerations of flip-chip integrated MEMS tunable capacitor', *Sensors and Actuators A: Physical* **80**: 108–118, with permission from Elsevier Science, © 2000 Elsevier Science
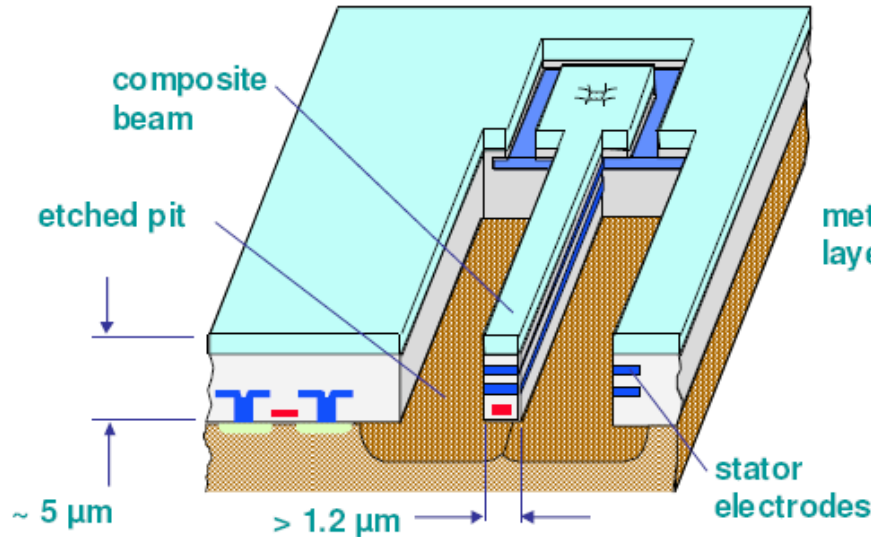
Varadan

Variable capacitors in CMOS-MEMS
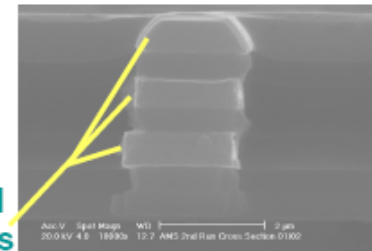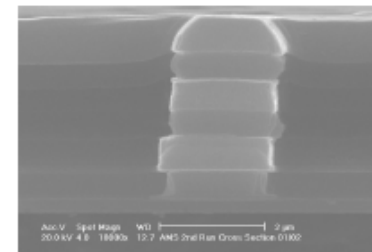

ASIMPS: CMOS-MEMS Process

CNRS – INPG – UJF

- Microstructures made from conventional CMOS followed by two maskless post-CMOS process steps

composite beam

etched pit

metal layers

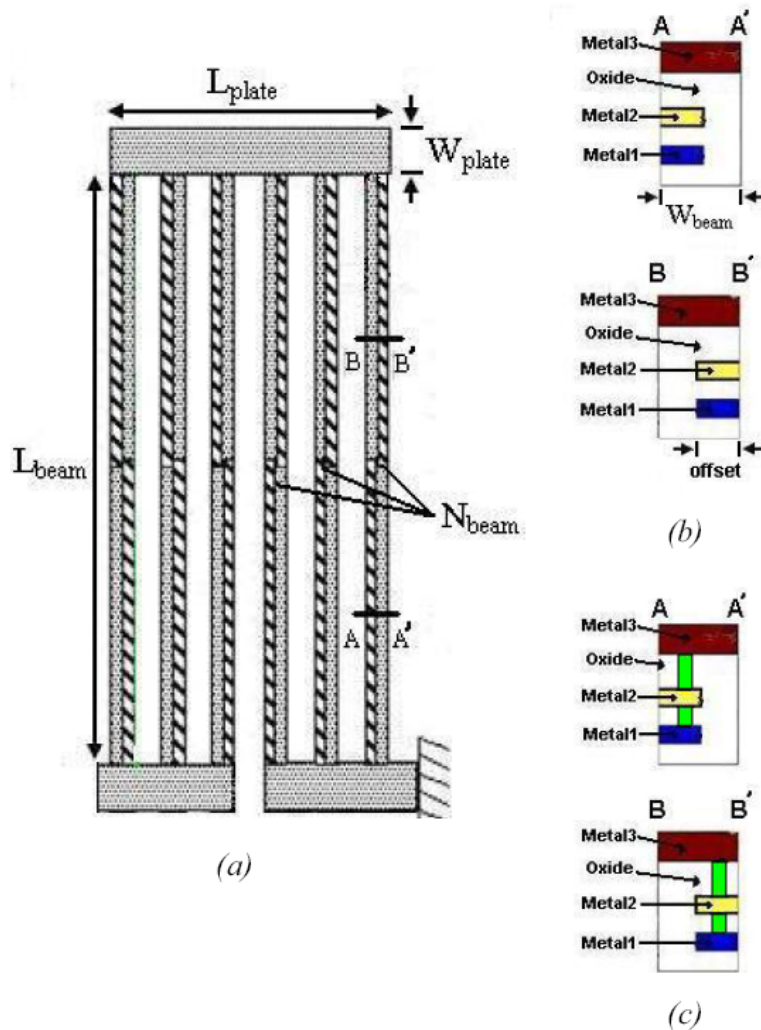M1-2-3 with field oxide

~ 5 µm

> 1.2 µm

stator electrodes

M1-2-3 w/o field oxide

- **Potential Applications**
  - Inertial sensors, RF MEMS, infrared sensors, flow and force sensors, … with on-chip detection and conditioning

G. Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

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CMOS-MEMS:
Lateral displacement due to different stress gradients in metal and Dielectrics

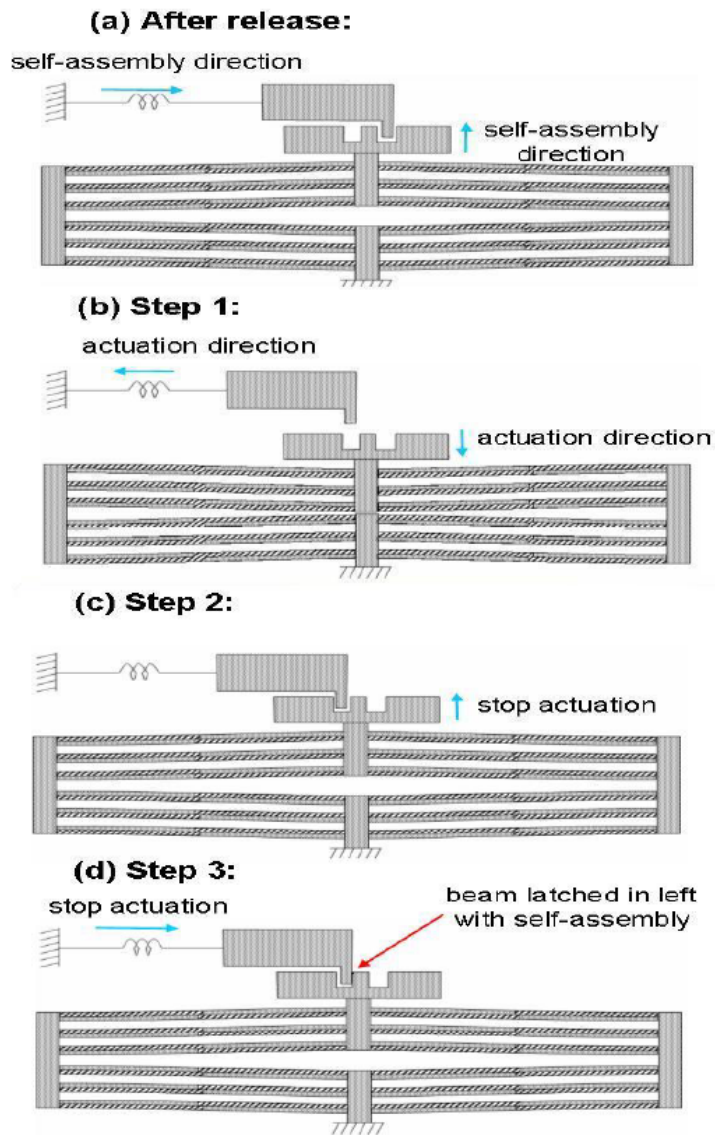The effect can be changed by rising the temperature →

Figure 1. (a) Layout and design parameters for a folded-flexure micromover, (b) Cross section of the micromover beams at two positions, showing the embedded metal offset, (c) Cross section of the micromover beams with vias between metal layers.

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(a) After release:

self-assembly direction

↑ self-assembly direction

(b) Step 1:

actuation direction

↓ actuation direction

(c) Step 2:

↑ stop actuation

(d) Step 3:

stop actuation

beam latched in left with self-assembly

Figure 5. Sequential steps for lateral latch mechanism.

Different thermal expansion coefficients (TCEs) for Al and dielectrics causes movement upon heating
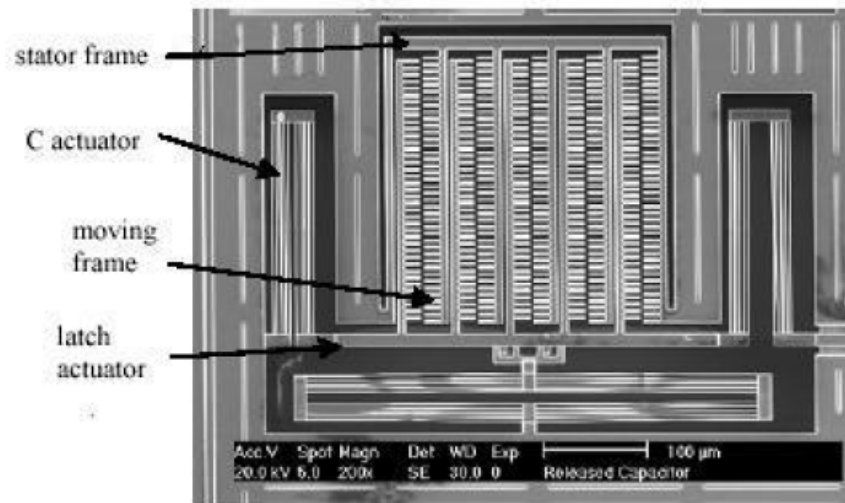
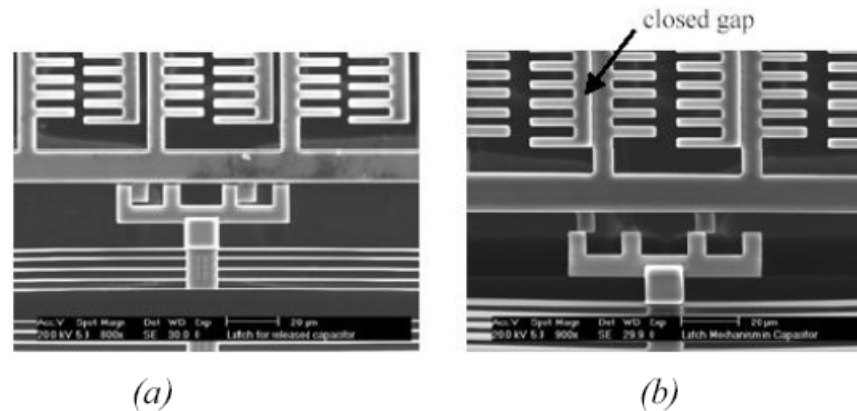(Master thesis NANO 09: Bård E. Nordbø)

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Full-size actuators   Fingers   Latch mechanism

Offset
metal
layers
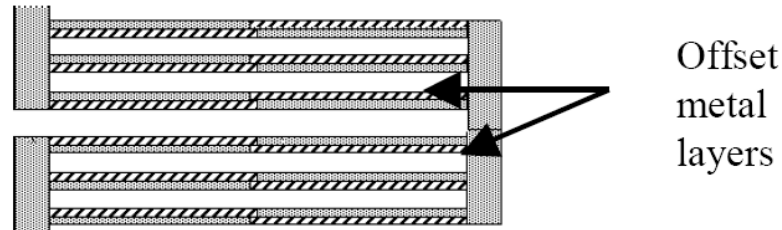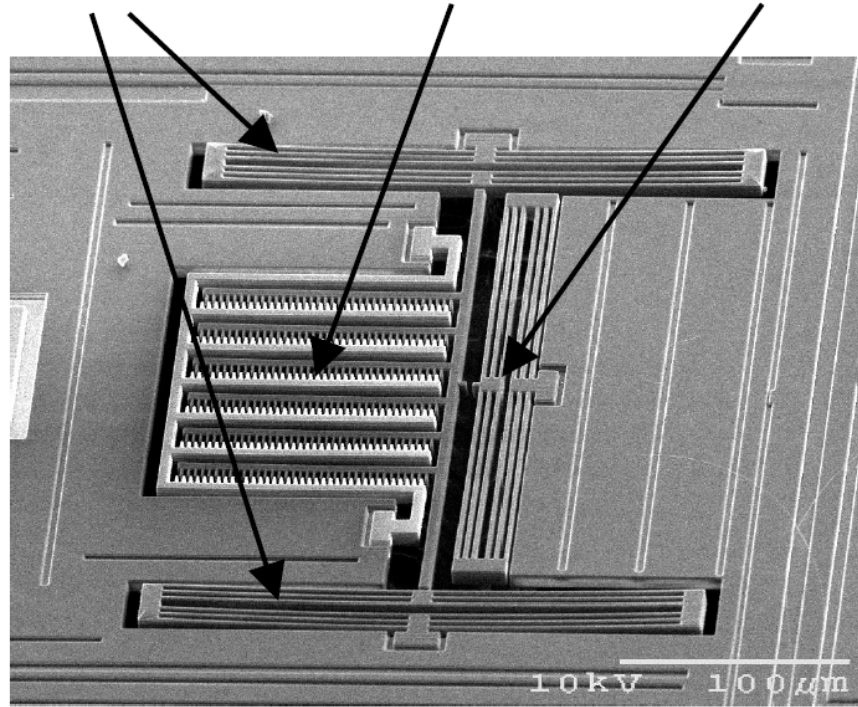
Figure 2. (a) SEM of a released capacitor in the TSMC 0.35 μm CMOS process with full-size actuators. (b) half-size actuator layout.

Carnegie Mellon University   54

Figure 6. An unengaged comb-finger tunable capacitor.

Figure 7. Capacitor latching. (a) A disengaged comb finger latch state, (b) A different latch state, where the comb truss beams contact mechanically.

Carnegie Mellon University
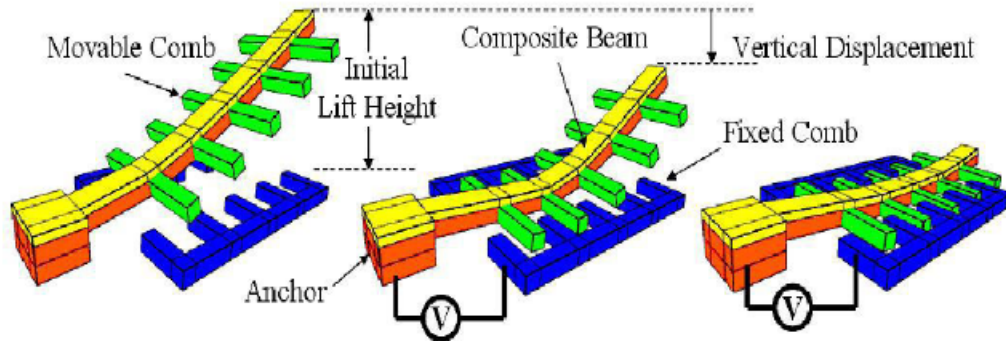
Vertical curling upon post-CMOS release

Figure 1. The resonator at different driving states. (a) Initial state. (b) Bias voltage state. (c) Critical bias voltage state.
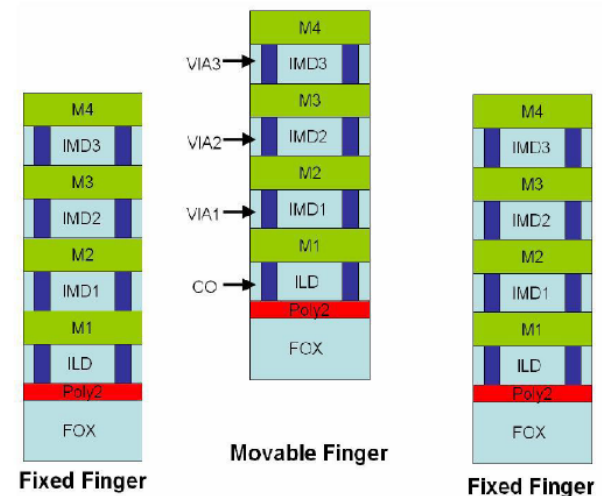

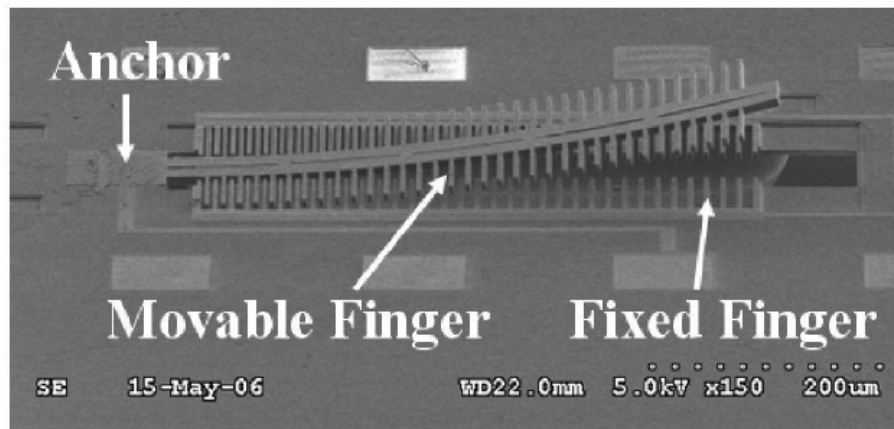Figure 3. Cross-section of the movable and fixed comb.

Figure 4. Fabricated resonator device.

The effect can be used for making variable C! (Master thesis NANO 09)

National Chung Hsing Univ, Taiwan, Dai et a

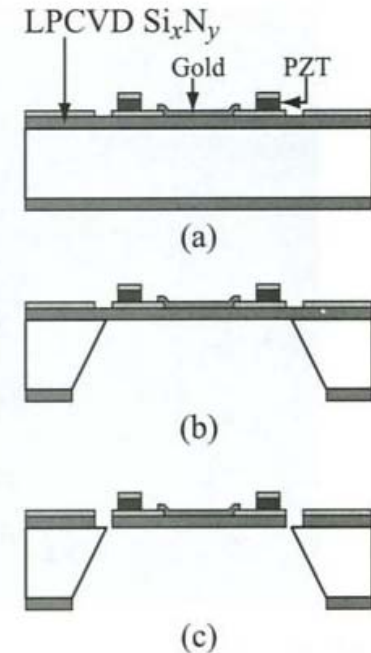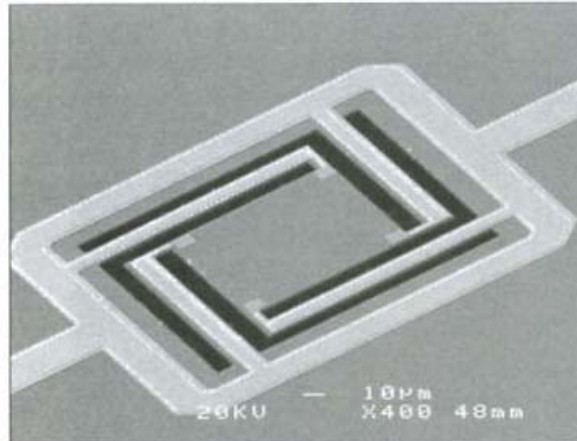Master thesis NANO 09: Kristian G. Kjelgård

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Piezoelectric tuning

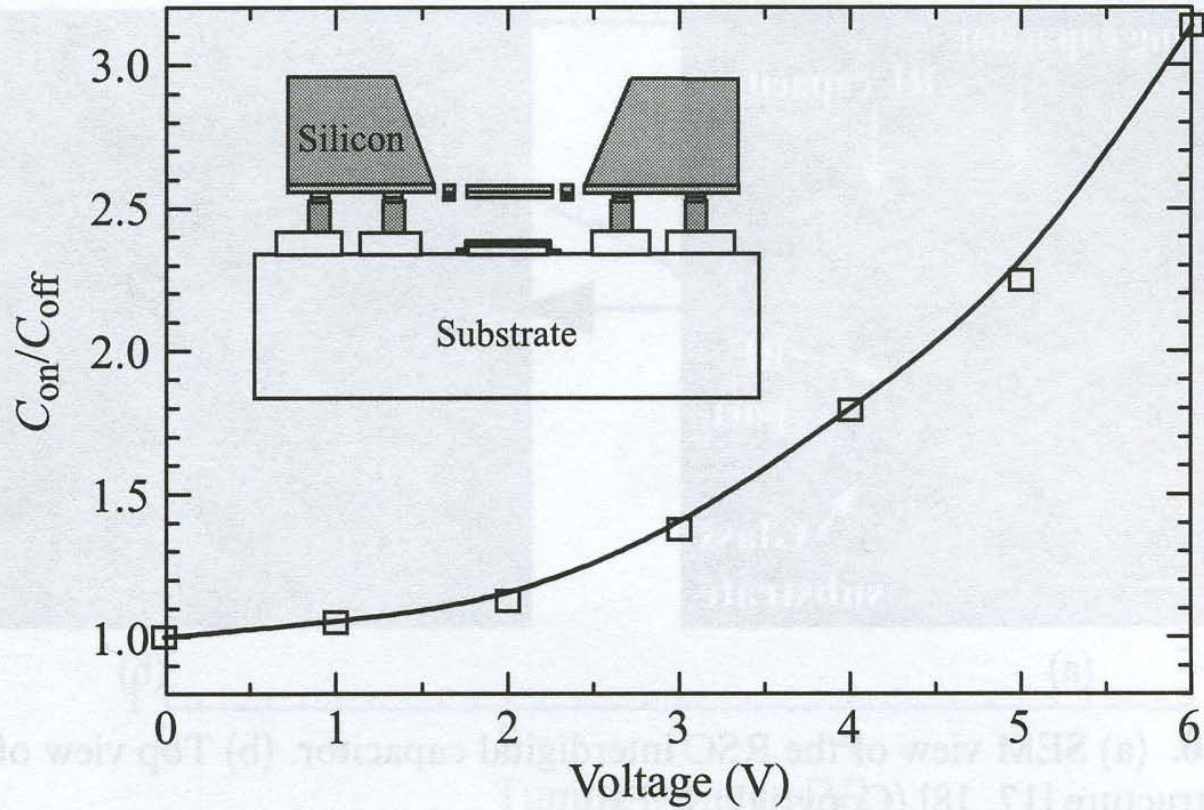A bias voltage causes the capacitor plate to move vertically
+ Low drive-voltage
+ Linear tuning of capacitance

Two of the beam lengths increase

Figure 11.17. Top view and fabrication process of the LG-Electronics piezoelectric varactor [15] (Copyright IEEE).

Rebeiz

Figure 11.18. Measured capacitance ratio of the LG-Electronics piezoelectric varactor [15] (Copyright IEEE).

Rebeiz

Dielectric tunable capacitances

- **Change the material properties between plates**
  - DC bias voltage can change electrical properties
    - Dielectric layer
    - Dielectric constant, ε
  - Ferro-electric thin-films, Var fig. 4.48 →
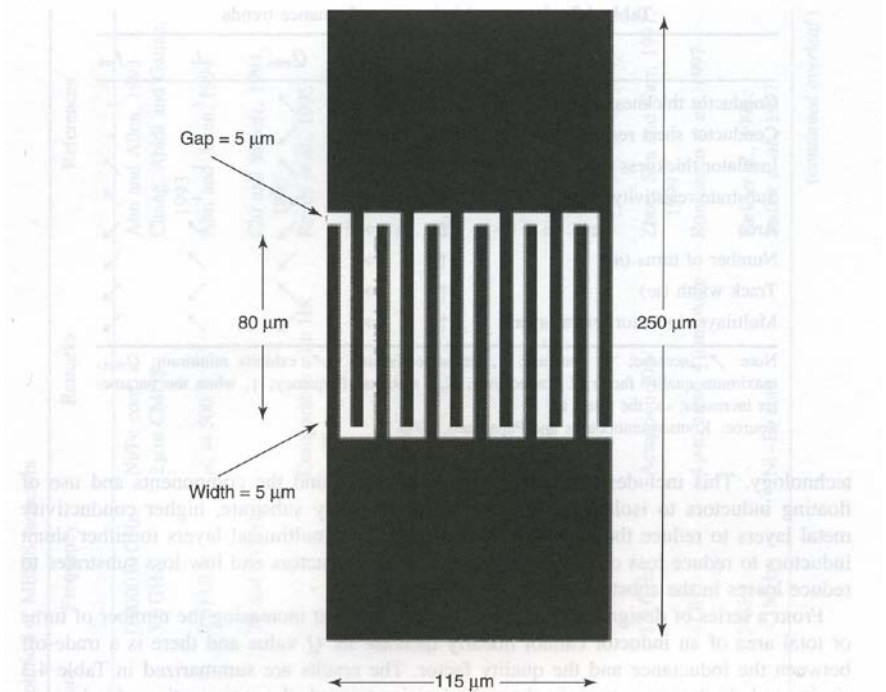
Figure 4.48 Schematic diagram and dimensions of the interdigital capacitor. Reproduced from S.W. Kirchoefer, J.M. Pond, A.C. Carter, W. Change, K.K. Agarwal, J.S. Horwitz and D.B. Chrisey, 1998, 'Microwave properties of $Sr_{0.5}Ba_{0.5}TiO_3$ thin film interdigitated capacitors', *Microwave and Optical Technology Letters* **18**(3): 168–171, by permission of IEEE, © 1998 IEEE

University of Michigan

(a)

(b)
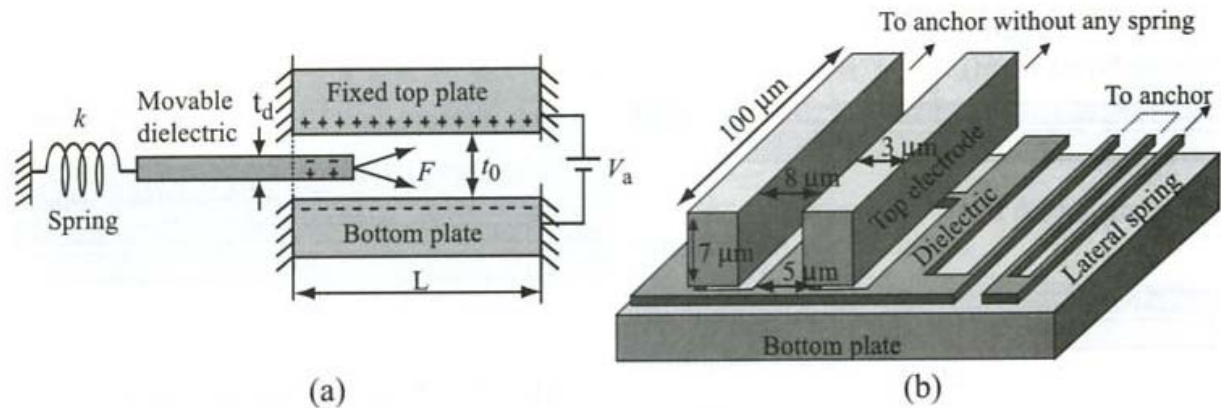
Movable dielectric membrane between fixed plates, - **masking** the effective area

Principle: both top and bottom are rigid

Tuning by a **movable** dielectric membrane (high-k = ε) that is electrostatically actuated
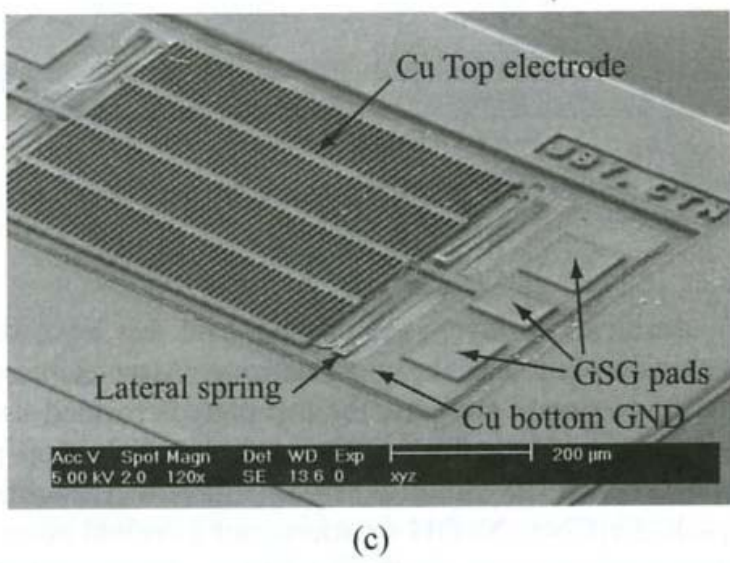
(c)

Figure 11.23. The UoM interdigital capacitor with a movable dielectric layer (a,b), and SEM picture of the fabricated device (c) [19] (Copyright IEEE).

Rebeiz

Univ of Micigan, contd.

- Performance parameters
  - IC compatible technology (<200 ° C), post CMOS
  - Electroplated metal + surface micromachining
  - Movable dielectric Nitride membrane
  - No pull-in effect
  - Low actuation voltage < 10 V with k = 0.187 N/m
  - TR = 40%
  - Q = 218 @ 1 GHz for C = 1.14 pF design (maybe the highest Q published!)
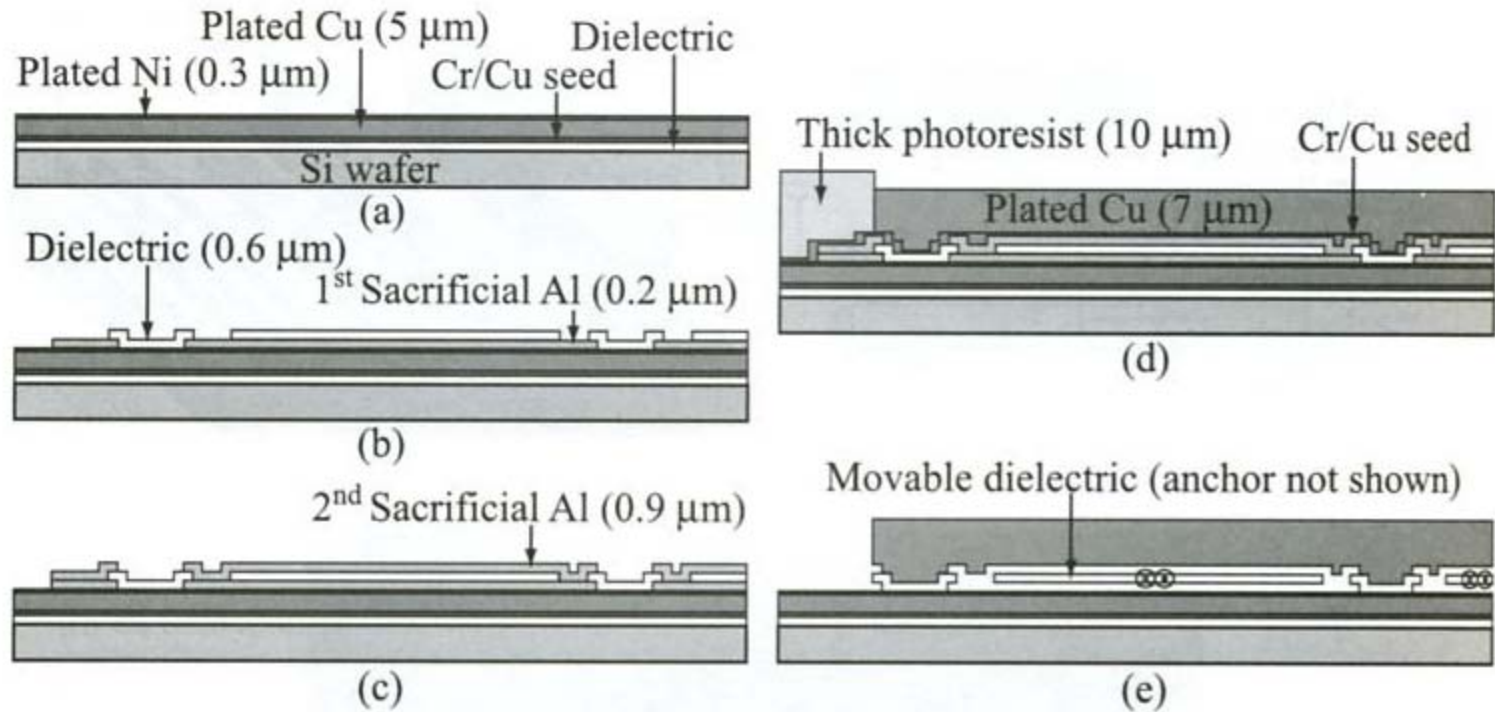
Univ of Micigan, contd.

**Figure 11.24.** Fabrication process of the UoM interdigital capacitor [19] (Copyright IEEE).

Rebeiz

RF MEMS capacitance banks

- Use of programmable capacitance banks
  - Use an "array" of fixed capacitances
  - Connect to the desired C-value
  - MEMS switches used for connecting
  - Can be programmed using a digital signal

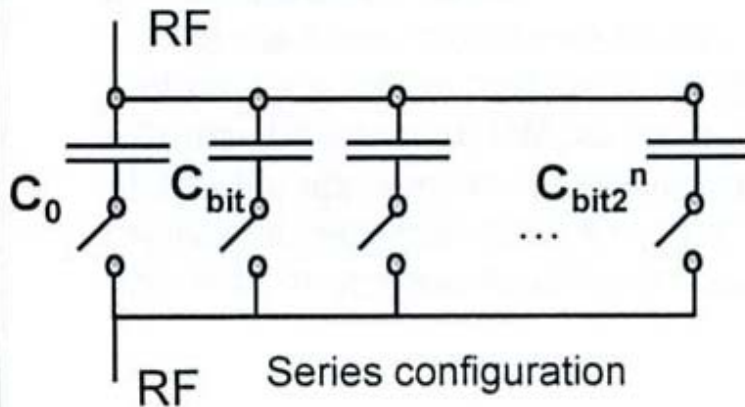 - Both series and shunt configurations are possible
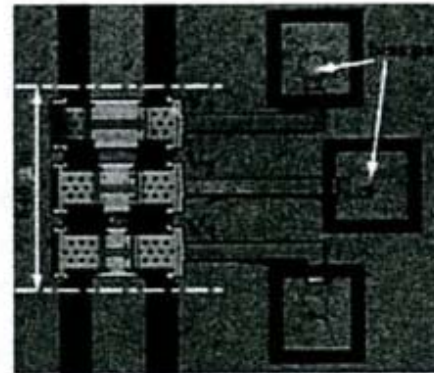
RF MEMS capacitor banks

n-bit capacitor bank with capacitive switch and fixed C_0

RF ... RF

C_0 C_{bit} C_{bit2}^n

Shunt configuration

RF

C_0 C_{bit} C_{bit2}^n ...
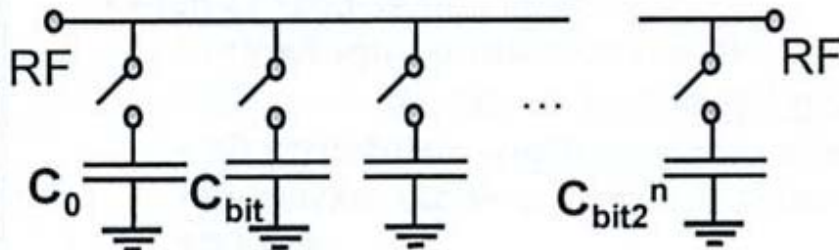
RF Series configuration

Design and process (University of Michigan)
• 3-bit digital MEMA varactor on glass substrate

Performance
• **TR= 3:1**, C=146- 430fF in K-band
• Q= 5 – 10 @ 10GHz
• Q > 50 – 200 reported by same authors

L. Dussopt and G. Rebeiz, IEEE Microwave and wireless comp. Letts, vol. 14, 2003, pp. 361-363.

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Ionescu, EPFL

Eliminate influence of thermal stress

- One example
    - H. Nieminen et al: "Design of a Temperature-Stable RF MEMS Capacitor, J MMSyst, vol 13, no 5, 2004:
    - Design capacitance into a **frame-structure** →
    - Use frame to compensate the thermal induced stress
    - Anchor the capacitance in such a way that when the frame is **deformed**, minimal stress is induced on the capacitance itself
        - Ex. corners displace very little
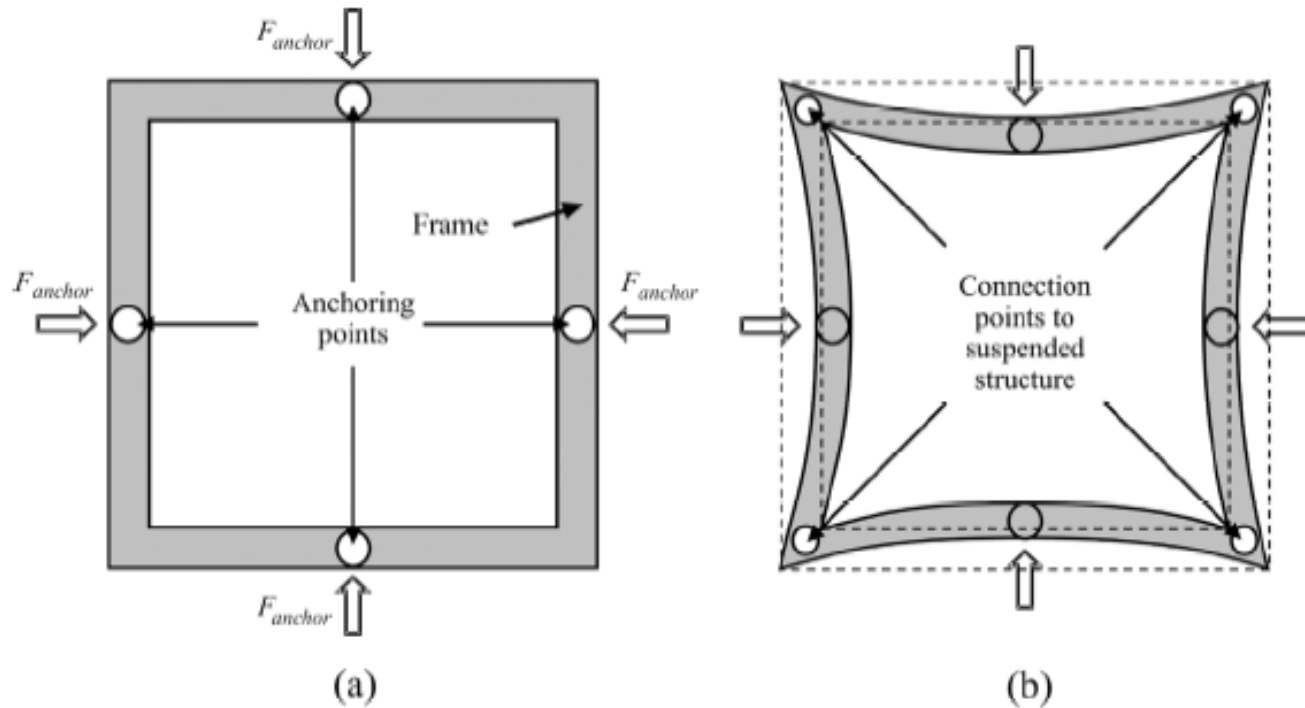   - **Anchor the capacitance at the corners!**

Fig. 2. The steps to create geometrical compensation of a suspended structure against external stress for arbitrary geometry are as follows. (a) Create frame geometry. Designate anchoring points. The force (F_{anchor}) that simulates the effect of external stress is exerted on these anchoring points. The force is directed to the geometrical center of the frame. (b) The frame bends due to the force. However, if the anchoring points and the geometry of the frame are selected properly, there are points in the frame that do not move or move very slightly. These are points where the frame is connected to the suspended structure.
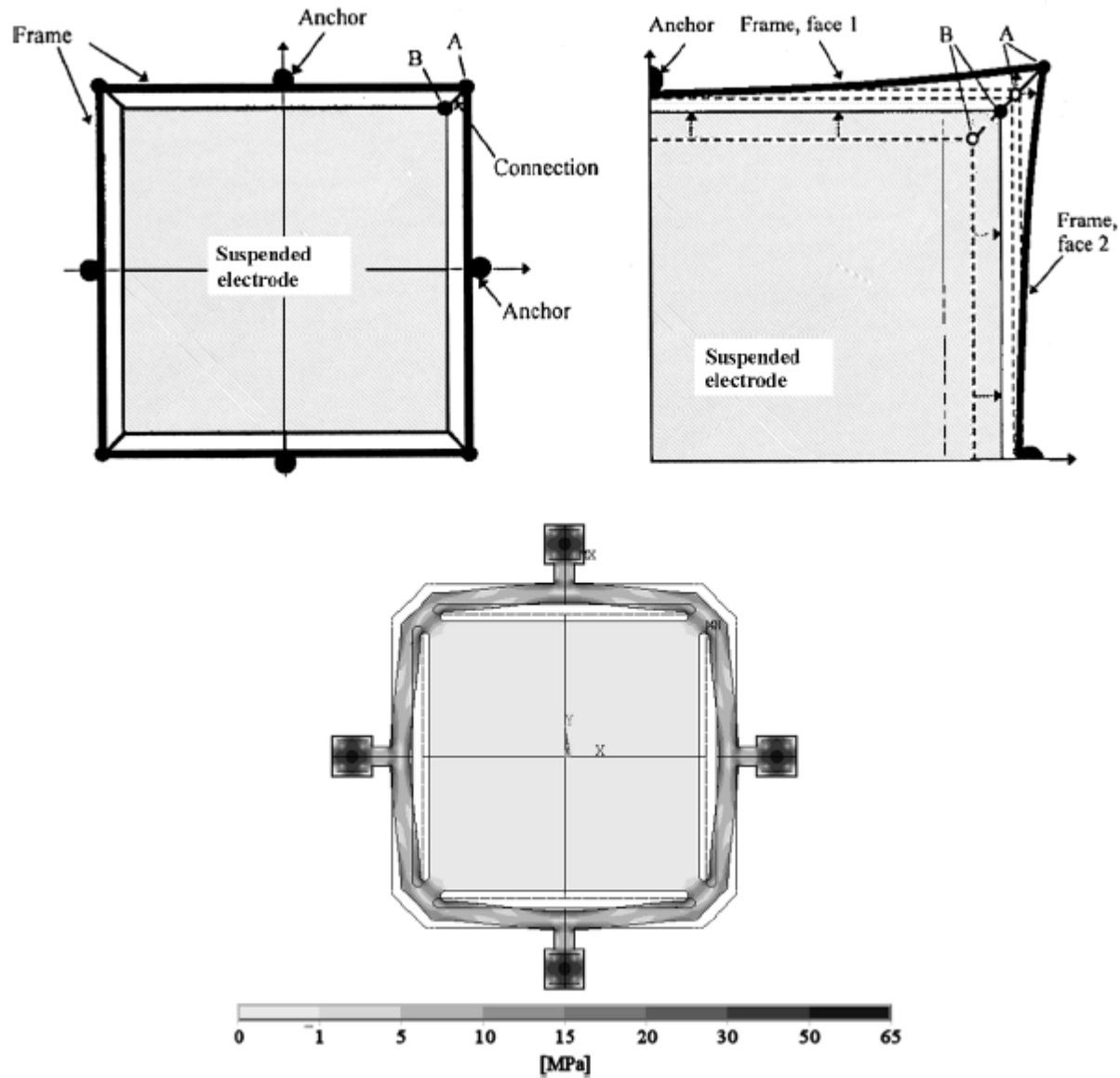
Fig. 3. FEM analysis of the temperature-compensated capacitor. Simulation is done with ANSYS. The temperature change is $-50\,°C$. The substrate is silicon. The suspended electrode, the frame and the anchors are 4-μm-thick gold. The scale at the bottom of the figure shows stress. Displacements in the figure are exaggerated.