INF 5490 RF MEMS

LN13: Integration and packaging

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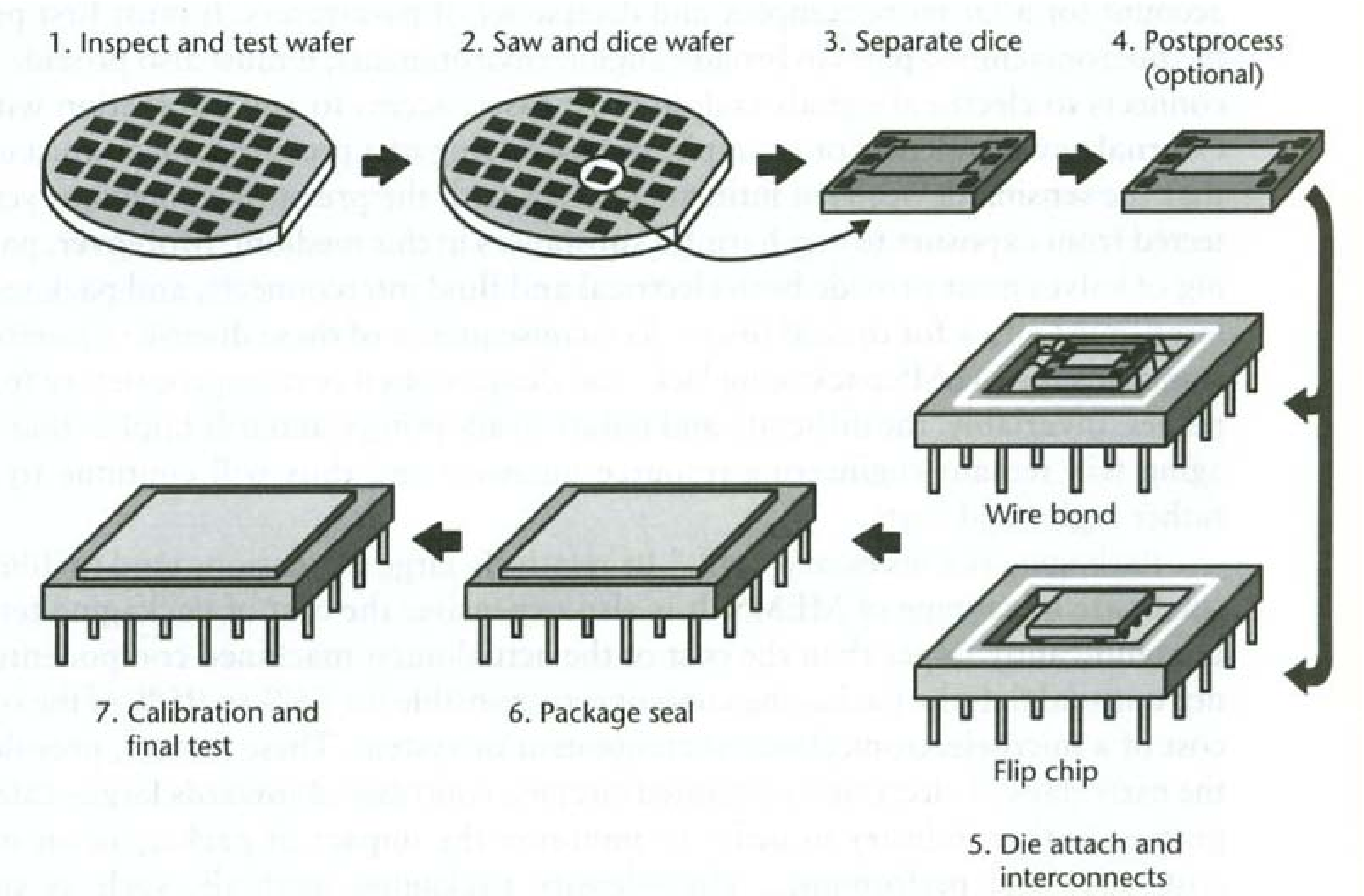
Today’s lecture

- Packaging of MEMS
- Packaging technology
- Different types of packages
- Quality control and reliability
- Integration of IC and MEMS

Purpose of packaging

- **Packaging** is needed for a **secure** and **reliable** interaction with the environment
- Package:
  - Is a mechanical **support**
  - Gives environmental **protection**
  - Provides **heat transport**
  - Offers electrical **signal connections**
  - Makes **contact** to the physical world / environment
    - Pressure sensor
    - Liquid system

Simplified packaging procedure



Packaging of MEMS

- Techniques from IC-industry have been adopted
- MEMS-packaging is more **complicated** than IC-packaging
  - Application specific, customized
  - High diversity
  - Unique requirements
  - E.g. circuits may have fragile micro structures

- **MEMS requirements:** <u>access to outside world needed**!**</u>
  - To allow mechanical interaction
  - Ex. movable structures on the surface of the wafer

Packaging of MEMS

- **→ Design of MEMS and packaging are highly inter-related**

- No standards exist
  - Often proprietary company packaging
  - ”cross-disciplinary” information is insufficient

- **”Packaging of MEMS is an art, rather than science”**

Important issues for packaging

- Reduce cost
- Maintain component performance
- Secure high packaging yield
- Obtain environmental protection
- Have thermal stability
- Cope with mechanical stress
- Allow post-packaging calibration

Important issues for packaging

- Cost
  - – Packaging may dominate total cost!
    - 75 – 95% of total cost
- <u>Component performance </u>should not degrade during packaging
  - – Ensure high reliability under normal operation
- Secure high <u>”yield” in production</u>
  - – Small amount of scrape during packaging

Environmental protection

- Protection against humidity
  - → to hinder corrosion
    - Al corrodes fast, gold slower
- Protection against liquids and gasses
  - **Hermetic packaging**
- Hinder pollution from particles/molecules
  - ”contamination”
  - **Protective coatings** used
    - Ex. **parylene** (poly polymer) is often used
- Isolation from mechanical chock, vibrations and unwanted acceleration
- Isolation from electric fields

Thermal issues

- **Thermal budget** for packaging is important
  - Components should not degrade due to high temperature steps
- **Thermal conductivity**
  - Metals and some ceramic materials have high thermal conductivity
  - ”die-attach”-material should have high thermal conductivity
- **Thermal coefficient of expansion** (TCE) in package should be similar to the MEMS-component TCE
  - Otherwise stress and cracks may arise
- **Thermal dissipation** is usually not a big problem
  - BUT, cooling of thermal MEMS actuators must be ensured
  - Cooling may be needed when integrating MEMS with other units (amplifiers)
- **Thermal stability** must be ensured and fluctuations avoided
  - MEMS on thick or thin membranes has different thermal stability
- **Thermal analysis** of die or package should be done
  - Sectioning into temperature zones

Other issues

- Mechanical stress
  - Piezoresistive and piezoelectric units should avoid unwanted stress from package or bonding
  - Thermal coefficients of expansion (TCEs) must ”match”
    - Will hinder stress
  - Long term drift properties of **adhesives** connecting die and package may introduce stress
    - **”slow creep”**
- Calibration
  - Calibration is often needed after packaging
  - Laser trimming of resistors
    - ”laser ablation”
  - Laser trimming of critical metal dimensions
    - ”tuning fork”
  - Today: more and more **”electronic” calibration** is used

Some packaging technologies

- Next →
  - Hermetic packaging
  - Wafer-level packaging
    - Microcaps
  - Die-attach
  - Wire bonding
  - Flip-chip bonding

Hermetic packaging

- Will give ”sealed package”
  - Increases **long term stability** of component
- Package of ceramics or metal must be used
  - Polymer (plastic) packages are not hermetic!
- Packaging materials may outgas, leading to performance degradation
- Package must often be filled with inert gas
  - Nitrogen, Argon, Helium
- Hermetic package is not generally applicable
  - MEMS often **interact** with the outside world, measure variables etc.
- **Vacuum packaging** must be used to obtain high Q in vibrating resonators
  - Vacuum requirement almost universal, - not only for resonators and filters

Wafer-level packaging

- Packaging partly done during fabrication process
- Wafers of same or different materials are bonded together (anodic bonding)
  - May implement free mechanical movement of MEMS structures inside **internal cavities**
  - Ex. piezoresistiv pressure sensor using Si to glass bonding
- Large thickness of ”stacked wafers” is a challenge
  - ”Stack” of bonded wafers may be 1 mm!

Microcaps

- Top Si microcap mounted by using ”fusion bonding”
  - Bonded caps give hermetic sealing and protection

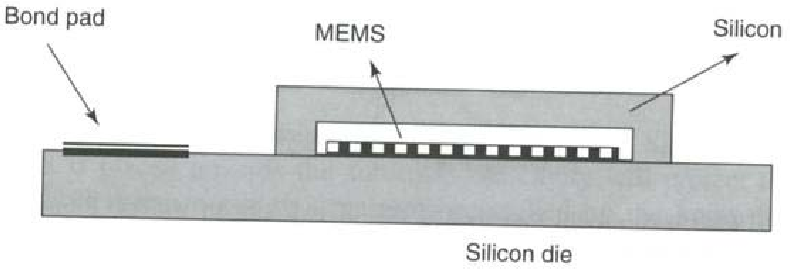


Figure 9.5 Silicon wafer-level packaging of RF MEMS

- Hinder damage from dicing, mounting and atmosphere
  - Sawing – dicing of wafer
    - Critical with respect to fragments, shaking, cooling liquid!
    - Ex. Perform etching of last sacrificial layer **after** sawing
- Conductive ”caps” can also give electromagnetic shielding, if grounded
- **Conventional methods** can then be used for the **succeeding** packaging process steps
  - Use of ”microcap” may allow polymer package (low cost)

Wafer-level **vacuum** encapsulation

- A **planar process** used to implement a “cap” which encapsulates the active unit:

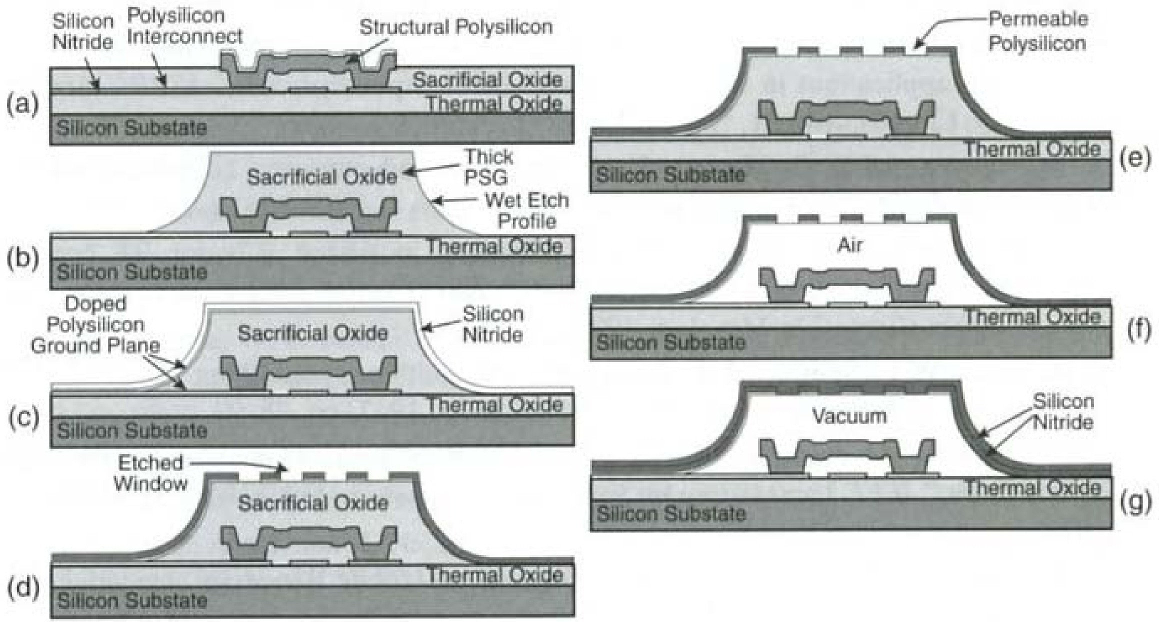


Figure 12.31. Process flow for vacuum-encapsulating a micromechanical resonator via planar processing. (a) Cross section immediately after the structural poly etch. (b) Deposit and pattern a thick, reflown PSG. (c) Deposit upper ground plane polysilicon and first nitride cap film. (d) Pattern etch windows in the cap. (e) Deposit permeable polysilicon [55]. (d) Etch sacrificial oxide (i.e., release structures) using HF, which accesses the sacrificial oxide through the permeable polysilicon, then dry via supercritical CO_2 [56], yielding the cross section in (f). (g) Seal shell under vacuum via a second cap nitride deposition done via LPCVD. Details for this process can be found in Lebouitz et al. [55].

Itoh et al

Example of other types of ”caps”

- A ”cap” is riveted to the substrate using nickel microrivets

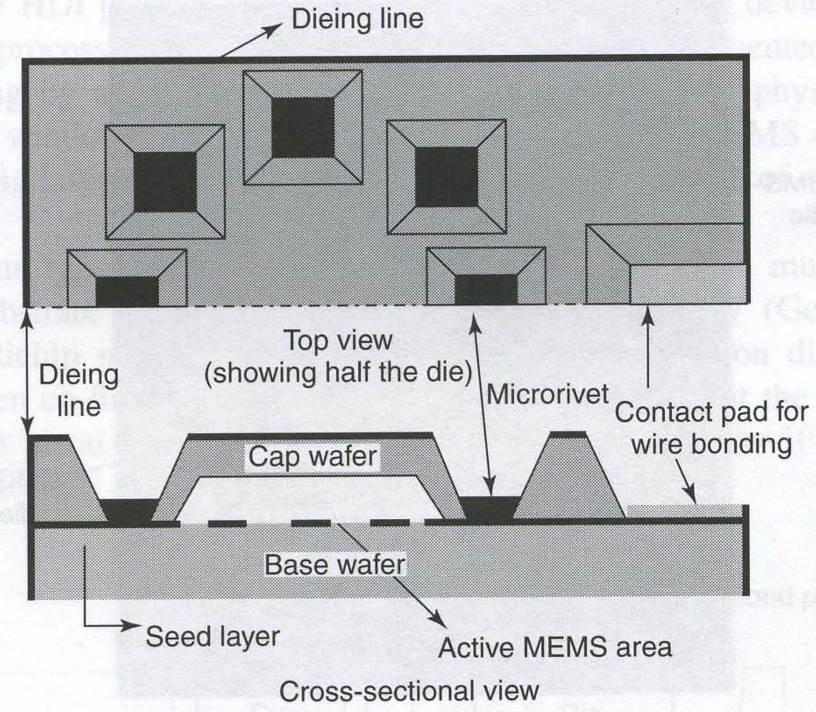


Figure 9.14 View of a packaged chip using microrivets. Reproduced from B. Shivkumar and C.J. Kim, 1997, ‘Microrivets for MEMS packaging: concept, fabrication and strength testing’, *Journal of Microelectromechanical Systems* **6**(3): 217–225, by permission of IEEE, © 1997 IEEE

”klinking”

”Die-attach” process

- Die must be mounted on package **substrate**
  - – Substrate serves as a mechanical support

- Die connected to substrate by
  - – Soldering
  - – Organic adhesives
    - Epoxy, silicone etc.
    - Cheap, low temperature

Wire bonding

- Used for electrical interconnections
  - DC and RF-signals
- Gold wire: 150 °C
- Ultrasound frequencies 50 – 100 kHz may be a problem for MEMS
  - May give oscillations of mechanical micro structures
  - Structural errors may arise
- Aluminum wire
  - Slower
  - Substrate not heated

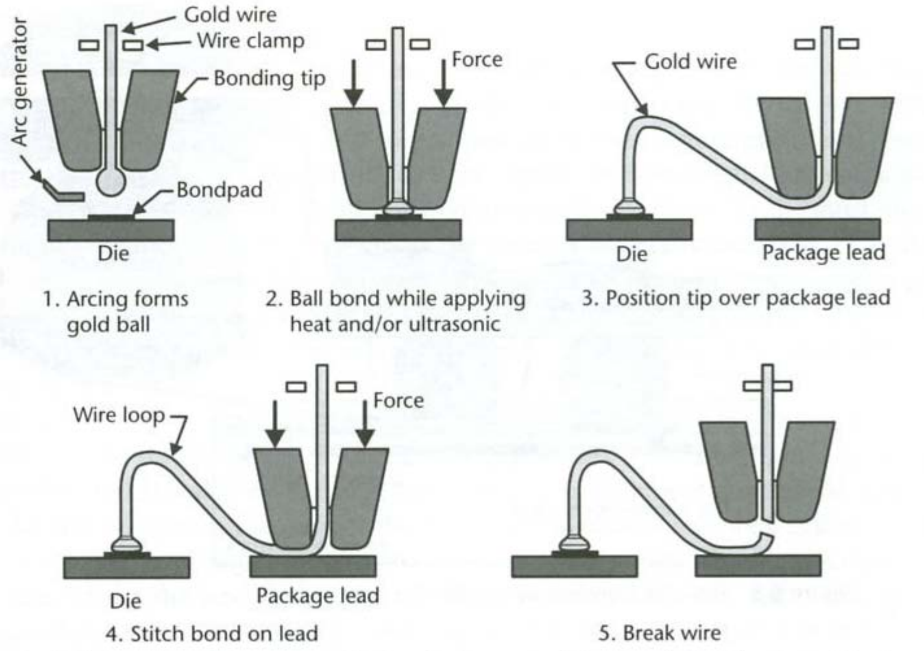


Figure 8.4 Illustration of the sequential steps in thermosonic ball and stitch bonding. The temperature of the die is typically near 150°C. Only the tip of the wire-bonding tool is shown [10].

Flip-chip bonding

- Die bonded with top surface down to a package substrate
- **Plated solder bumps** on die
- Contact points may be anywhere
  - Density of I/O increases
- Low inductance due to **short distances**
- Used for fast circuits, RF
- High reliability
  - Standard bond wires may be a reliability threat
- Many MEMS dies may be mounted on the same substrate
  - Can not be used if environmental access is needed
- Especially suitable if the MEMS die already has ”caps”

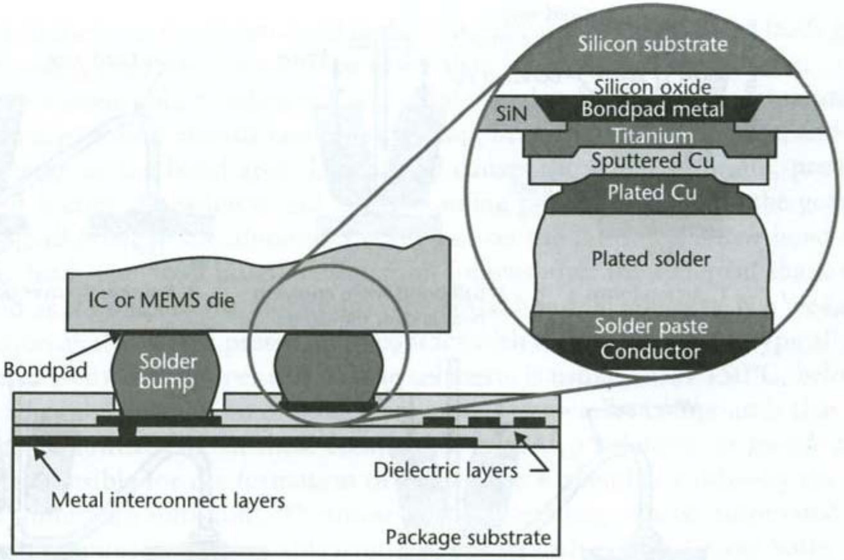


Figure 8.5 Flip-chip bonding with solder bumps.

Different packages used

- Important issues
  - Package size, form, number of pins
  - Package material
- Different package types
  - **Ceramic packages**
  - **Metal packages**
  - **Polymer packages**
- Package can be combined with a 1. level encapsulation
  - Die level encapsulation: ”microcaps”
  - Can be used if MEMS does not need direct contact with liquids and gasses

Ceramic packages

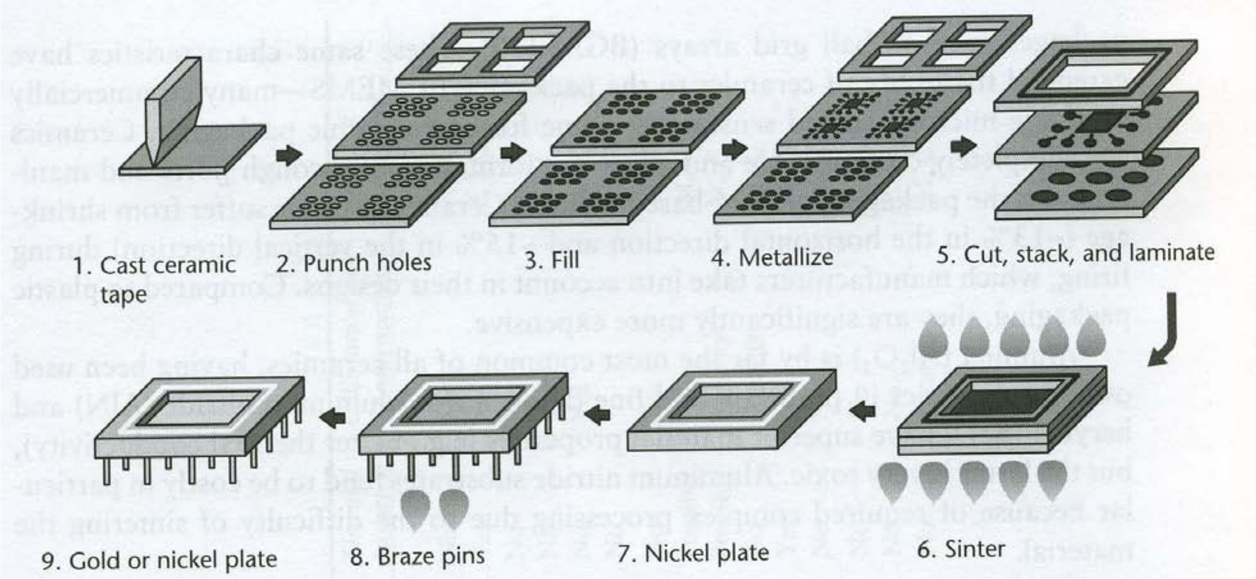
- **Ceramics** is a hard, fragile, non-metallic mineral
  - Electric insulating
  - Good thermal conductivity
  - Easy to machine
  - High reliability
- **Alumina** most common ceramic material, Al2O3
  - Also AlN, Aluminum nitride, used
- Common for IC-packaging
- Can be **sealed** (hermetic encapsulation)
  - Encapsulation and putting on a lid are important process steps
- Used for MEMS multi-chip modules
- Package can be custom or standard

- Relatively complex and costly method
  - More costly than using polymer

Laminating ceramic packages

- A ceramic package is made up of **laminates**
  - Each layer is formed and patterned individually
  - Laminates are pressed together (”sintered”, ”co-fired”) at 1500-1600 °C
    - Newer methods at lower temp (800 °C)
  - Starting material: ”green unfired soft tape”
  - Electric conductors deposited by **screen printing** on each layer
  - The result is a **”stack” of laminates** (3-16 layers)

- Heated to high temp (”firing”) for densification
- Drawback is that ceramic shrinks (13-15%) during ”firing”



Metal packages

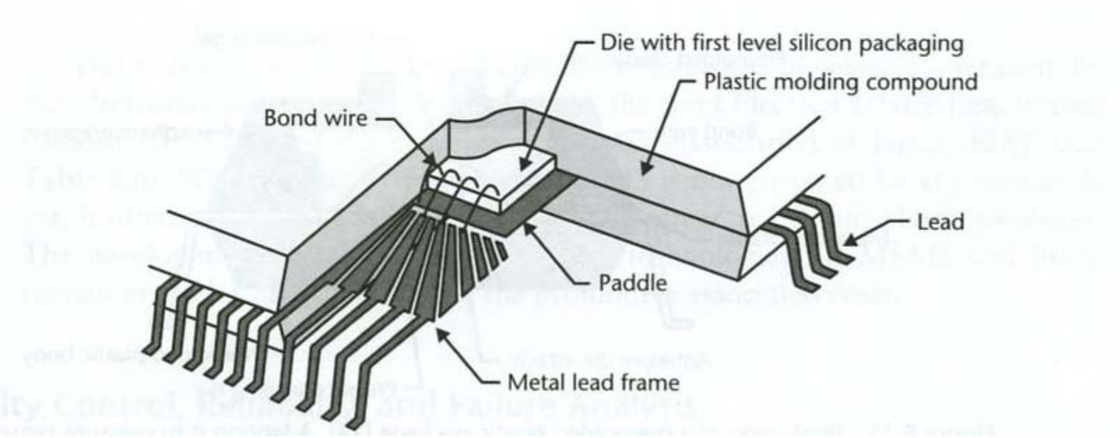
- Used for IC with few pins (”TO-can”)
- Excellent thermal dissipation
- Good electromagnetic shielding
- Often used in MMIC, ”Monolithic Microwave ICs”
- For MEMS: robust, simple to mount
  - OK number of pins for most MEMS applications
  - Several standard packages with various cavities exist
  - Simple prototyping for small volume
  - Packaging for rough environment (robust steel packages)
  - Simple sealing process
  - More expensive than polymer
- Steel or Kovar (alloy) used
  - Kovar has low TCE

Molded polymer packages

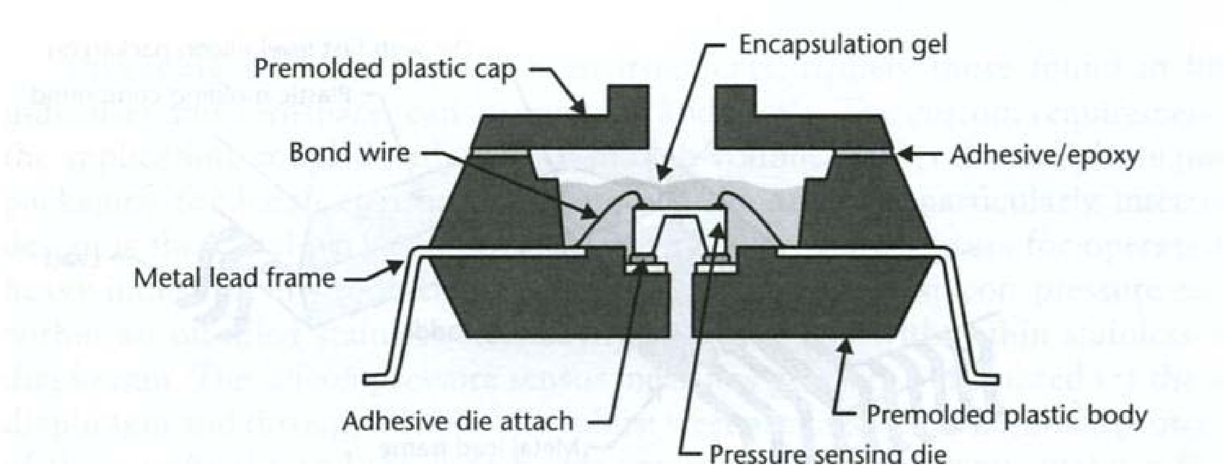
- Low cost
- Hermetic encapsulation **not** possible
- Reliability is increasing
- Polymer material is typical <u>epoxy</u>
- Often large thermal mismatch between polymer, frame and die
  - Can cause damage
  - Additives in epoxy may change TCE

- Different fabrication methods
  - **Post-molding**
    - Molded after die is fastened to lead frame
  - **Pre-molding**
    - Die fastened after molding
    - Preferred if risk of damage
    - More expensive

Post- and pre-molding



Post-molding



Pre-molding

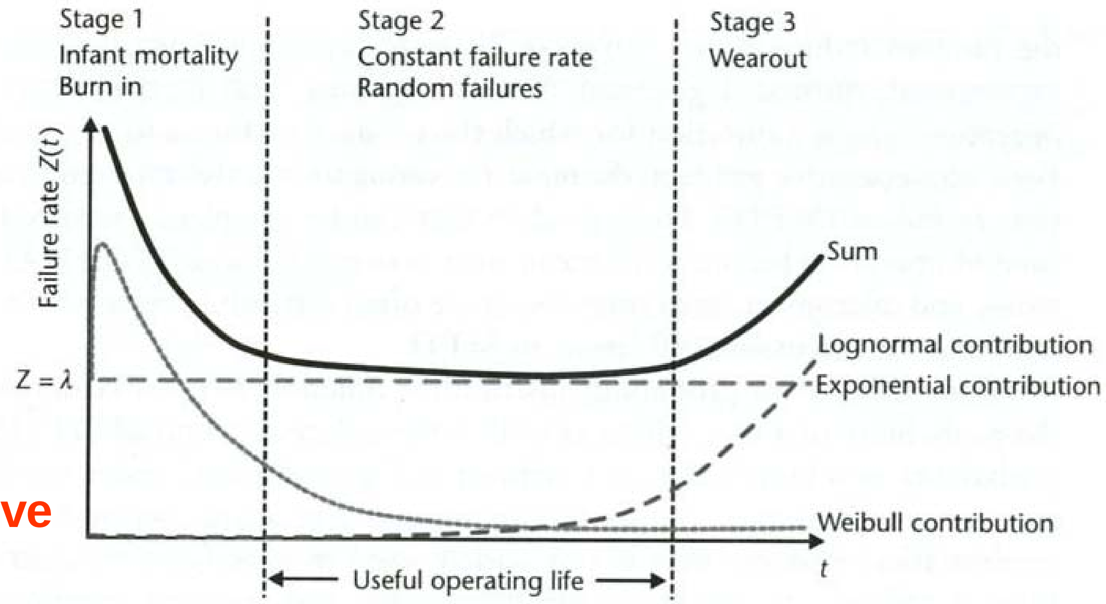
Quality control and reliability

- Quality control
  - No standards exist
  - Typical application specific standards and guidelines are used (f.ex. from automotive industry)
  - ISO 9000, QS 9000 say nothing about qualifying tests
  - **IEEE, MIL –standards** give detailed **operational tests** for qualification and reliability

- Perform statistical analysis: **failure analysis**
  - MTBF, Mean Time Between Failure
- DAC simulations may reveal points with high **stress** that could cause cracks

Operational tests

- Enforce ”demanding environments”
  - Shock, vibration, temperature, humidity
- Provoke a weak point to cause an error
  - **”burn-in”,** maximum load
  - ”infant mortality”



“Bath tube” curve

Important failure modes

- Fracture and cracks due to large stress or mechanical shock
  - Reduced by round corners, damping
- Change of elastic properties
  - Influences resonance and damping
- Delaminating of package
  - Laminate ”stack” destroyed due to bad process control
- Corrosion due to environment
  - Vapor/gas influence
  - Critical for movable parts
- ”Stiction”
  - Surfaces are “glued” together
  - Ex. Capacitive switches
  - Charging of dielectric layer can permanently keep the switch plate down
- Different electrical and thermal failure modes

Integration of IC and MEMS

- **Multi-chip module packaging**
  - Figure shows a HDI process (High Density Interconnect) where ”naked dies” are mounted in cavities in the substrate

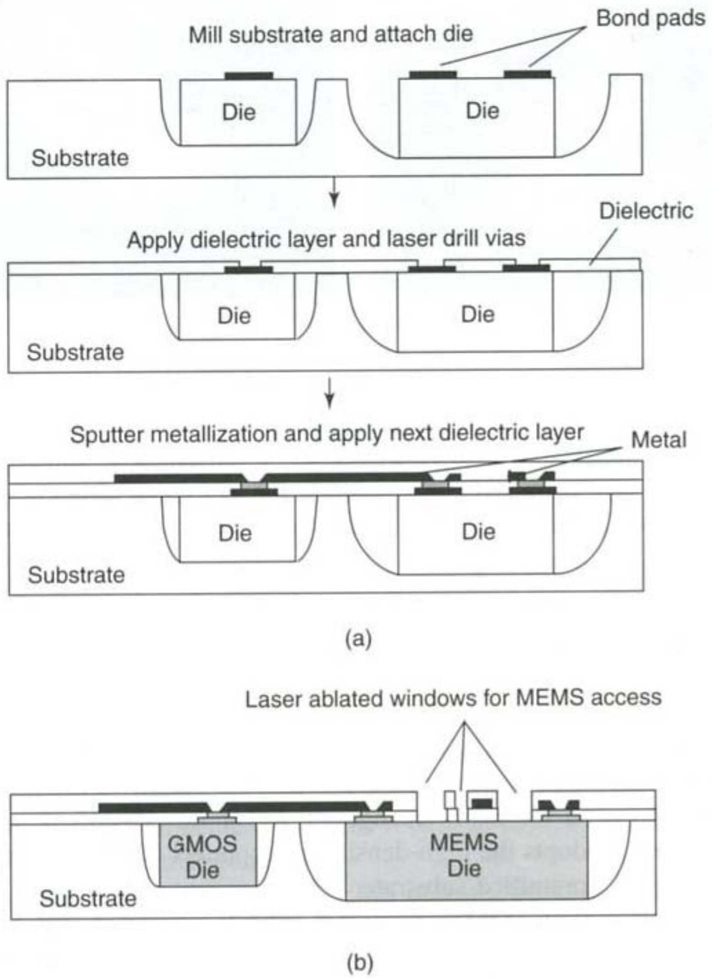


Figure 9.12 (a) High-density interconnected (HDI) process; (b) MEMS access in HDI process. Reproduced from J.T. Butler, V.M. Bright, P.B. Chu and R.J. Saia, 1998, ‘Adapting multichip module foundries for MEMS packaging’, in *Proceedings of IEEE International Conference on Multichip Modules and High-Density Packaging*, IEEE, Washington, DC: 106–111, by permission of IEEE, © 1998 IEEE

Integration of IC and MEMS, contd.

- Separate MEMS- and IC-dies can be impractical and costly
  - Often the only possibility
    - Due to different technology requirements
  - **+** MEMS and CMOS may then be individually **optimized**
  - **-** Parasitic capacitances, impedances!
  - **→ One-chip solution desired! (monolithic integration)**

- Technologies for monolithic integration
  - **Pre-circuits (Pre-CMOS)**
  - **Mixed circuit- and micromechanics (Intermediate CMOS)**
  - **Post-circuits (Post-CMOS)**

Pre-CMOS circuits

- Fabricate micromechanics first, - then IC
- Benefits
  - May fabricate MEMS optimally at high temp (+ annealing)
  - Only one passivation , **planarization** step needed after micromechanics processing
  - Can upgrade each processing module individually
- Drawbacks
  - Large topography variations present after MEMS (ex. of 9 µm)
    - Use of a trench for MEMS components
  - CMOS photo resist spinning and patterning become more difficult
    - Especially for submicron circuits
    - CMOS and MEMS have different min. geometries (waste area)!
  - Must make the surface planar before CMOS processing
  - CMOS foundry processes do not allow ”dirty” MEMS wafers into the fabrication line

Pre-CMOS circuits, contd.

- Ex. of iMEMS-process that has overcome the drawbacks
  - Process from Sandia National Laboratories →
  - The micromechanical components are made in a trench
  - Structure is planarized using CMP = Chemical Mechanical Polishing
  - Then the IC-steps are performed

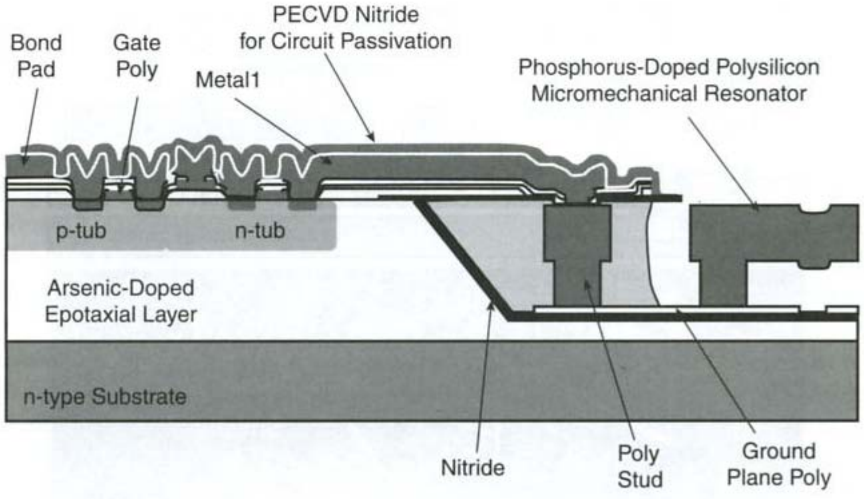
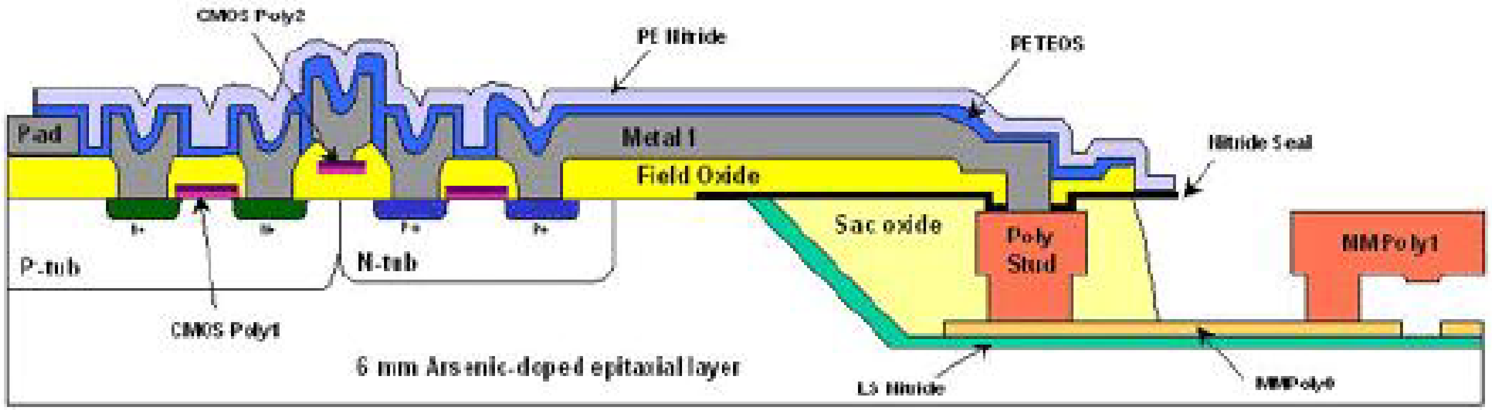


Figure 12.29. Cross section of Sandia's *iMEMS* process [48].

MEMS → CMOS

Sandia Embedded Process

1. Trench etched into Si using KOH
2. MEMS fabricated in trench
3. Trench filled with LPCVD oxide
4. Trench planarized with CMP
5. MEMS stress anneal
6. Trench seal with LPCVD nitride
7. Standard CMOS fabrication next to MEMS
8. CMOS passivated with PECVD nitride
9. Trench opened, MEMS released



Mixed circuit- and micromechanics

- IC and MEMS-processes integrated into one process
  - ”MEMS in the middle”

- Drawbacks
  - Limitations on what kind of MEMS structures that can be fabricated
  - Many passivation layers needed
    - When switching between circuit and micromechanics process
  - Only custom CMOS-processes can be used
  - Total redesign of the whole process if one of the combined technologies (“modules”) is changed
  - Ex. of a combination process →

Combination processes

- BiMOSII process from Analog Devices for fabrication of accelerometers

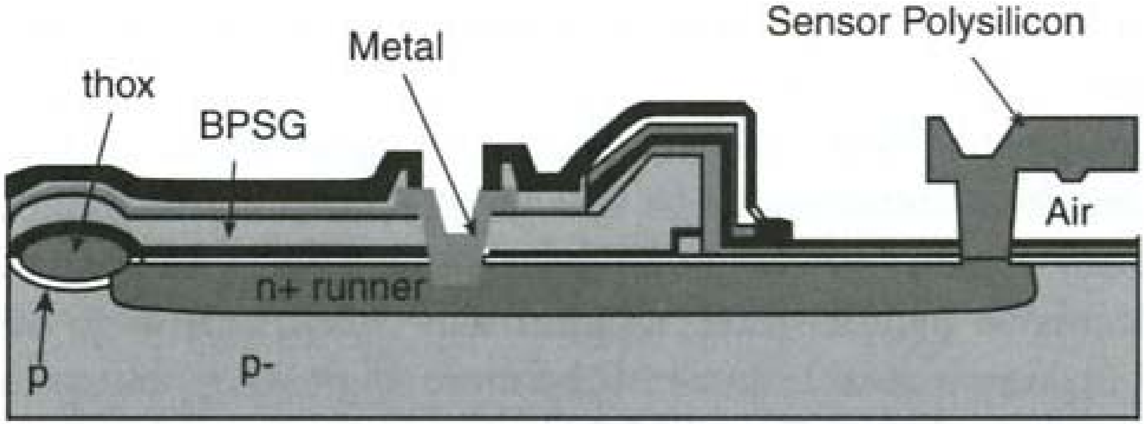


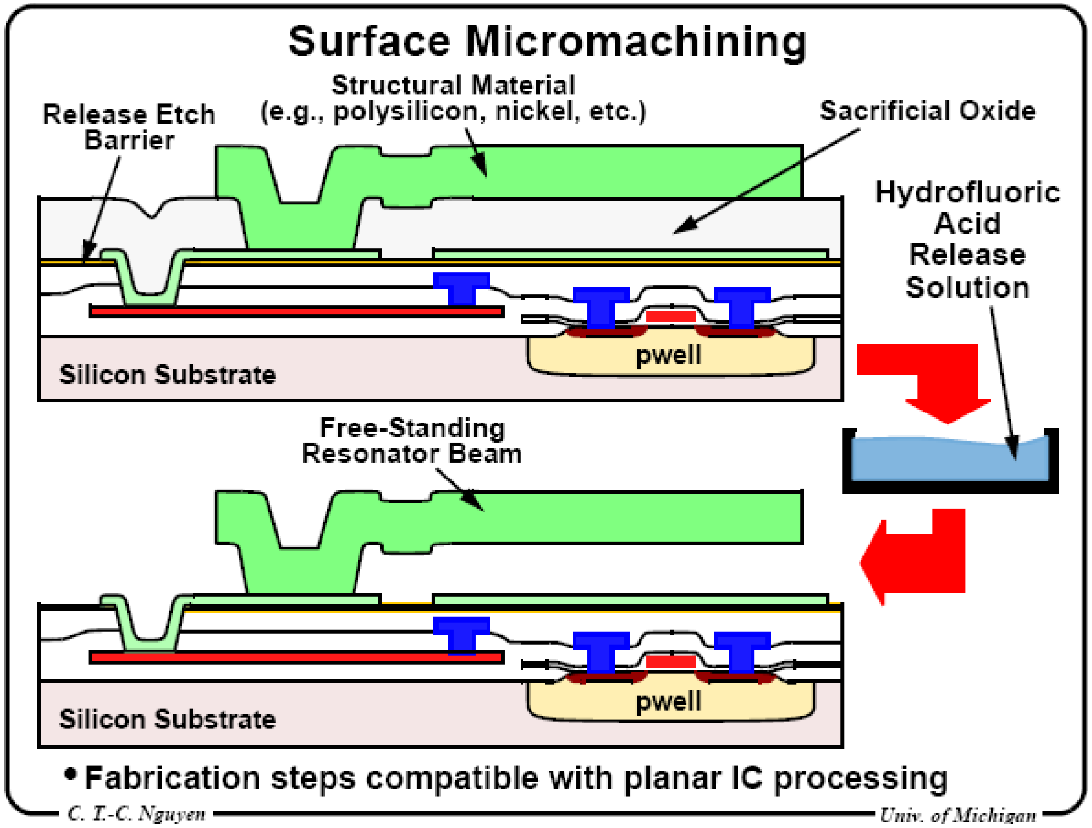
Figure 12.28. Cross section of the sensor area in Analog Devices' BiMOSII process [47].

Post-CMOS circuits

- CMOS circuit processing performed **before** MEMS
  - Possibly the most promising procedure
  - Planarization not needed
  - May use advanced/standard IC foundries and succeeding micromechanical processing
  - Method gradually developed
- Drawbacks
  - **Difficulties with CMOS Al-based metallization**
    - Al can not withstand the **high temperature steps** typically needed for several micromechanical process steps
      - Especially those needed for high Q: f.ex. polySi deposition/annealing
  - Compromises must be done for one or both processes
    - Ex. MICS process: Tungsten (“wolfram”) as CMOS metal
      - can withstand higher temp
    - Ex. UoC Berkely: use SiGe as MEMS structure material
      - lower deposition temp

MICS process

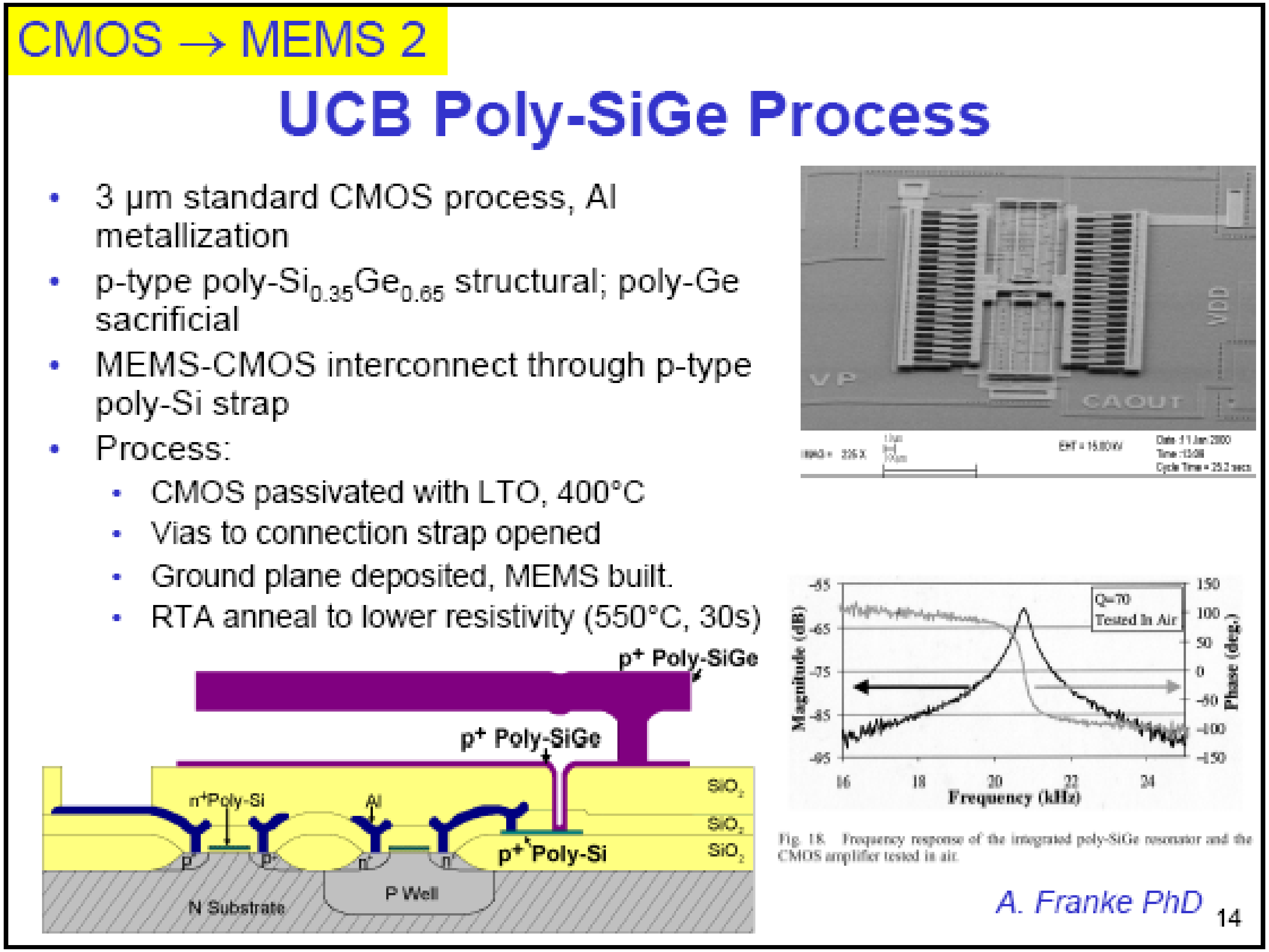
- **Tungsten** ("wolfram") used for metallization instead of Al before polySi surface micromachining process
  - Tungsten withstands higher temperatures



Al-metallization kept

Low temperature poly-SiGe used as structural material

Minimal reduction in micromechanical performance!



CMOS → MEMS 2

UCB Poly-SiGe Process

- 3 µm standard CMOS process, Al metallization
- p-type poly-$Si_{0.35}Ge_{0.65}$ structural; poly-Ge sacrificial
- MEMS-CMOS interconnect through p-type poly-Si strap
- Process:
  - CMOS passivated with LTO, 400°C
  - Vias to connection strap opened
  - Ground plane deposited, MEMS built.
  - RTA anneal to lower resistivity (550°C, 30s)

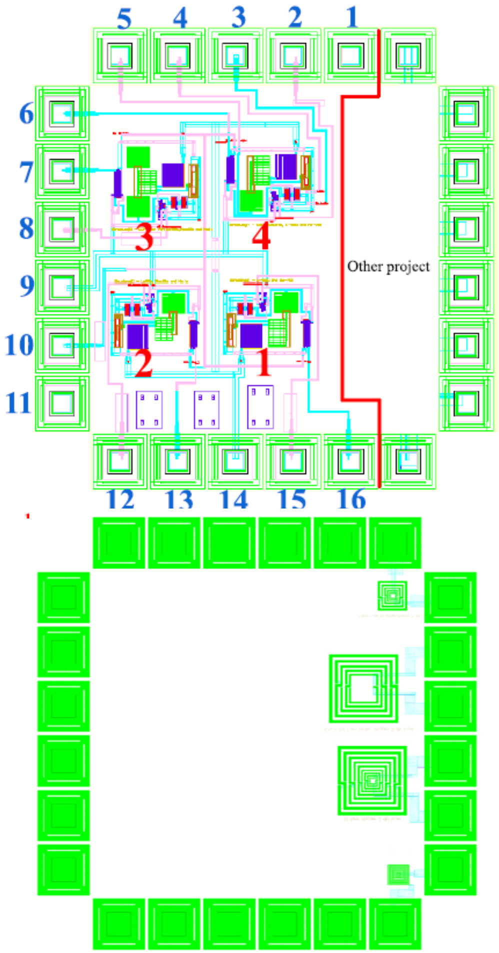
Fig. 18. Frequency response of the integrated poly-SiGe resonator and the CMOS amplifier tested in air.

A. Franke PhD

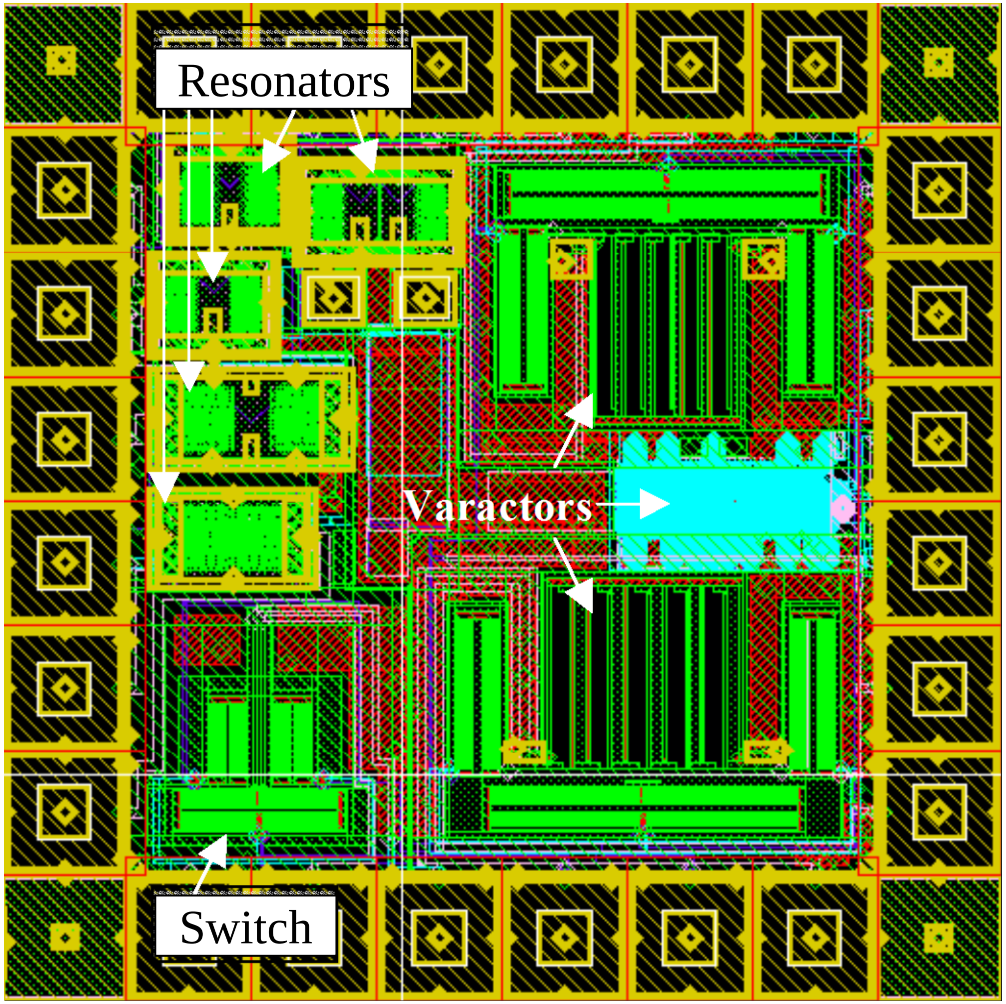
CMOS-MEMS

- Implementation of MEMS-components by using an ordinary CMOS-process
  - ASIMPS:
    - CMP, ”Circuits Multi-Projets”, runs MPW
    - ST Microelectronics 0.25 µm BiCMOS
    - Postprocessing at Carnegie Mellon University
  - Test circuits designed at Ifi S2007
    - Jan Erik Ramstad, Jostein Ekre

- Typical process characteristics →



CMOS-MEMS circuit F2008



Jan Erik Ramstad
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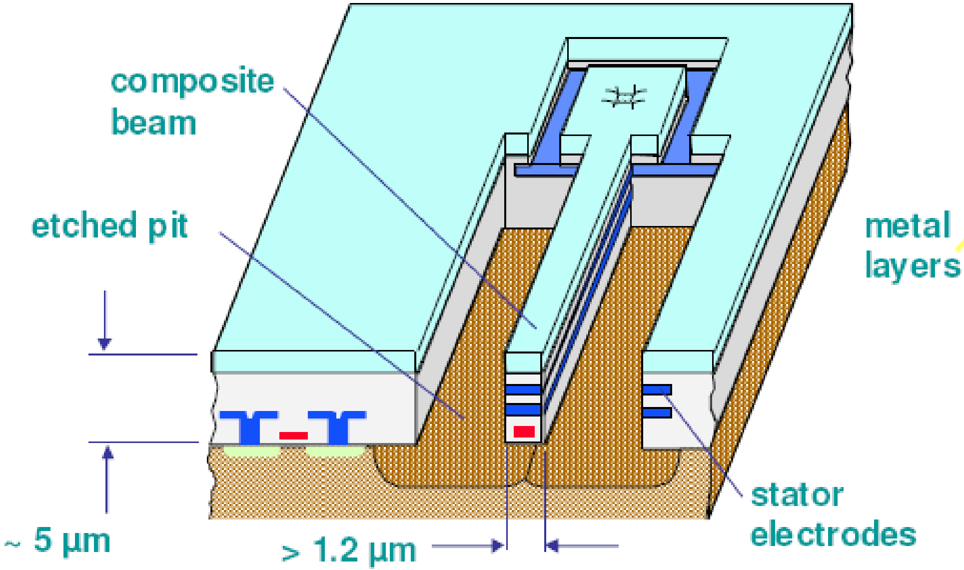
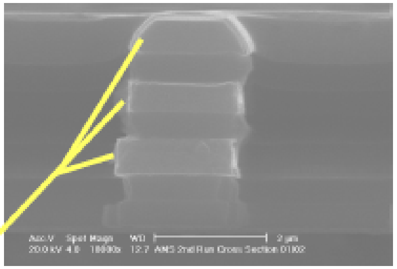
ASIMPS: CMOS-MEMS Process

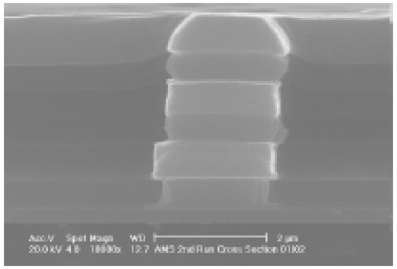
CNRS – INPG – UJF

- Microstructures made from conventional CMOS followed by two maskless post-CMOS process steps





M1-2-3 with field oxide



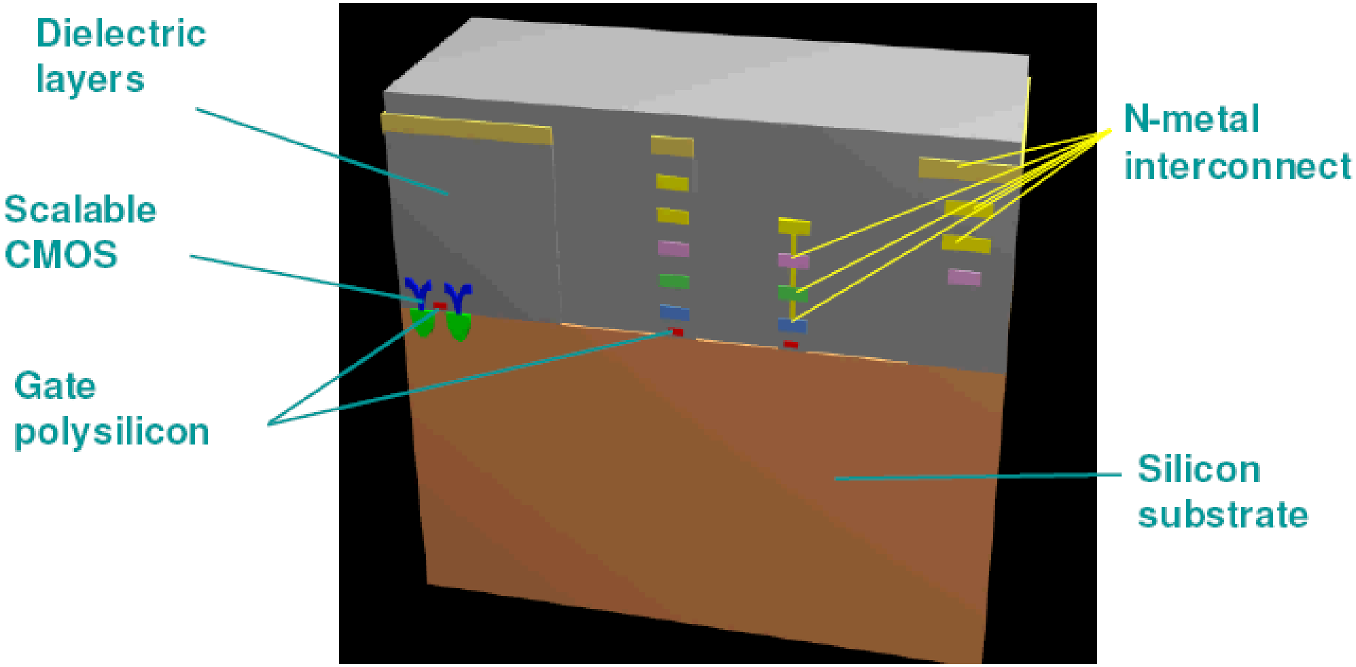
M1-2-3 w/o field oxide

- **Potential Applications**
  - **Inertial sensors, RF MEMS, infrared sensors, flow and force sensors, … with on-chip detection and conditioning**

G. Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

Post-CMOS Micromachining

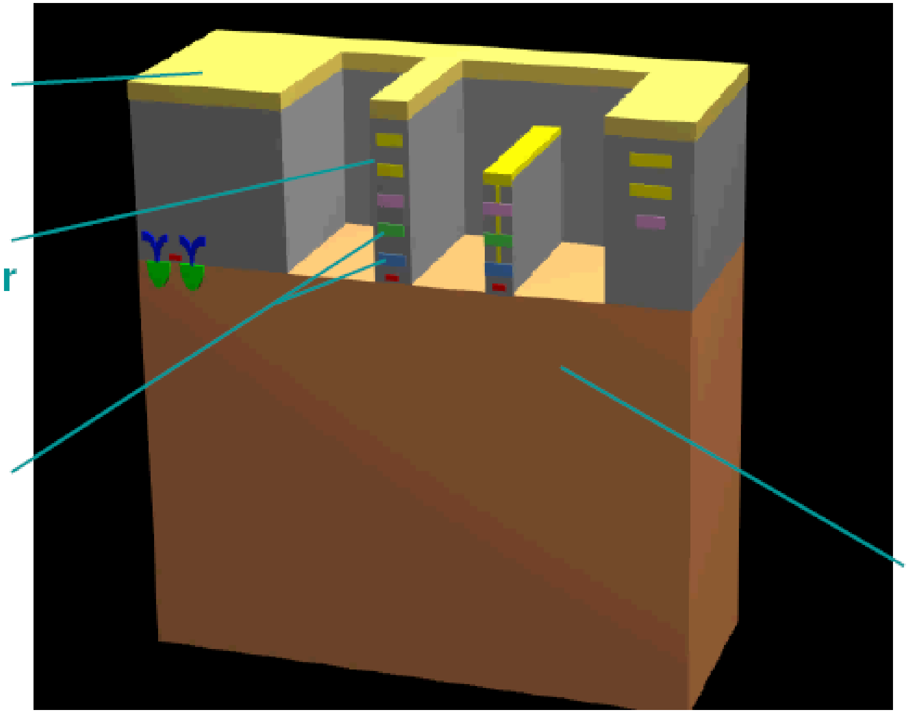
- Structures made using conventional CMOS
- Starting CMOS cross-section from the foundry:



G. Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

Post-CMOS Micromachining – Oxide RIE (2/2)

- Step 1: reactive-ion etch of dielectric layers
- Top metal layer acts as a mask & protects the CMOS



Metal mask layer

Composite structural layer

Electrically isolated interconnect on beam

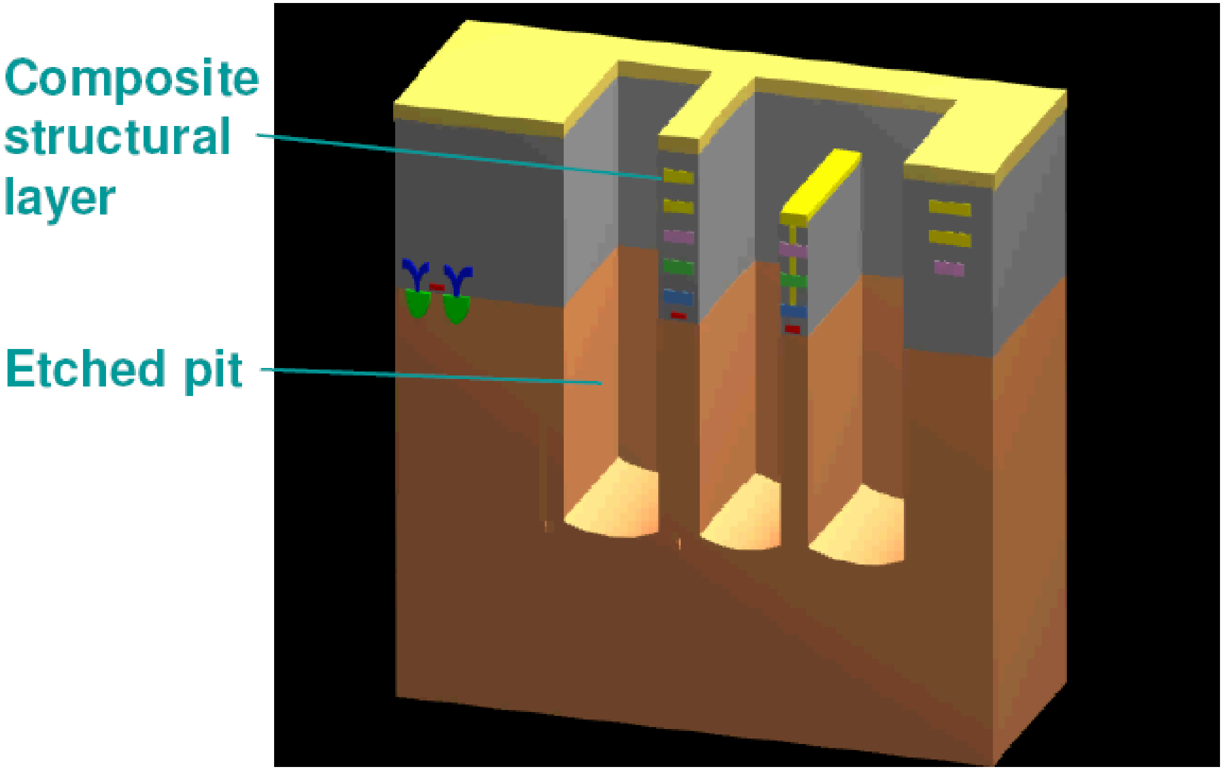
Exposed silicon

Gregory.DiPendina@imag.fr

Post-CMOS Micromachining – Si DRIE (2/2)

CNRS – INPG – UJF

- Step 2: DRIE of silicon substrate
- Spacing between structures and silicon is defined



ASIMPS at CMU

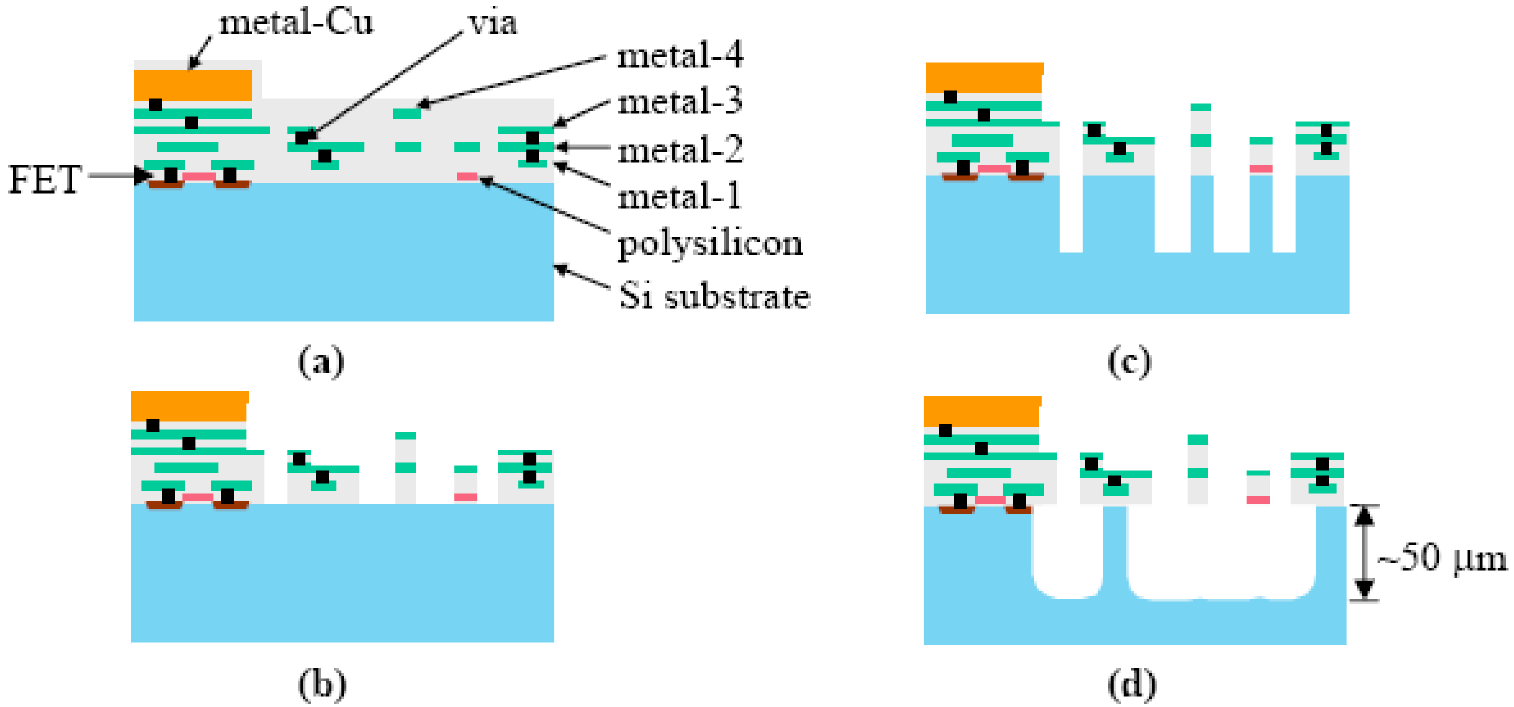
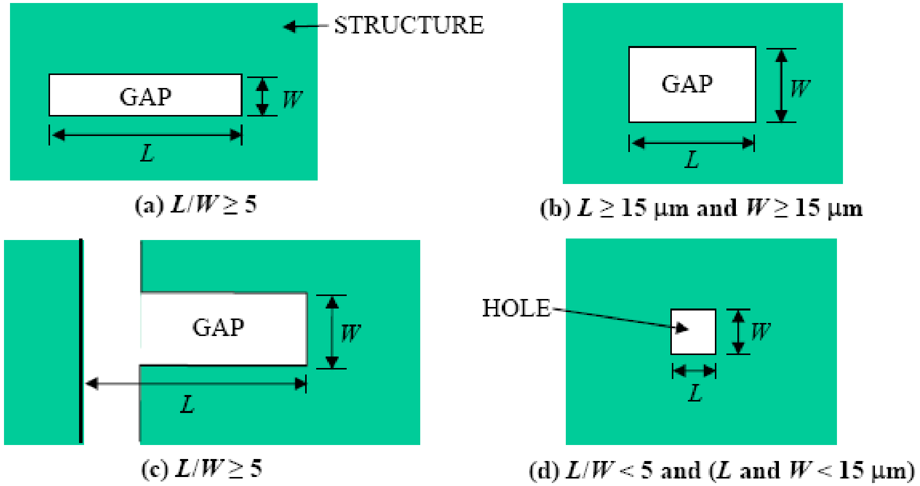


Figure 1. ST7RF CMOS MEMS process flow. (a) Foundry CMOS before micromachining; (b) CHF_3/O_2 reactive-ion etch of dielectric stack down to the silicon substrate; (c) Deep reactive-ion etch of Si substrate (nominal 35 μm deep); and (d) Si undercut (nominal 15 μm undercut and 50 μm deep).

Specific design rules are required



(a) $L/W \geq 5$

(b) $L \geq 15$ µm and $W \geq 15$ µm

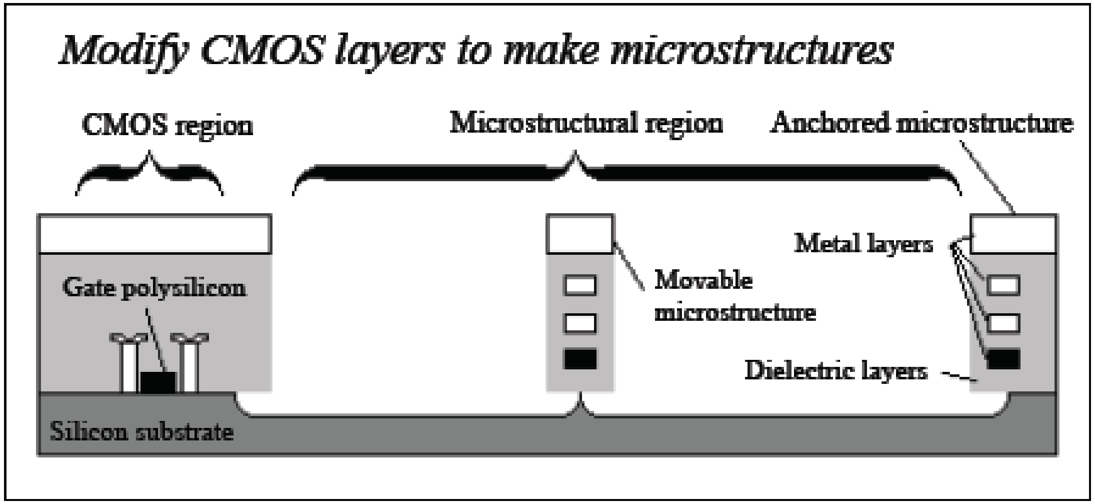
(c) $L/W \geq 5$

(d) $L/W < 5$ and (L and $W < 15$ µm)

Figure 2. Illustrations of GAP and HOLE.

Ex. of ASIMPS design rules

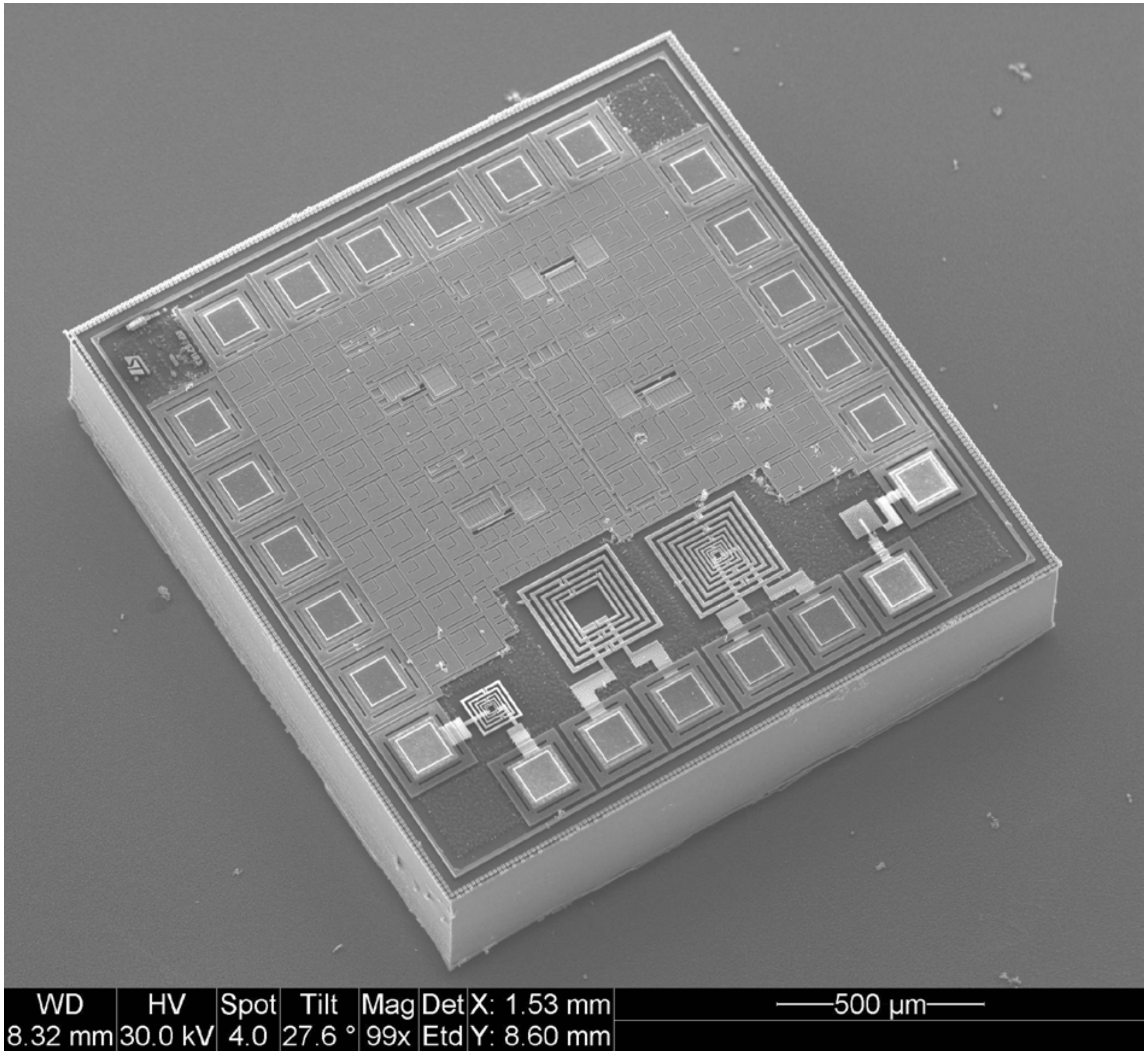
European ASIMPS: critical characteristics



(CMU)

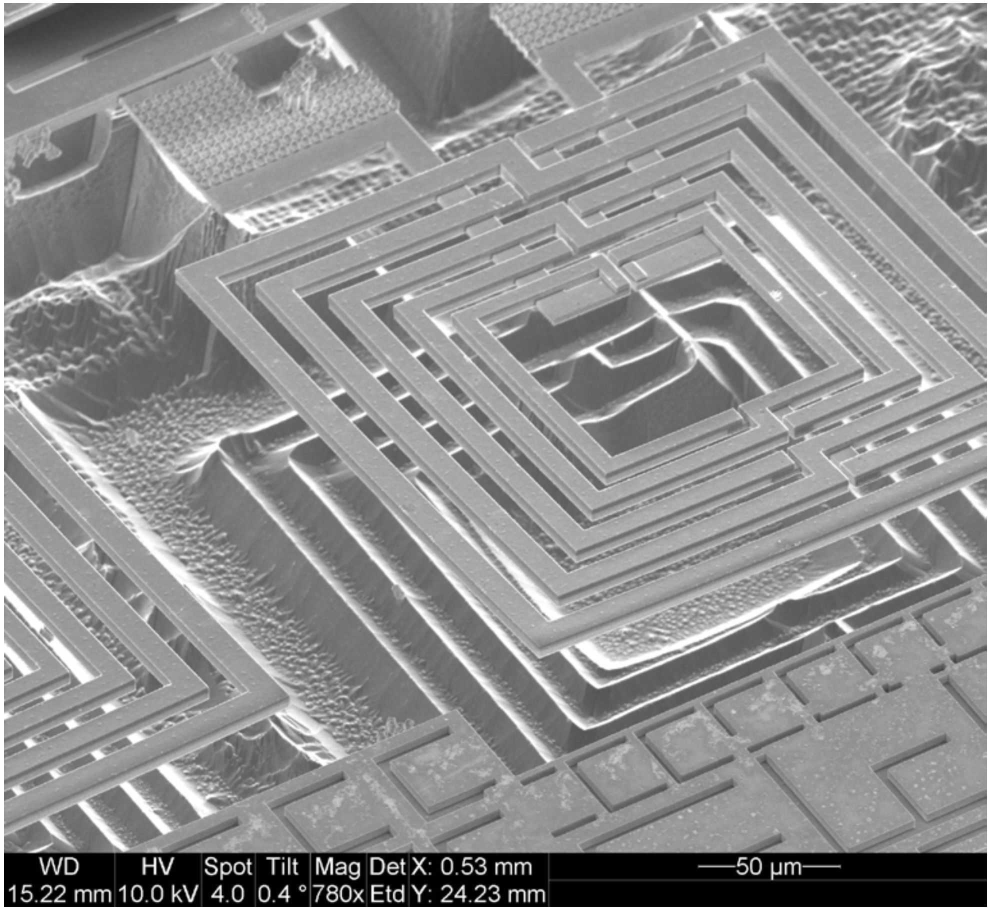
- Multilayer structure of metal + dielectric
- 5 metal layers
- Top metal layer used as mask
- MEMS released in a mask-less etch step
- RIE + isotropic under-etch
- CMOS must be covered by metal
- Specific MEMS design rules

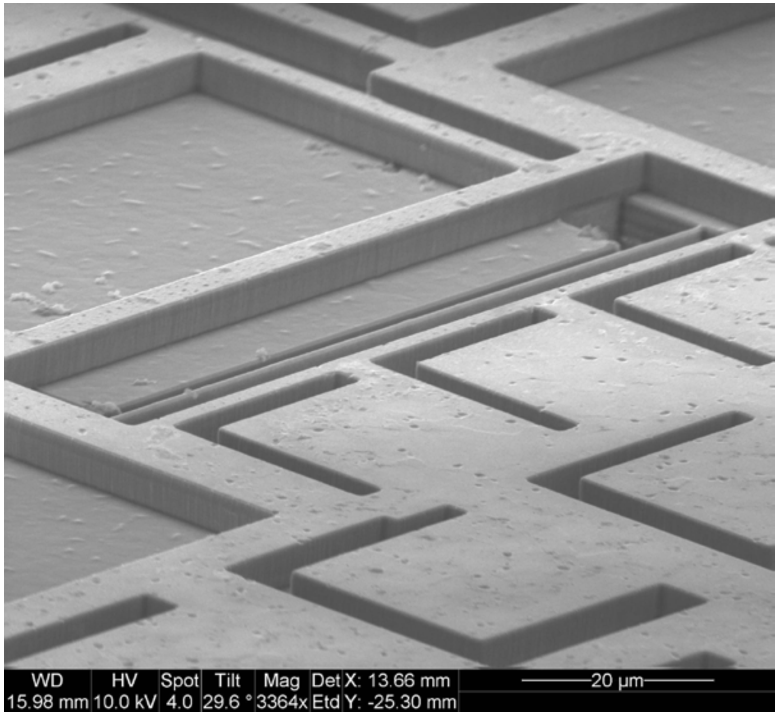
- Can exploit enormous investments in CMOS-process development



RIE -etched
at MiNaLab

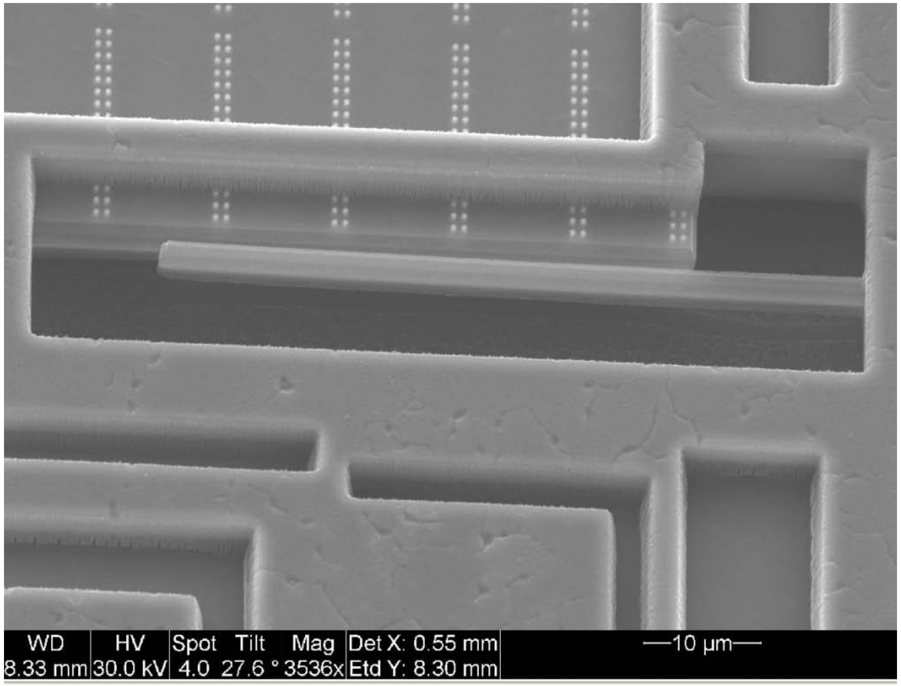
IFI test circuits from STM (JER, JE)

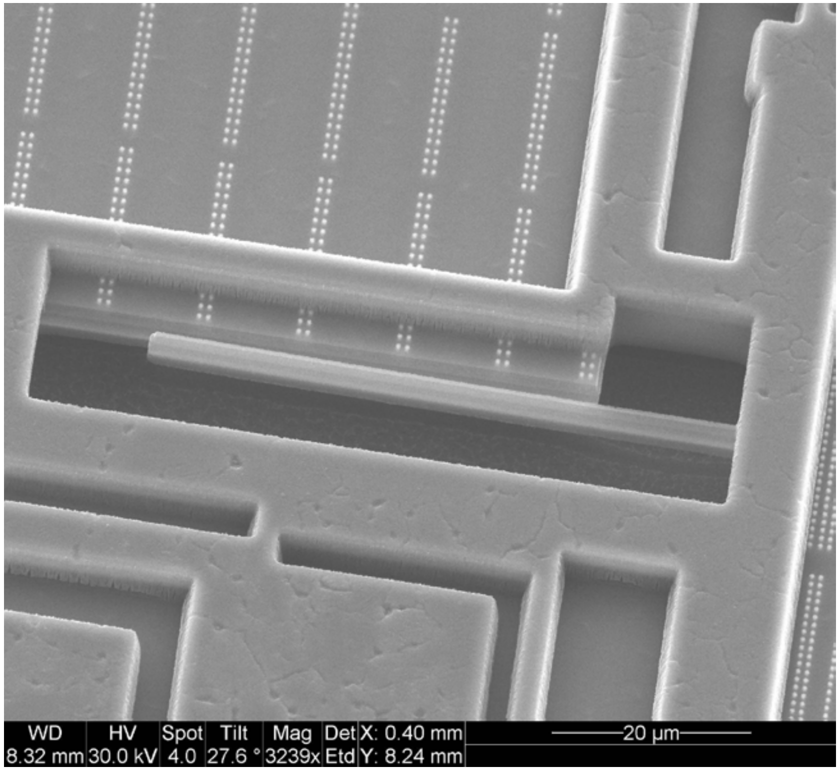




Details from IFI test circuit
Postprocessed at CMU

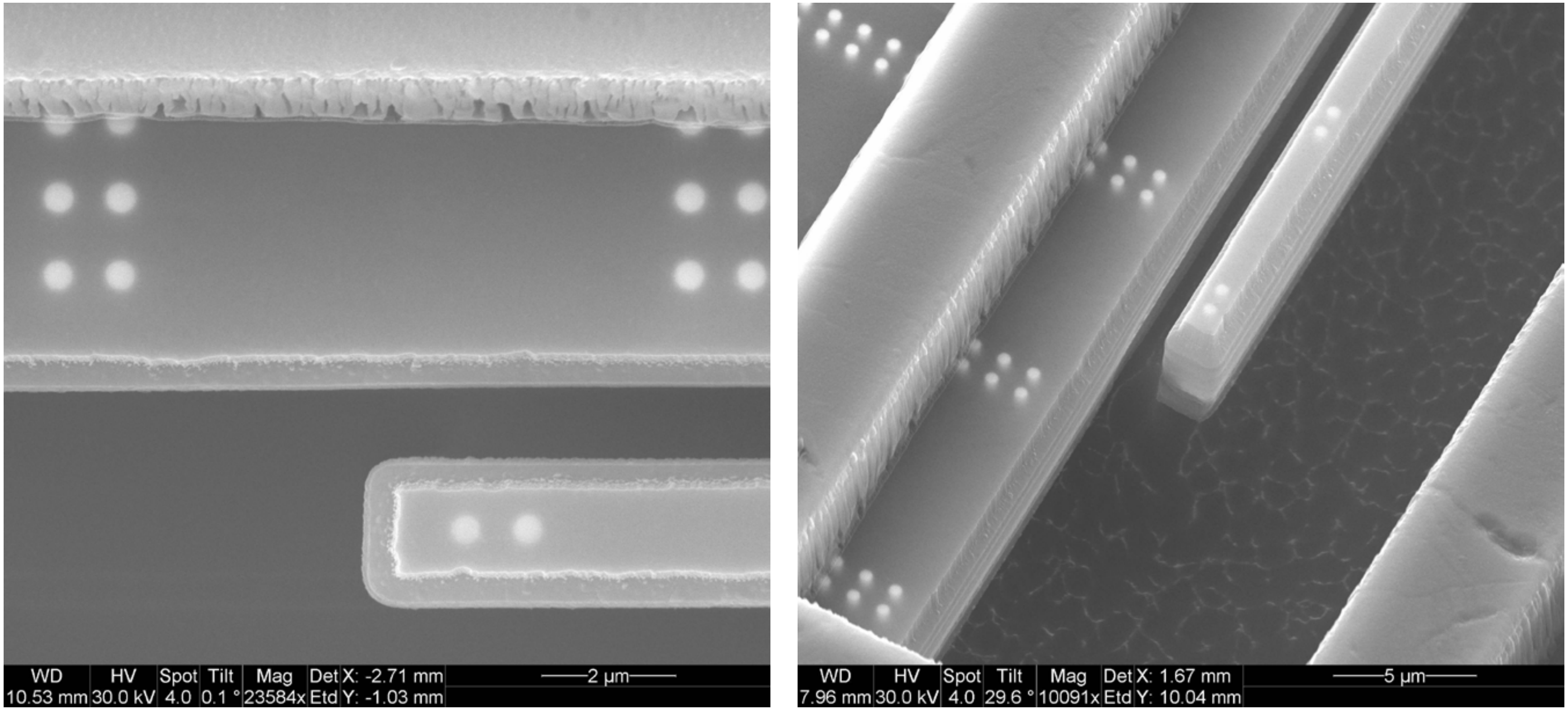
MiNaLab: post-CMOS etching of STM circuit





MiNaLab: After unisotropic etch

Laterally moving cantilever beam (JER)



MiNaLab: high ion energy used → top layer is heavily eroded (initial run)

Other integration methods

- Bonding processes may be used
  - IC circuits and micromechanics merged by bonding one wafer onto the other
    - F.ex. **Anodic bonding**
  - Alternatively: Bond an IC-circuit on a MEMS structure
  - Alternatively: Bond MEMS on an IC circuit
    - Reducing the bonding pad dimensions may give acceptable interface **capacitance values** for the IC circuits